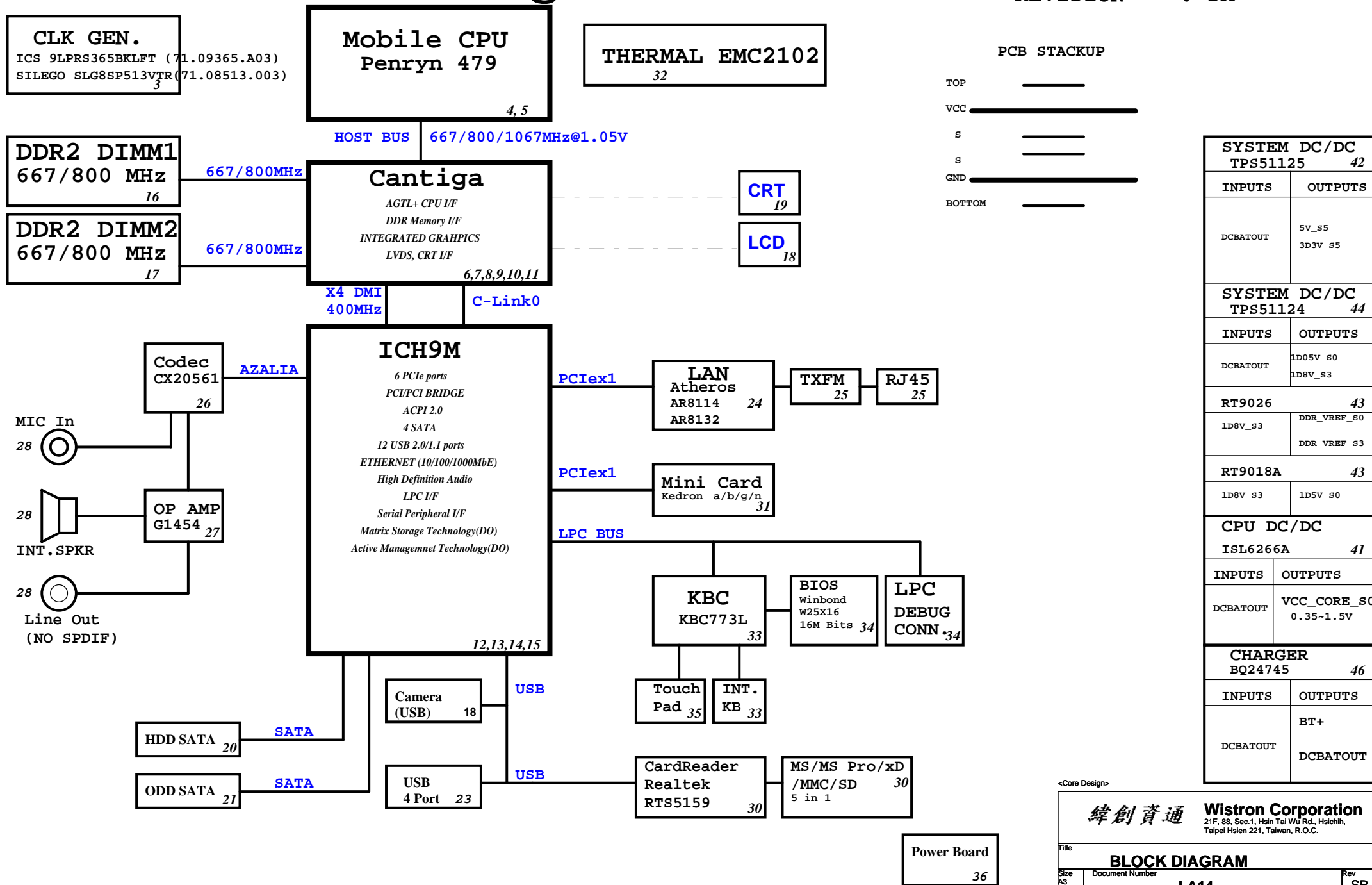


# LA14 Block Diagram

Project code: 91.4BW01.001  
PCB P/N : 48.4BW01.01M  
REVISION : SA



ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h) . This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#/GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#:SPI_CS1#/GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage. Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resistor.

ICH9M Integrated Pull-up and Pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRS LPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native LAN. GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH [3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5 page 218

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) 1=The iTPM Host Interface is disalbed(default)
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality (default)
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. 1= Normal operation(Default):Lane Numbered in order
CFG10	PCIE Loopback enable	0 = Enable (Note 3) 1= Disabled (default)
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) 11 = Disabled (default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation(Default): Lane Numbered in Order 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3 DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display Port or PCIE is operational (Default) 1 = Digital display Port and PCIE are operating simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 =No SDVO Card Present (Default) 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1= LFP Card Present; PCIE disabled

NOTE:  
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.  
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.  
Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

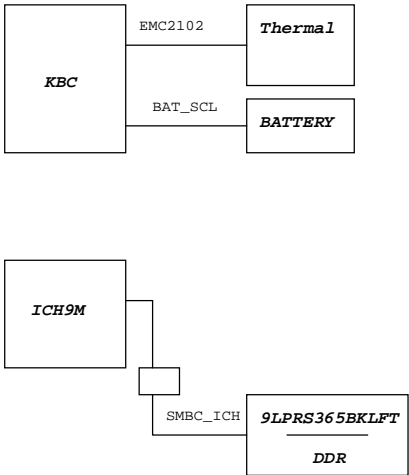
USB Table

USB	
Pair	Device
0	USB1
1	NC
2	NC
3	MINIC1
4	WEBCAM
5	NC
6	NC
7	Bluetooth
8	NC
9	USB2(High speed)
10	NC
11	CardReader

PCIE Routing

LANE1	LAN Atheros AR8114A
LANE2	MiniCard WLAN
LANE3	NC
LANE4	NC
LANE5	NC
LANE6	NC

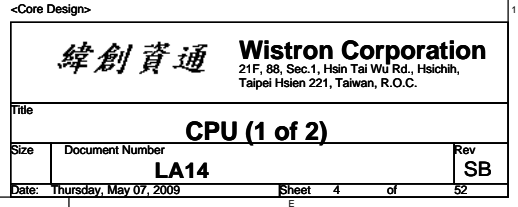
SMBus



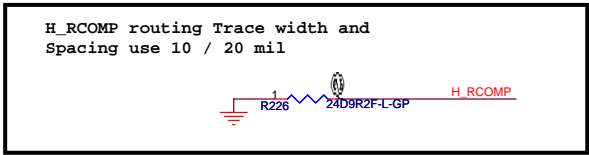
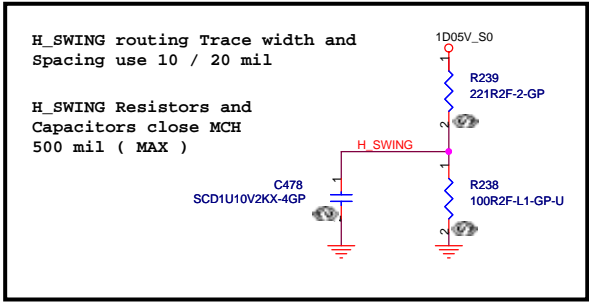
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<b>緯創資通 Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
Reference	
Size A3	Document Number
LA14	
Date: Thursday, May 07, 2009	Rev SB
Sheet 2	of 52

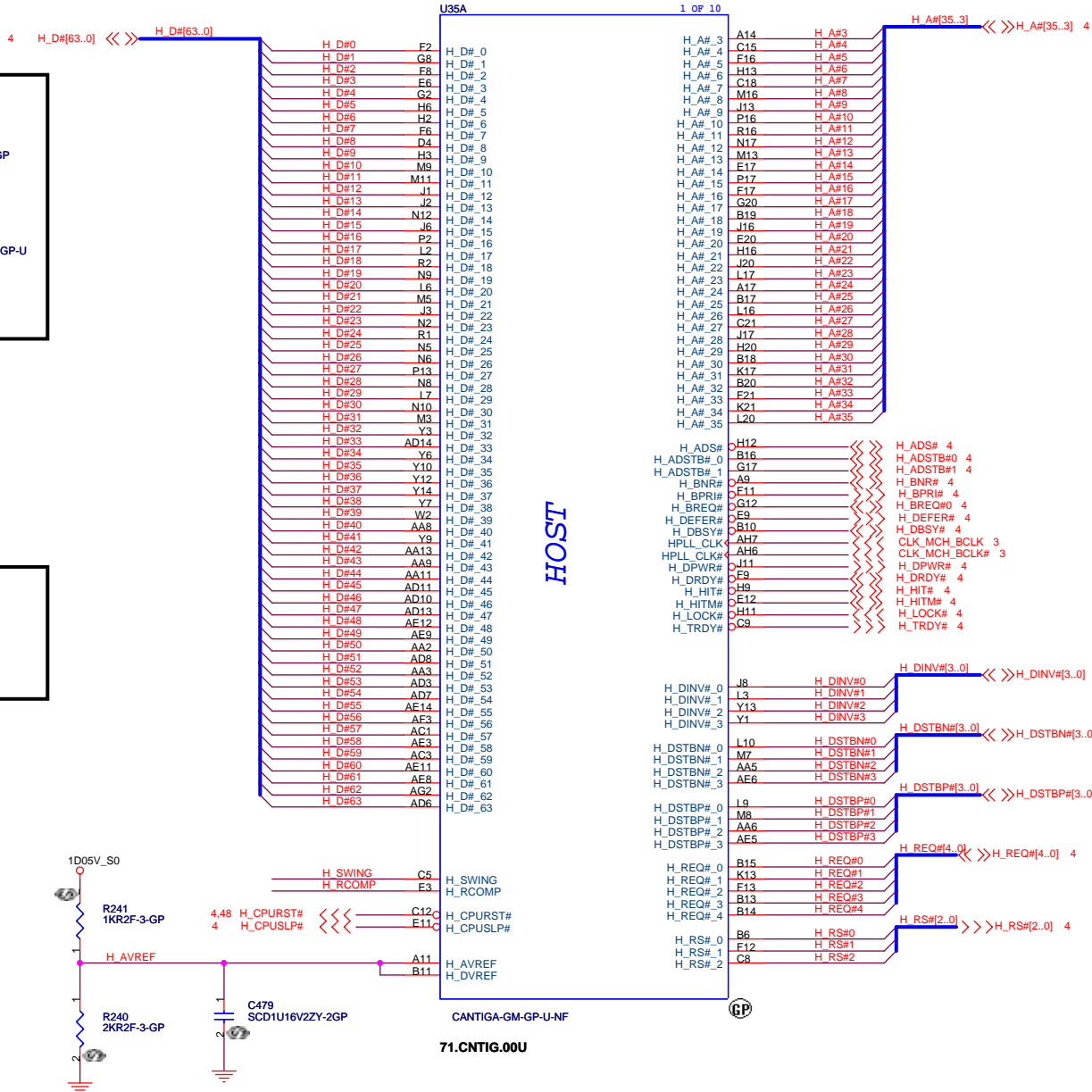




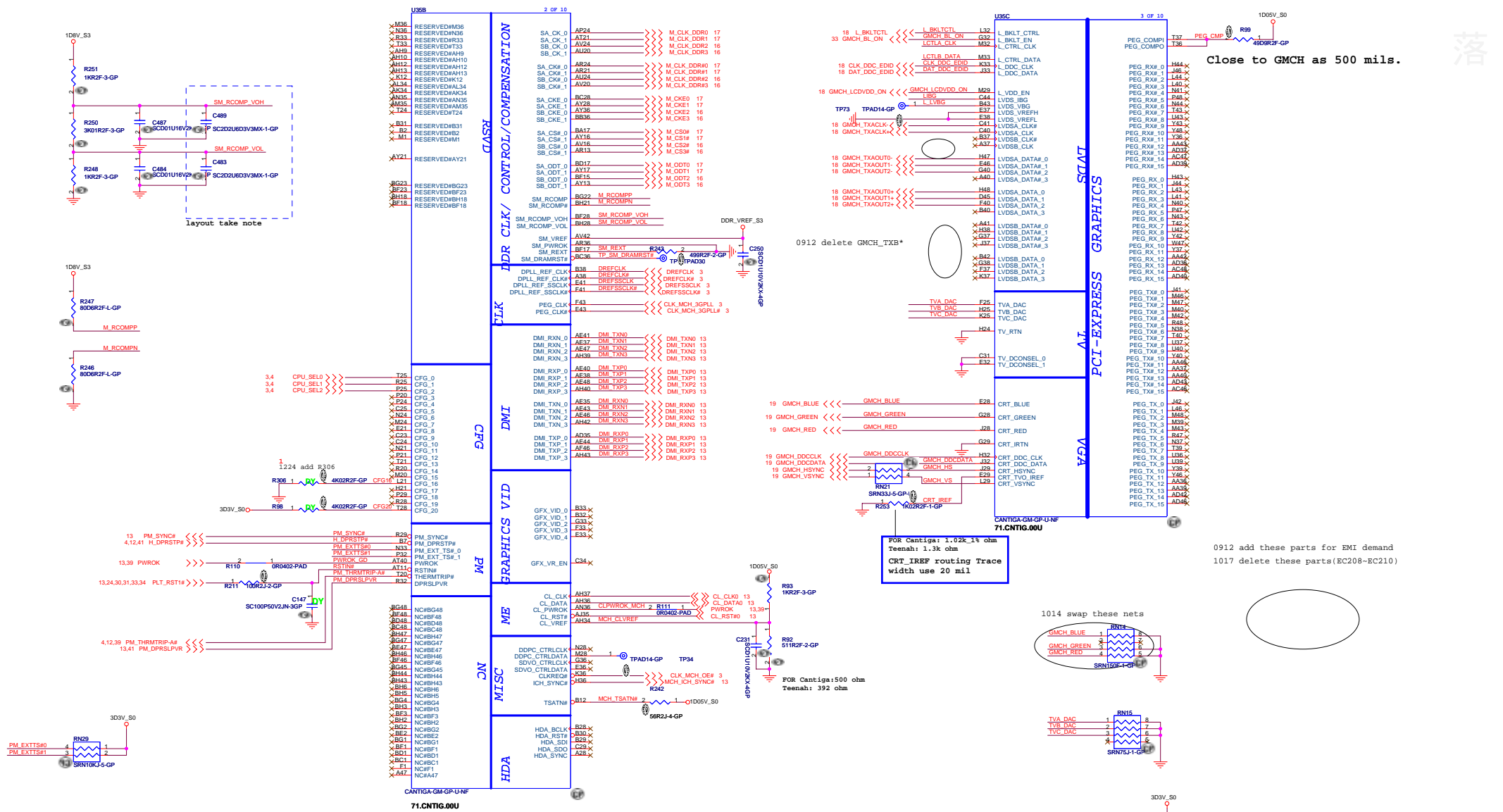




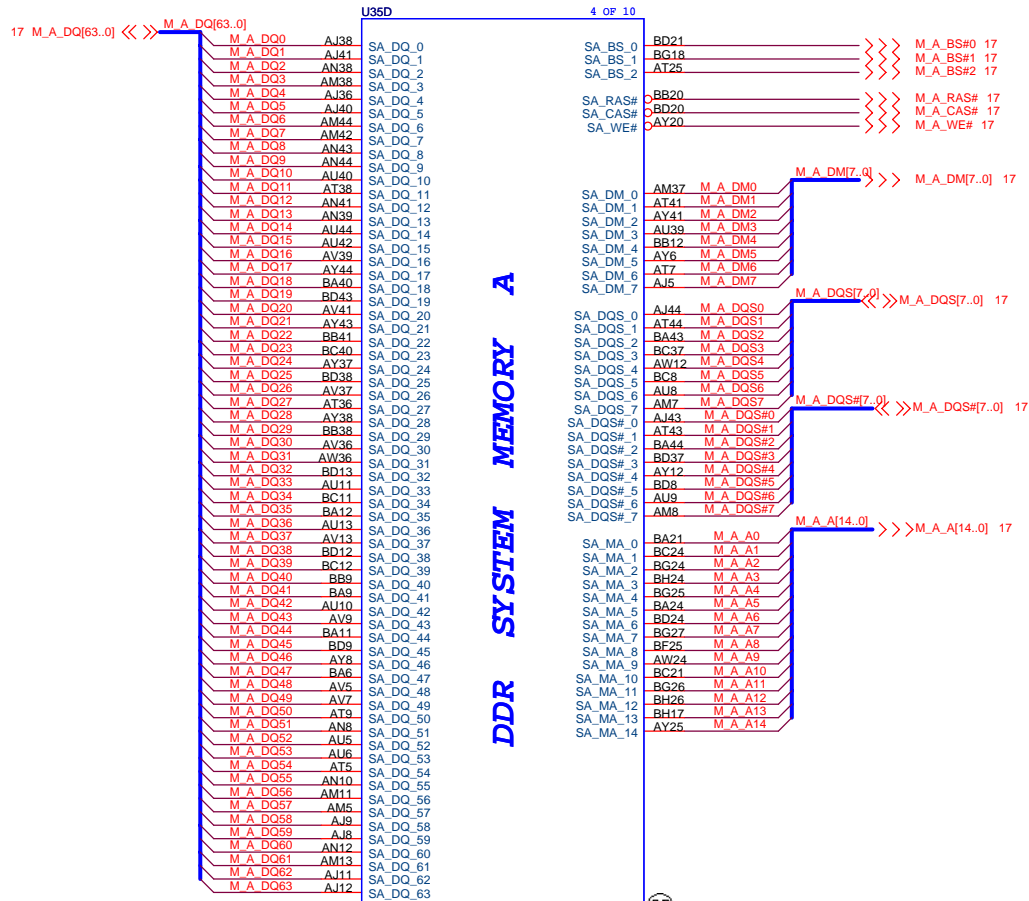
Place them near to the chip ( < 0.5")





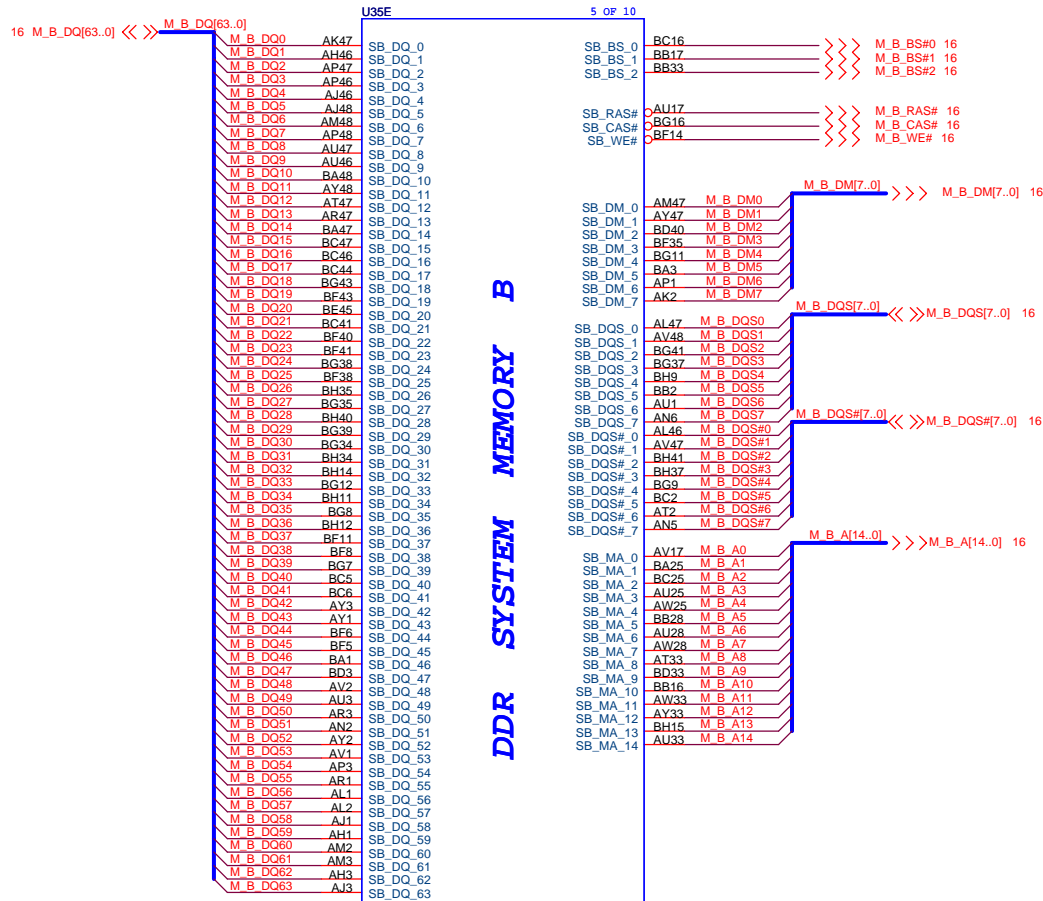


Pin Name	Strap Description	Configuration
CFG20	Digital DisplayPort (SDVO/DP/HDMI) Concurrent with PCIE	Low = Only digital DisplayPort (SDVO/DP/HDMI) or PCIE is operational (default) High = Digital DisplayPort (SDVO/DP/HDMI) and PCIE are operating simultaneously via the PEG port



CANTIGA-GM-GP-U-NF

71.CNTIG.00U



CANTIGA-GM-GP-U-NF

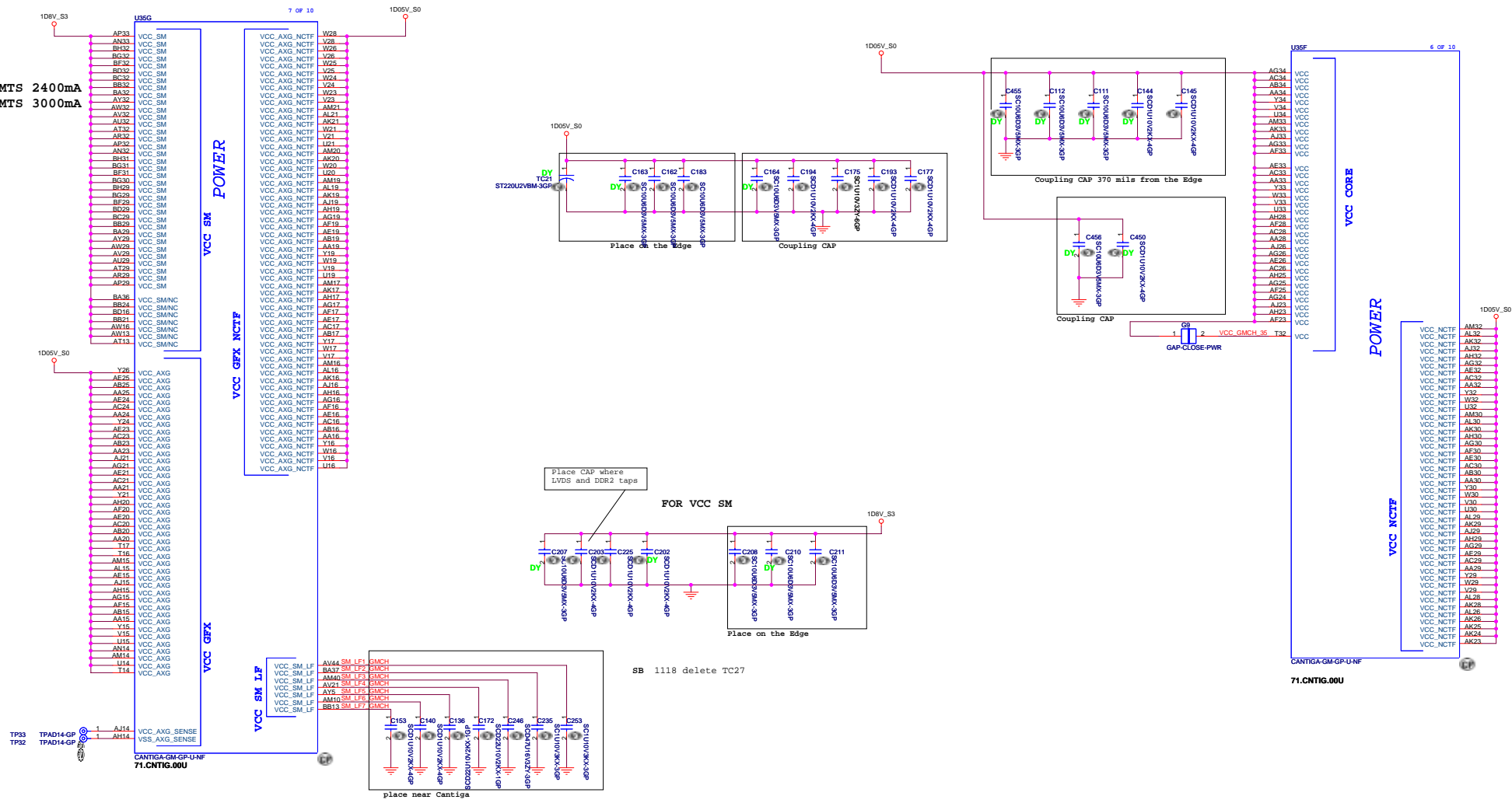
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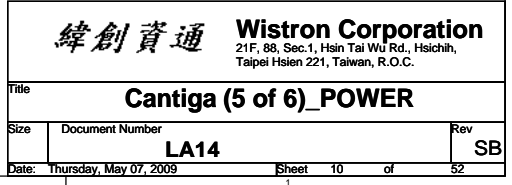
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin,  
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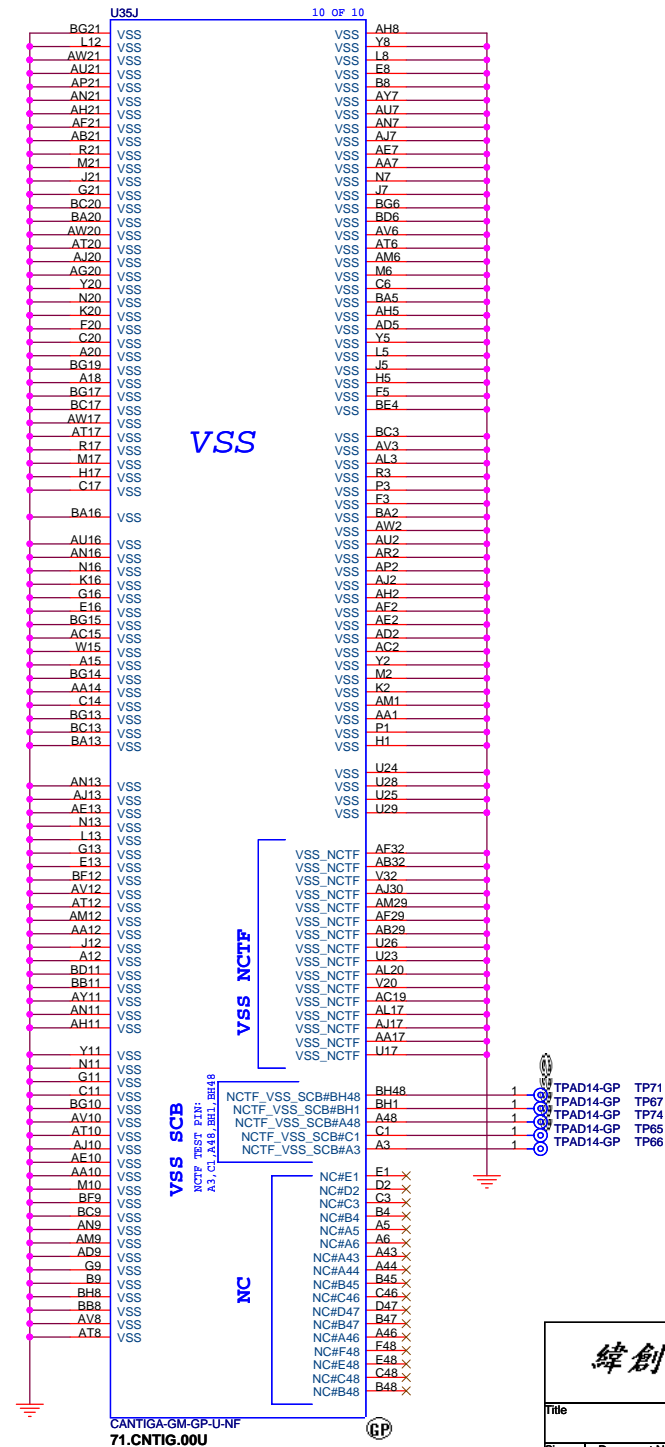
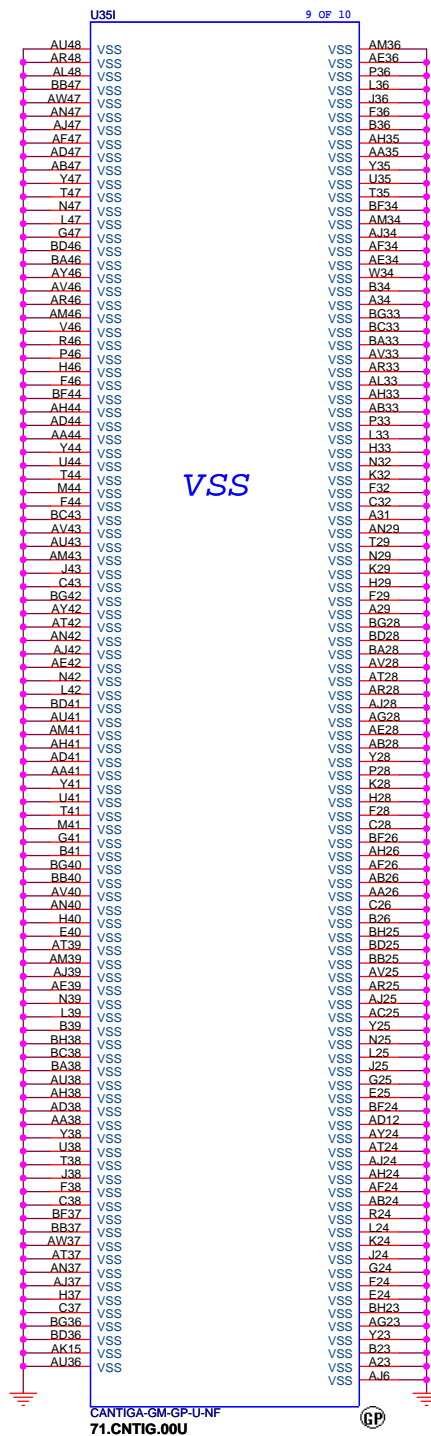
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Cantiga (3 of 6) DDR		
Size	Document Number	Rev
	LA14	SB
Date:	Thursday, May 07, 2009	Sheet 8 of 52

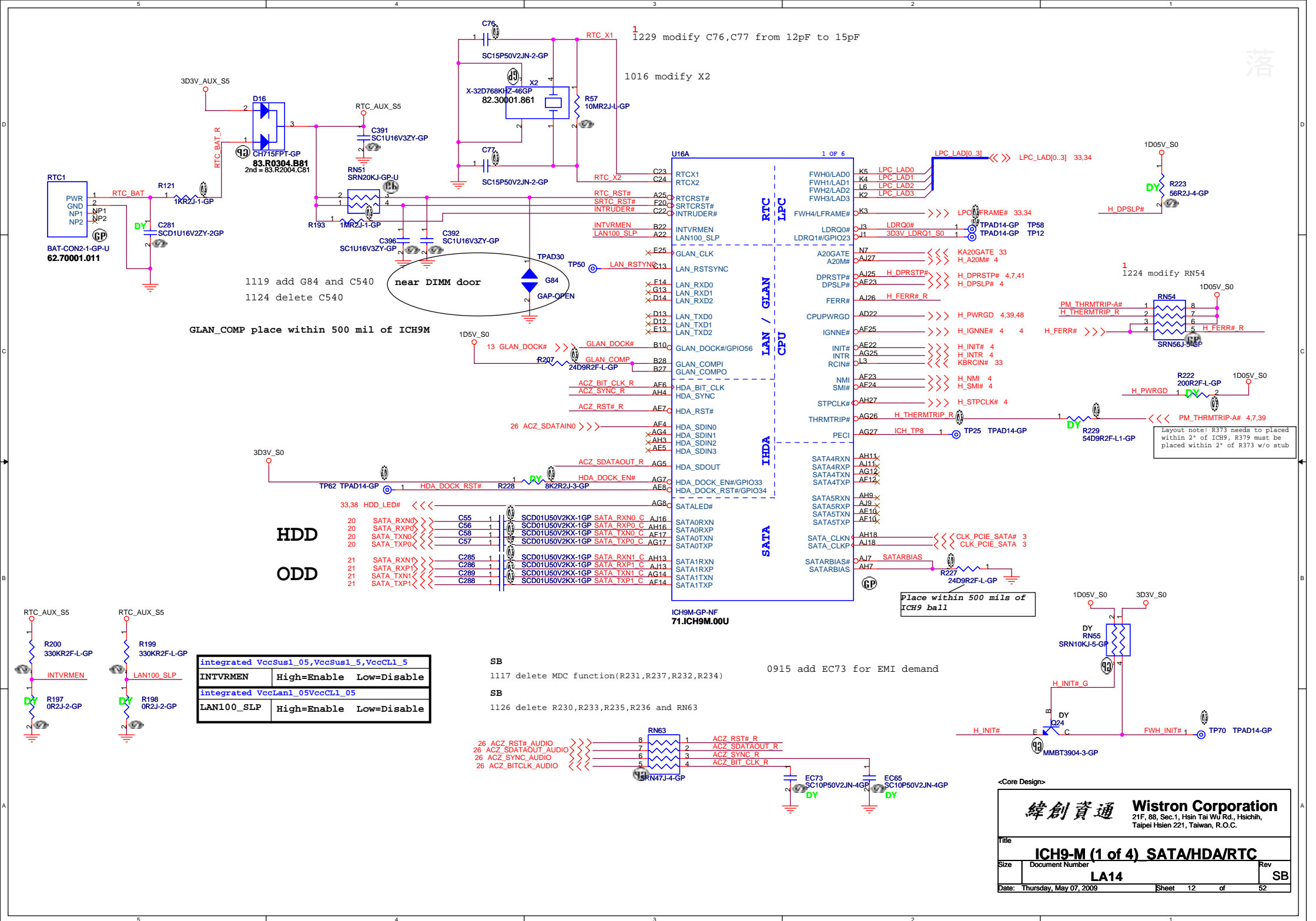


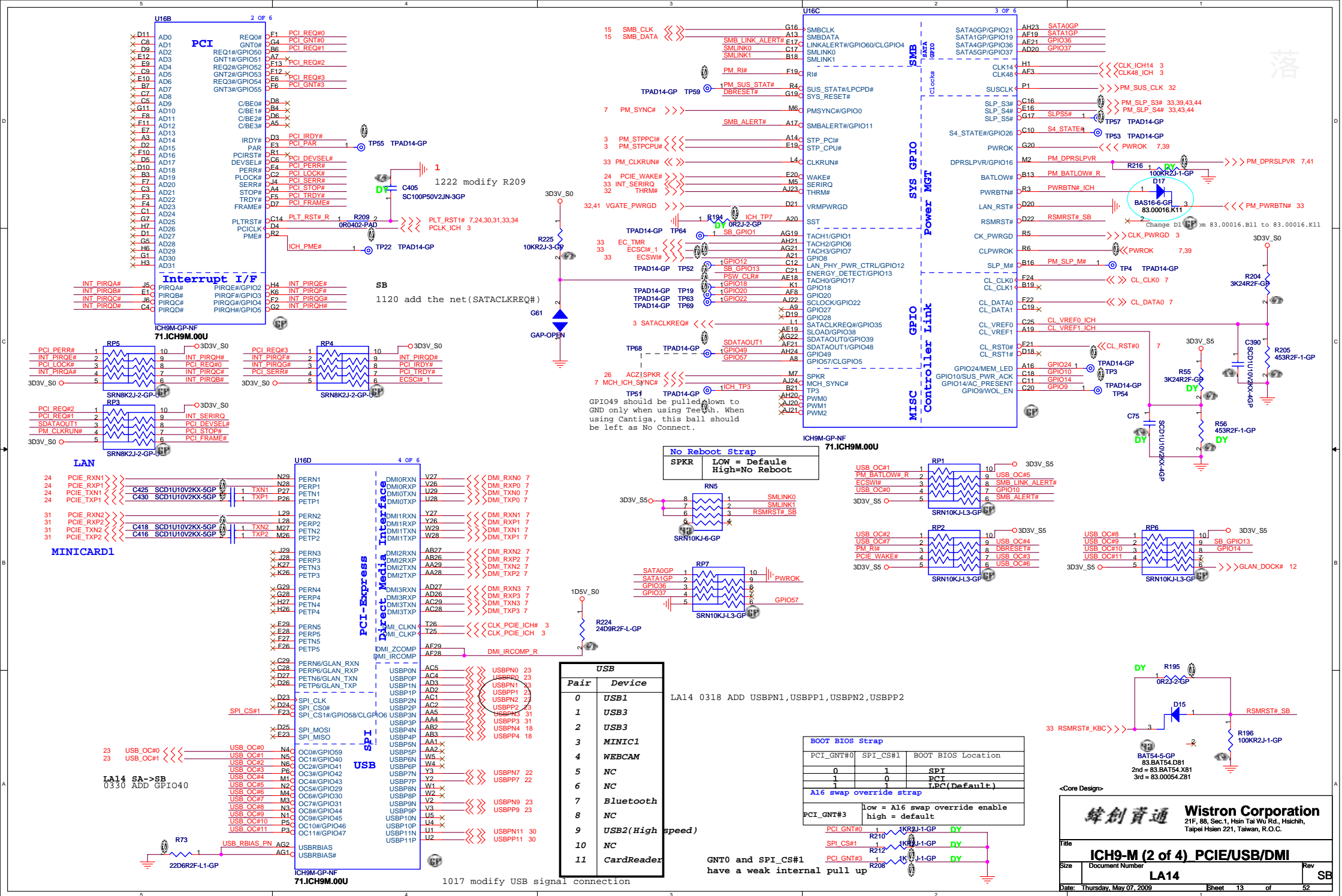
667MTS 2400mA  
800MTS 3000mA







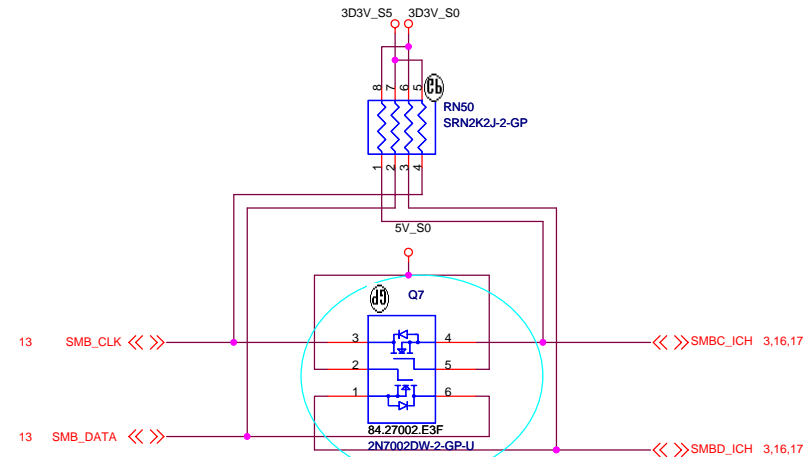
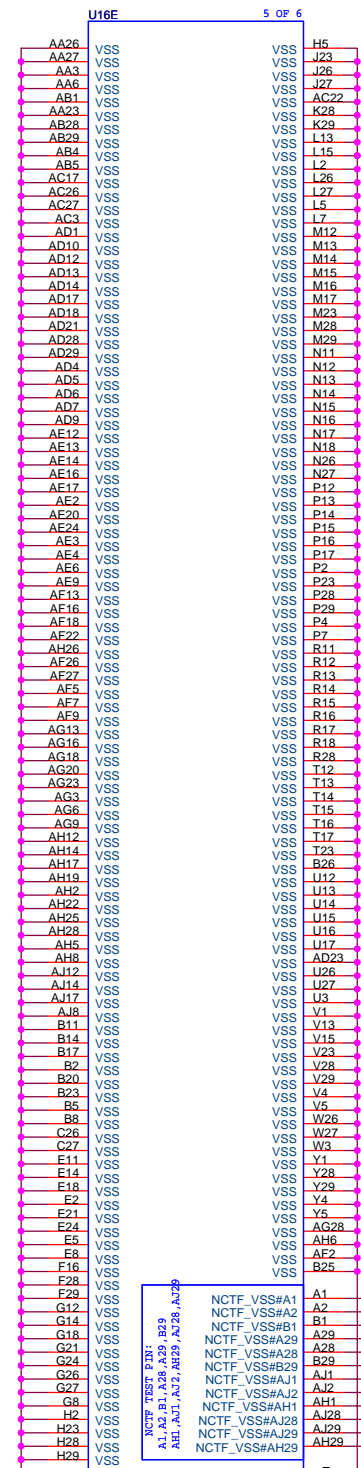






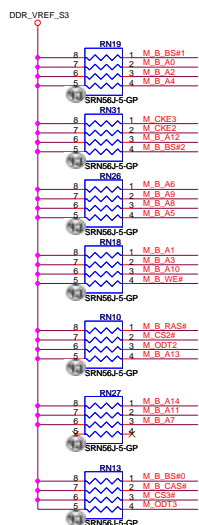




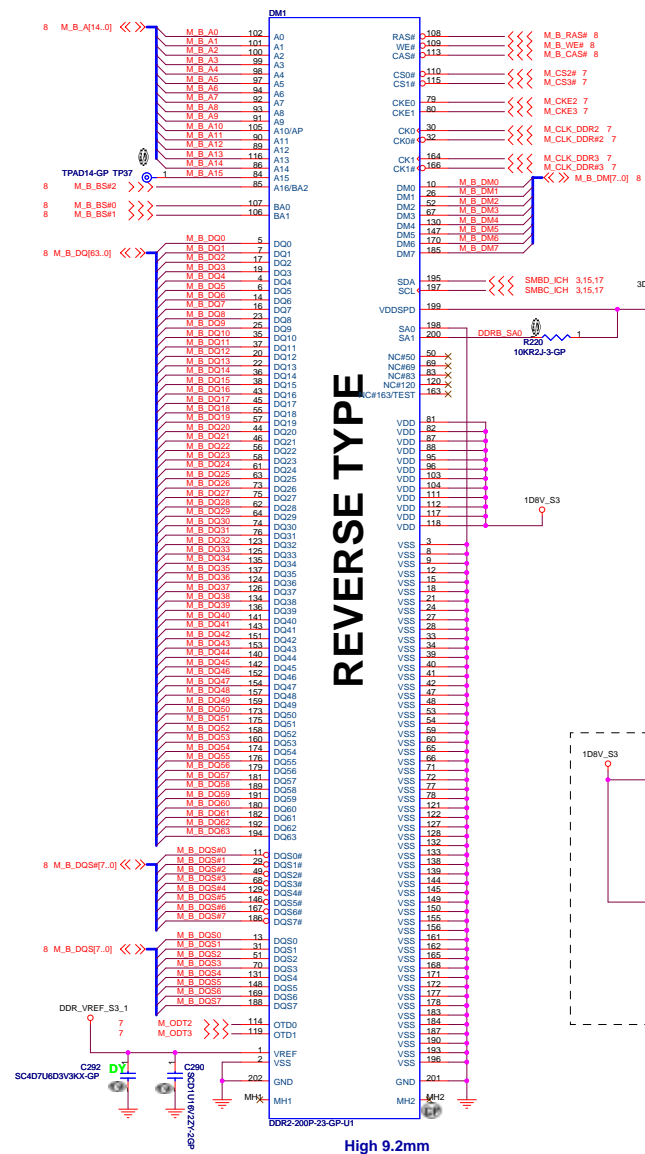
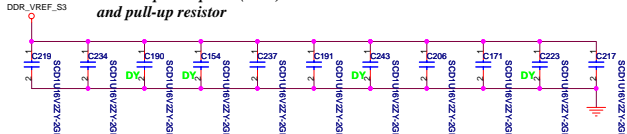


*Put decap near power(0.9V) and pull-up resistor*

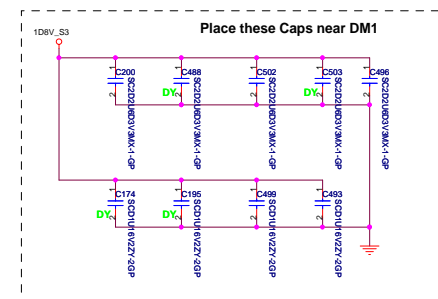
*Put decap near power(0.9V) and pull-up resistor*



*Put decap near power(0.9V)  
and pull-up resistor*



## REVERSE TYPE

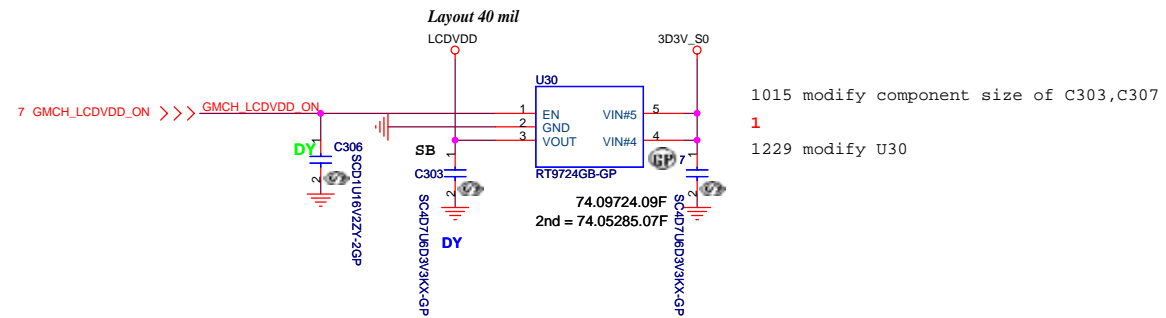
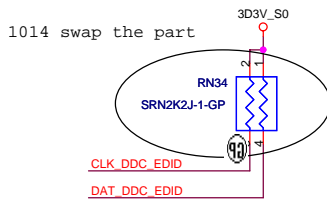
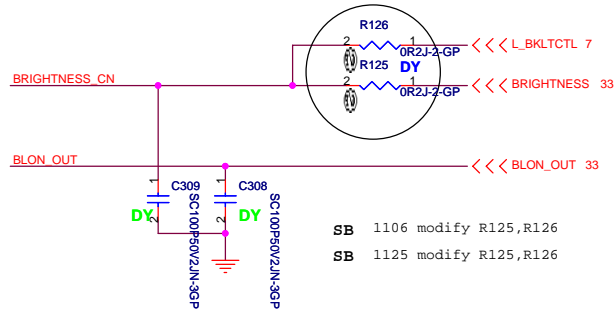
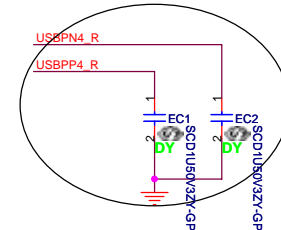
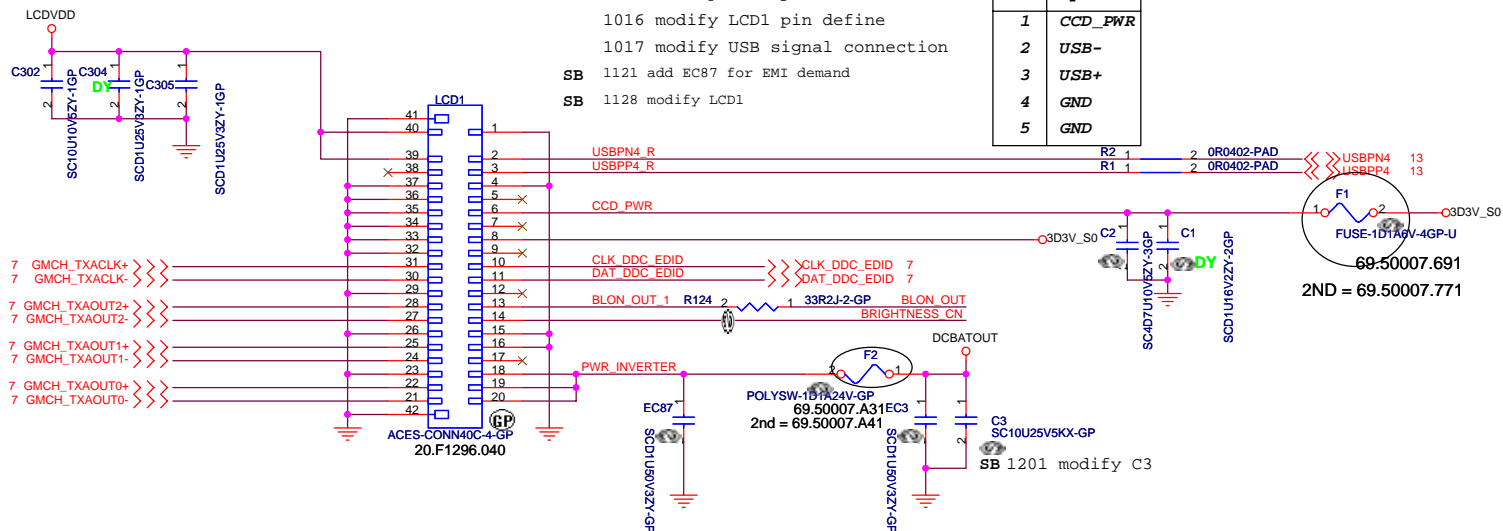




# LCD/CCD CONN

- 1015 modify F1  
1015 modify LCD1 pin define  
1016 modify LCD1 pin define  
1017 modify USB signal connection  
SB 1121 add EC87 for EMI demand  
SB 1128 modify LCD1

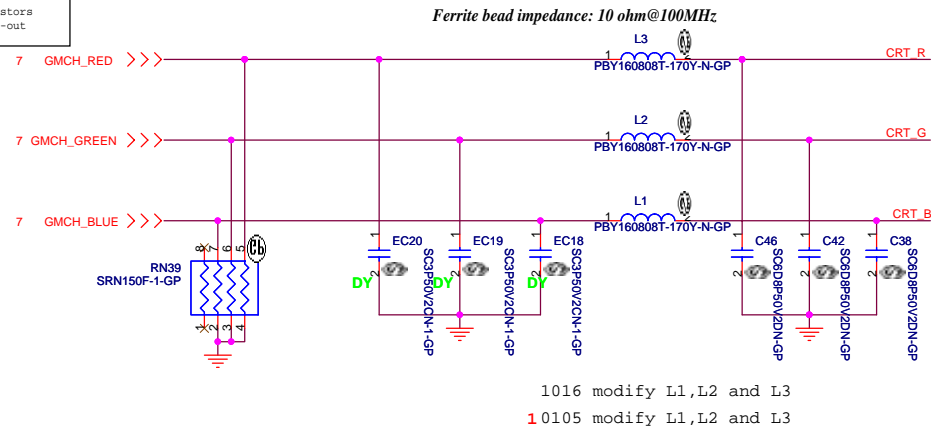
Pin	Symbol
1	CCD_PWR
2	USB-
3	USB+
4	GND
5	GND



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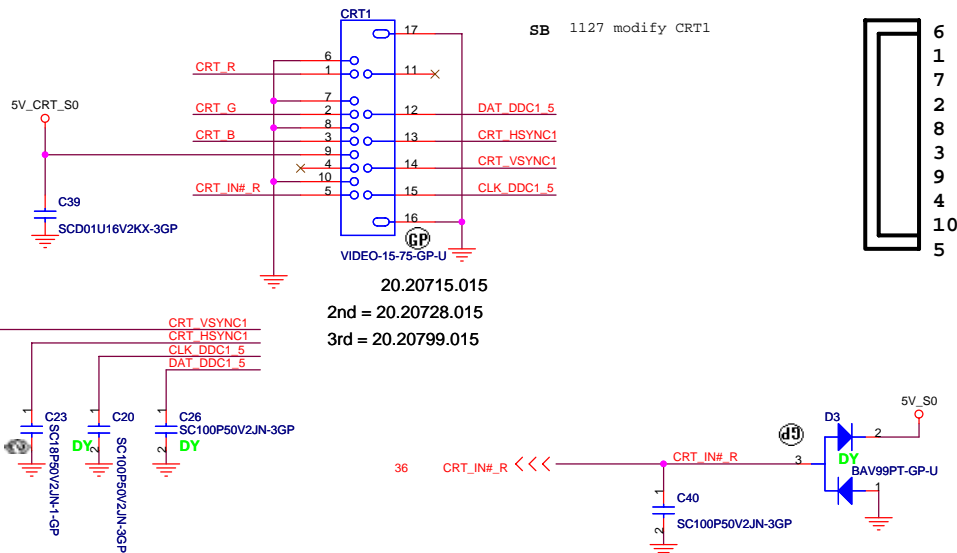
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Title			
<b>LCD CONN</b>			
Size	Document Number		Rev
	<b>LA14</b>		<b>SB</b>
Date:	Thursday, May 07, 2009	Sheet 18 of	52

Layout Note:  
Place these resistors  
close to the CRT-out  
connector

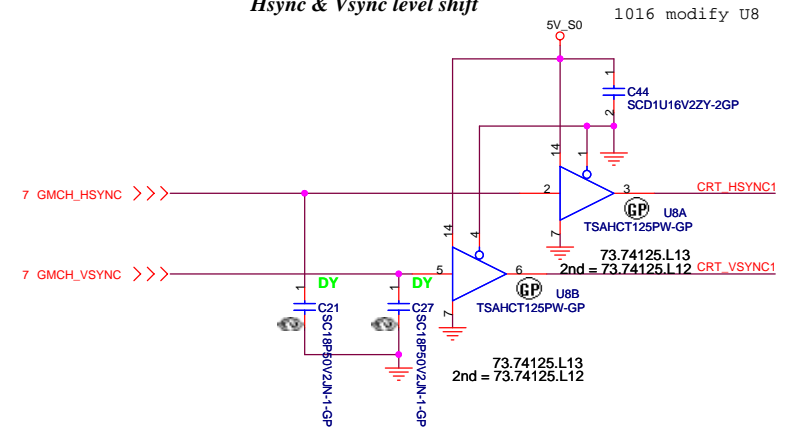


**Layout Note:**  
\* Must be a ground return path between this ground and the ground on the VGA connector.  
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

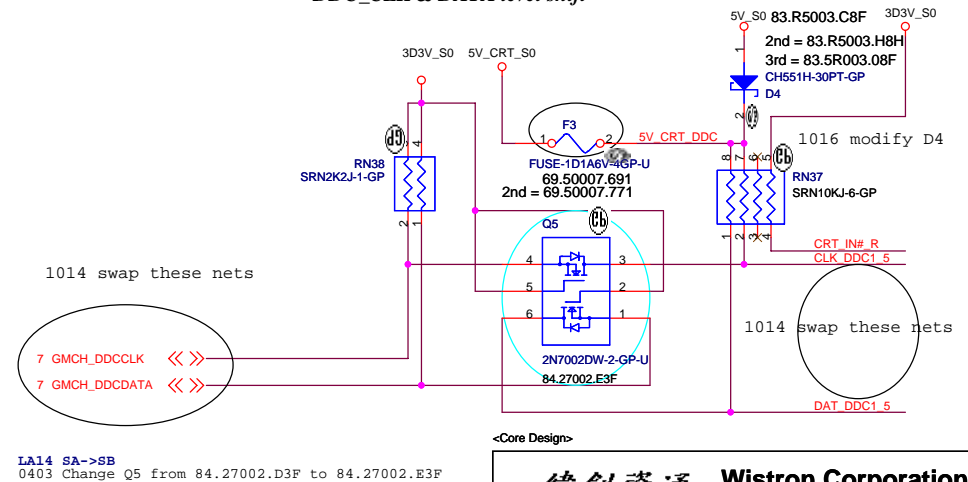
## CRT I/F & CONNECTOR



## Hsync & Vsync level shift



## DDC\_CLK & DATA level shift



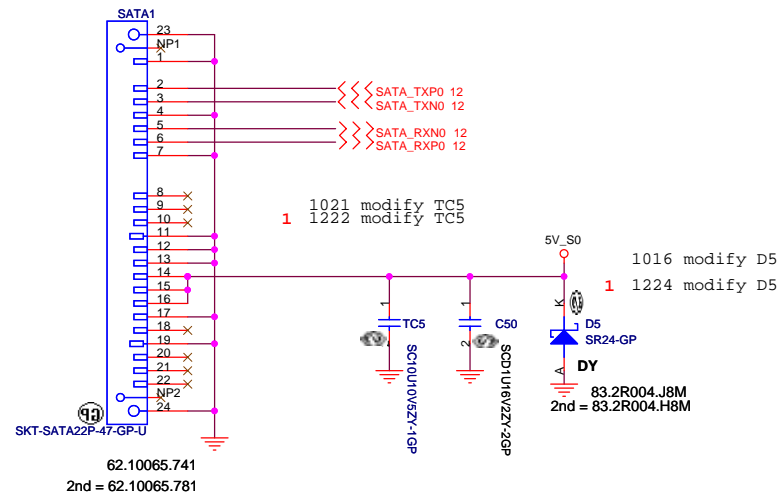
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Title	CRT Connector		Rev
Size	Document Number	LA14	SB
Date:	Thursday, May 07, 2009	Sheet	19 of 52

# SATA Connector

0912 add these parts for EMI demand  
1001 delete these parts for EMI demand  
1021 modify SATA1

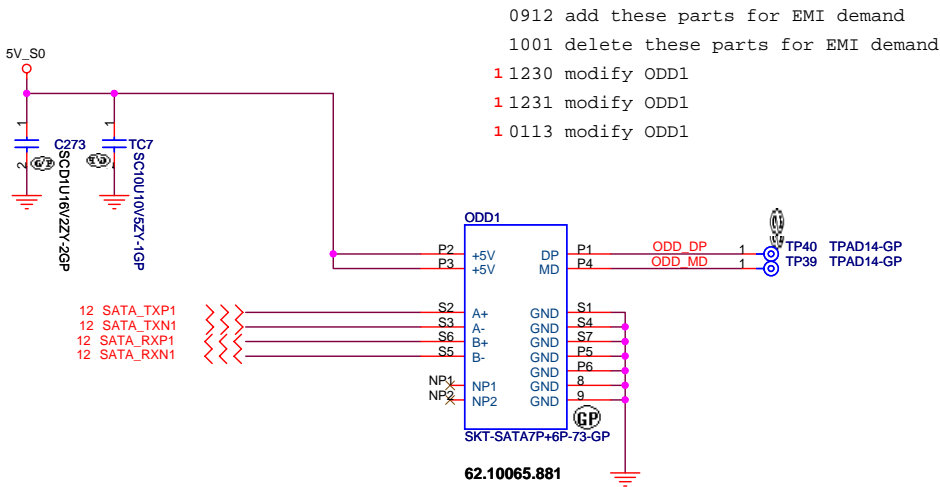


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Title			
<b>HDD</b>			
Size	Document Number		Rev
	<b>LA14</b>		<b>SB</b>
Date:	Thursday, May 07, 2009	Sheet 20 of	52



# SATA ODD Connector



<Core Design>

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Title			
<b>ODD</b>			
Size	Document Number		Rev
	<b>LA14</b>		<b>SB</b>
Date:	Thursday, May 07, 2009	Sheet 21 of 52	

D



B

A

11

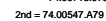
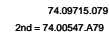
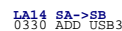
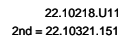
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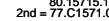
SB

1

Sheet 22 of 52
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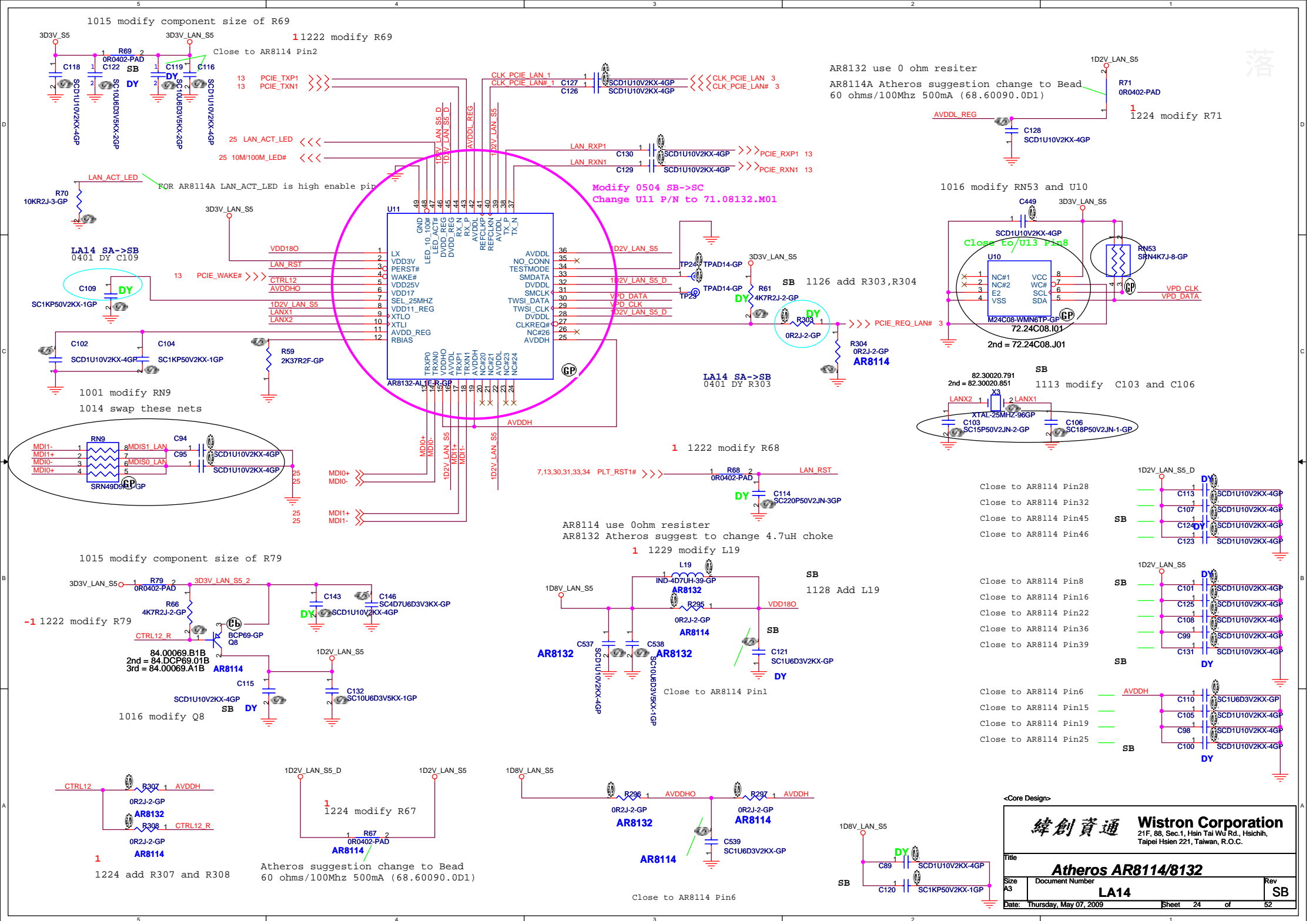
100 mil



緯創資通

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Title			
<b>USB</b>			
Size	Document Number		Rev
	<b>LA14</b>		S
Date: Thursday, May 07, 2009	Sheet	23 of	52





## PC BEEP GAIN CONTROL

Default gain is -6dB without populating the 10K-ohms pull-down resistors going to GPIO1 and GPIO2.

0912 add the part for EMI demand

GAIN	10K GPIO RESISTORS	
	R105	R106
0dB	Populate	Populate
-6dB	Omit	Omit
-12dB	Populate	Omit
-18dB	Omit	Populate

SB 1118 delete C245 and C270

0911 add net name(DVDD\_1\_8)

0911 add net name(ACZ\_SDATAIN0\_R)

12 ACZ\_RST#\_AUDIO >>>  
12 ACZ\_BITCLK\_AUDIO >>>  
12 ACZ\_SYNC\_AUDIO >>>  
12 ACZ\_SDATAIN0 >>>  
12 ACZ\_SDATAOUT\_AUDIO >>>

SB 1126 add C541 and modify R101

1M 0121 add R310

27 EAPD# <<<

CX20561

68.00119.081  
2nd = 68.00230.021

1001 Add R107

SB 1113 modify 2nd of U19

SB 1118 delete R107 and add L18

1113 modify 2nd of U19

1014 swap these nets

1014 modify these nets

0911 add net name(FLY\_P,FLY\_N,VREF\_LO,VREF\_HI)

1014 modify R258 from 10k to 20k ohm

<Core Design>

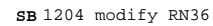
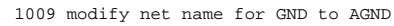
緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin,  
Taipei Hsien 221, Taiwan, R.O.C.

Title Azalia codec CX20561

Size A3 Document Number LA14 Rev SB

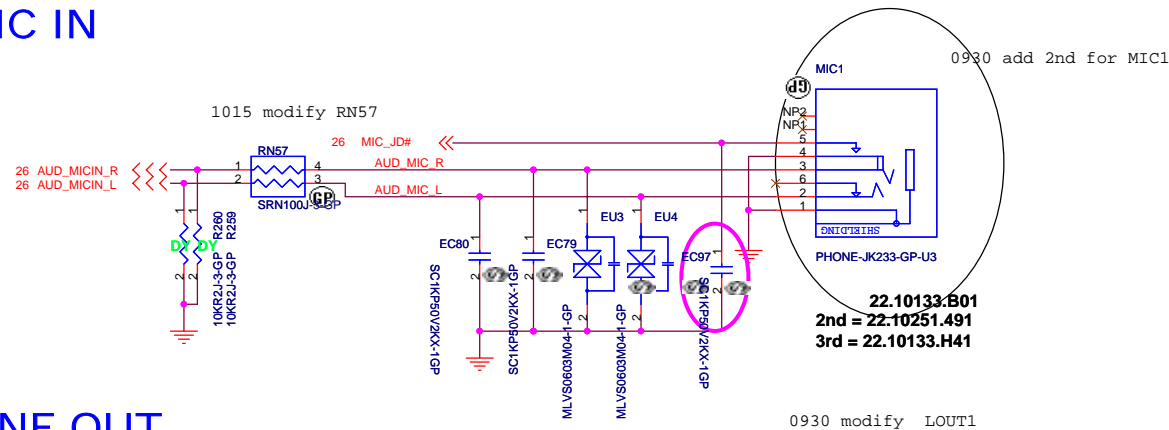
Date: Thursday, May 07, 2009 Sheet 26 of 52



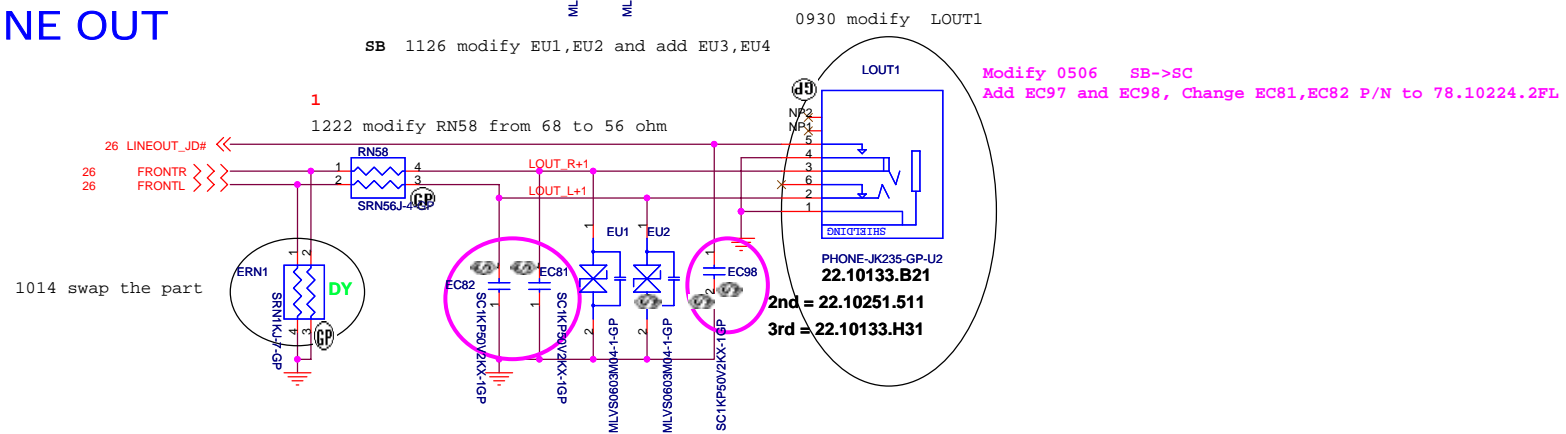


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Size	Document Number		Rev
	<b>LA14</b>		<b>SB</b>
Date:	Thursday, May 07, 2009		Sheet 27 of 52

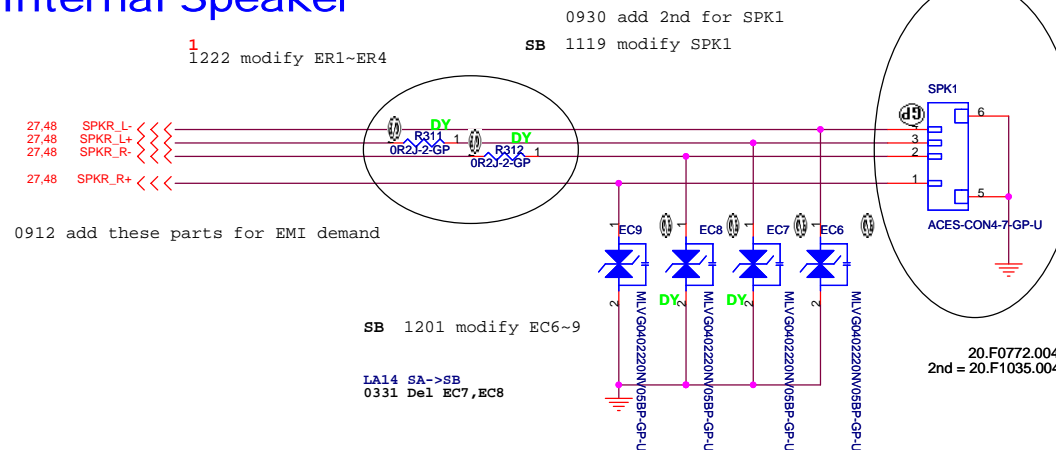
## MIC IN



## LINE OUT



## Internal Speaker



<Core Design>

緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title

**AUDIO JACK**

Size

Document Number

**LA14**

Rev

**SB**

Date: Thursday, May 07, 2009

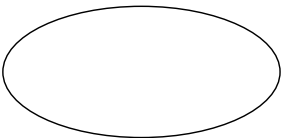
Sheet 28 of 52

# MDC 1.5 CONN

0912 add the part for EMI demand

1002 modify MDC1

**SB**  
1112 delete MDC function



<Core Design>

緯創資通

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21F, 88, Sec.1, Hsin Tai Wuj Rd., Hsichih,  
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Title

MDC

Size

Document Number

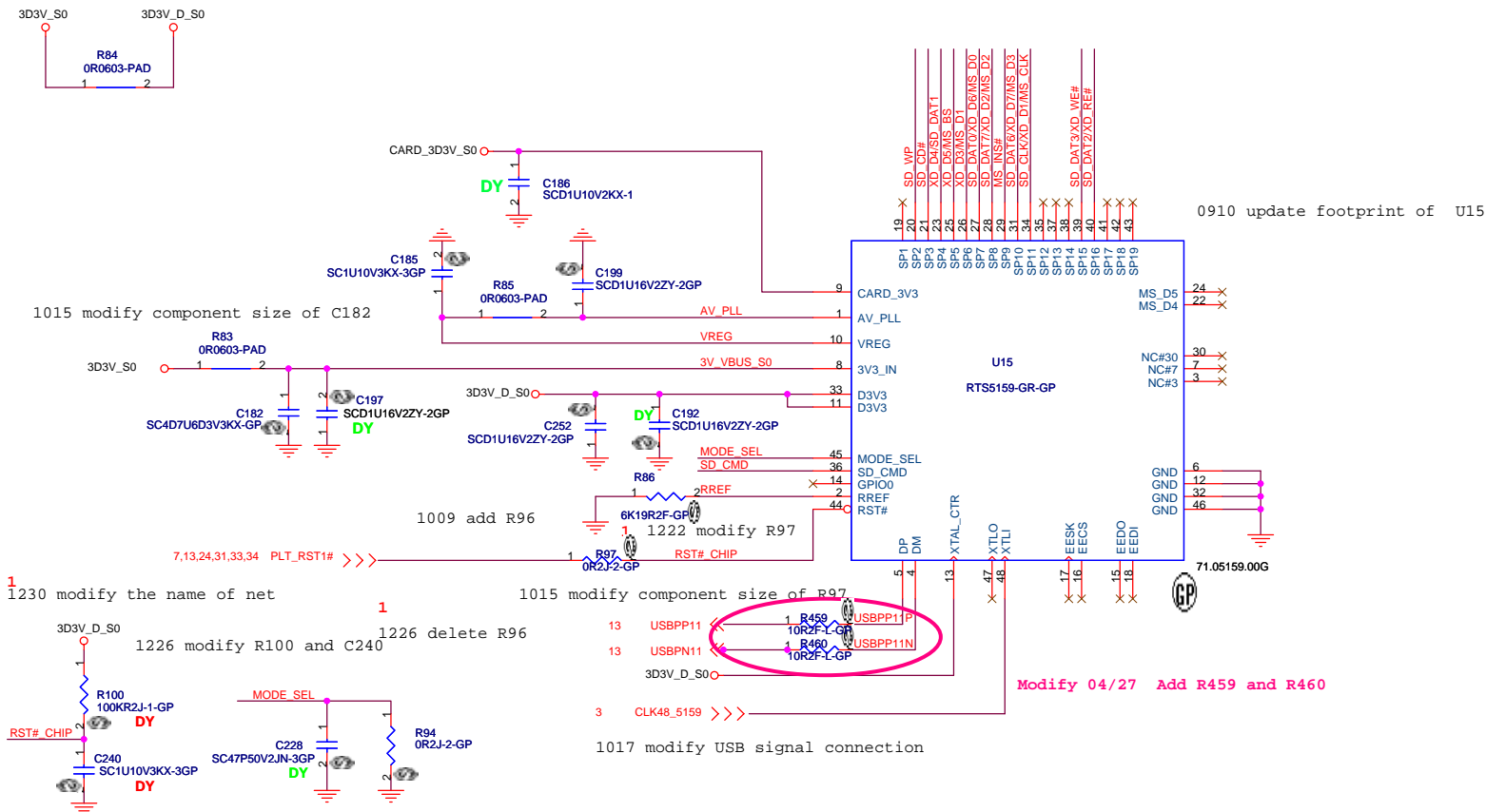
Rev

LA14

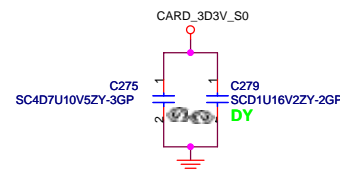
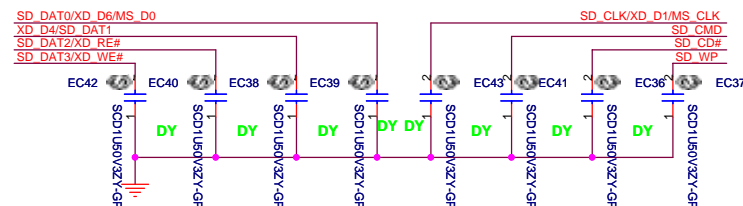
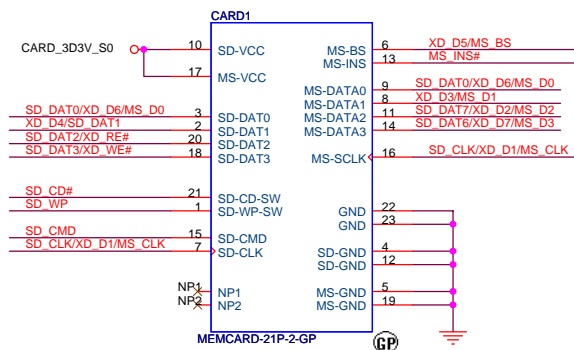
SB

Date: Thursday, May 07, 2009

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### 3 IN1 CARD-READER (SD/MMC/MS)



## <Core Design>

**緯創資通** **Wistron Corporation**  
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Taipei Hsien 221, Taiwan, R.O.C.

Title			
<b>CARD READER- RTS5159</b>			
Size	Document Number		Rev
	<b>LA14</b>		<b>S</b>
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1009 modify this net

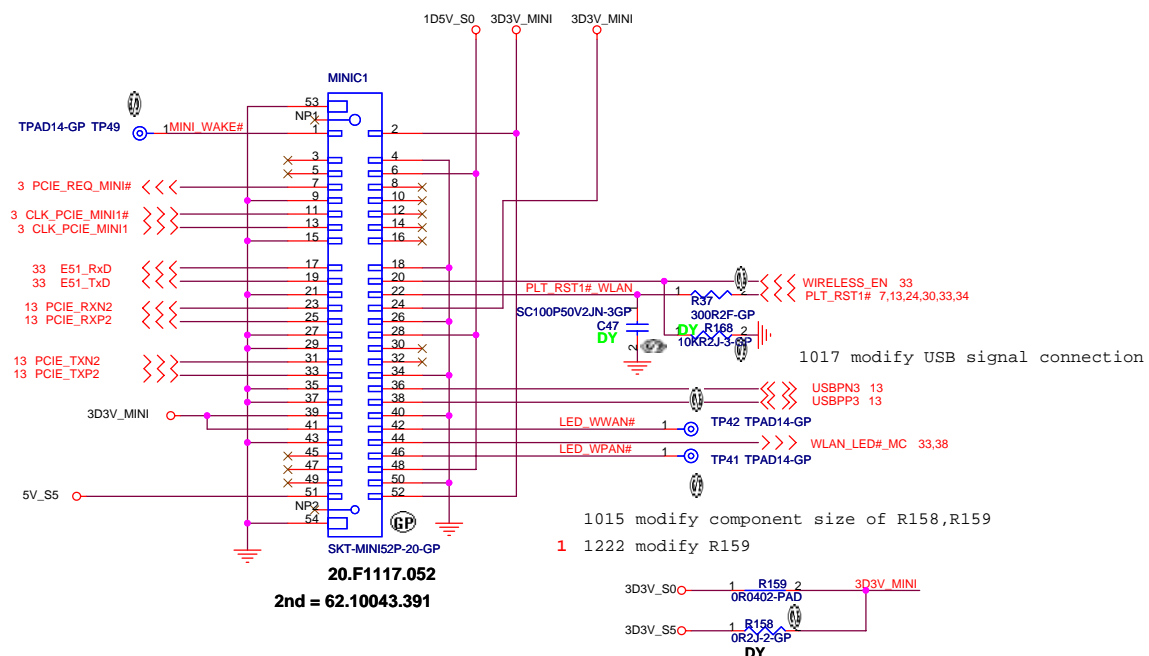
```
1013 modify card1
```

```
1 1222 modify card1 from 20.I0043.001 to 20.I0043.011
```

```
1 1229 modify card1
```

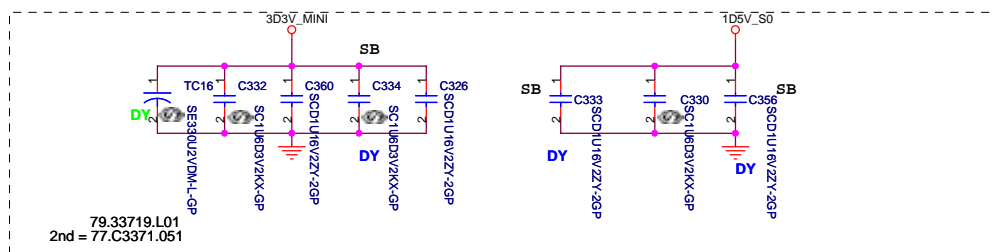
**LA14 SA** 0217 modify card1 from 20.I0043.011 to 20.I0033.021

# Mini Card Connector(WLAN)



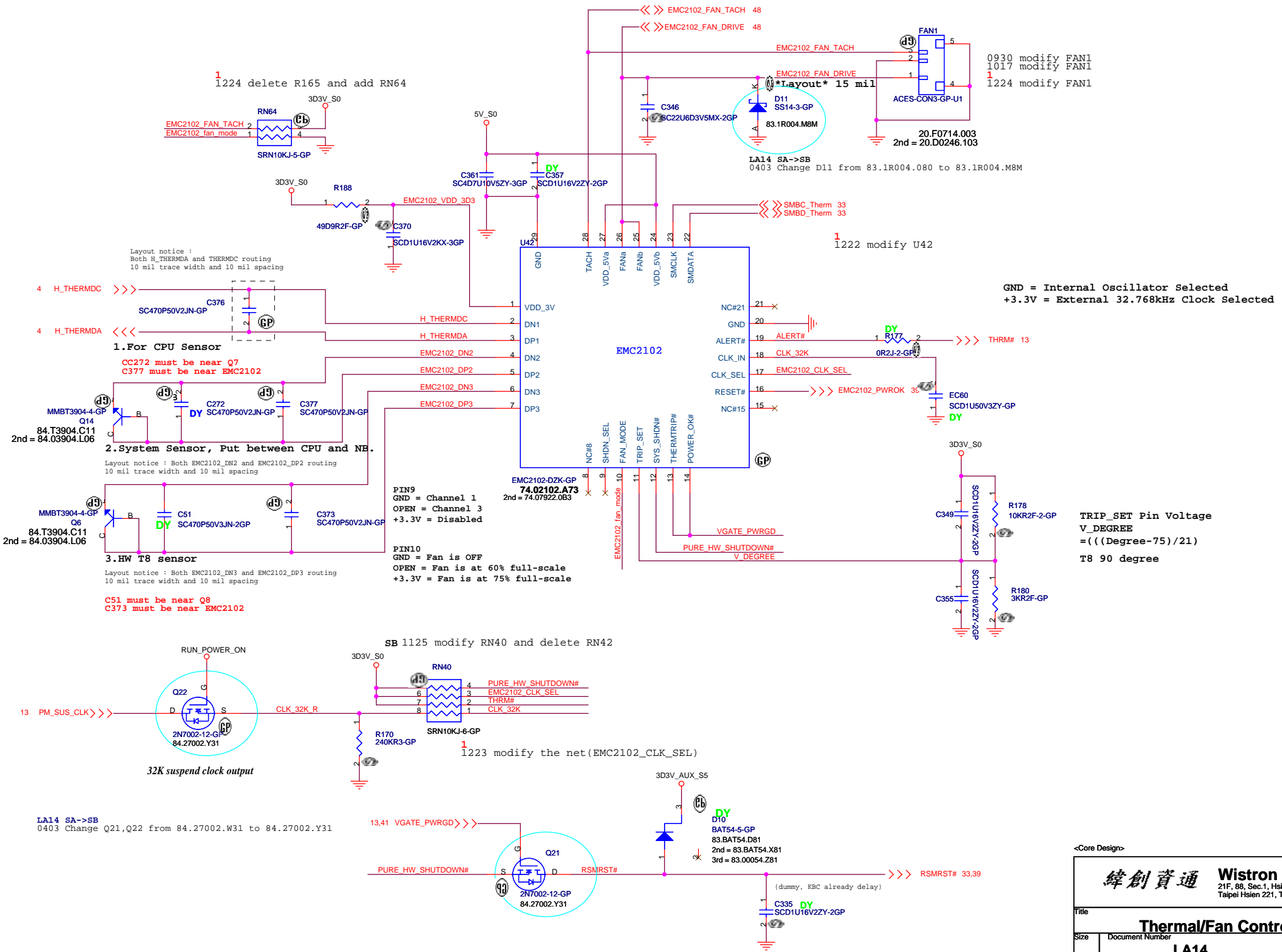
1021 modify TC16

Place near MINIC1



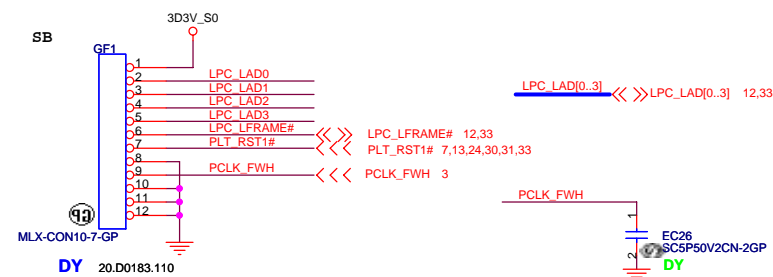
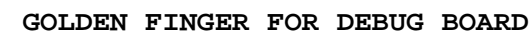
<Core Design>

<b>緯創資通</b>		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>MINI CARD</b>			
Size	Document Number	Rev	
	<b>LA14</b>	<b>SB</b>	
Date: Thursday, May 07, 2009	Sheet	31	of 52

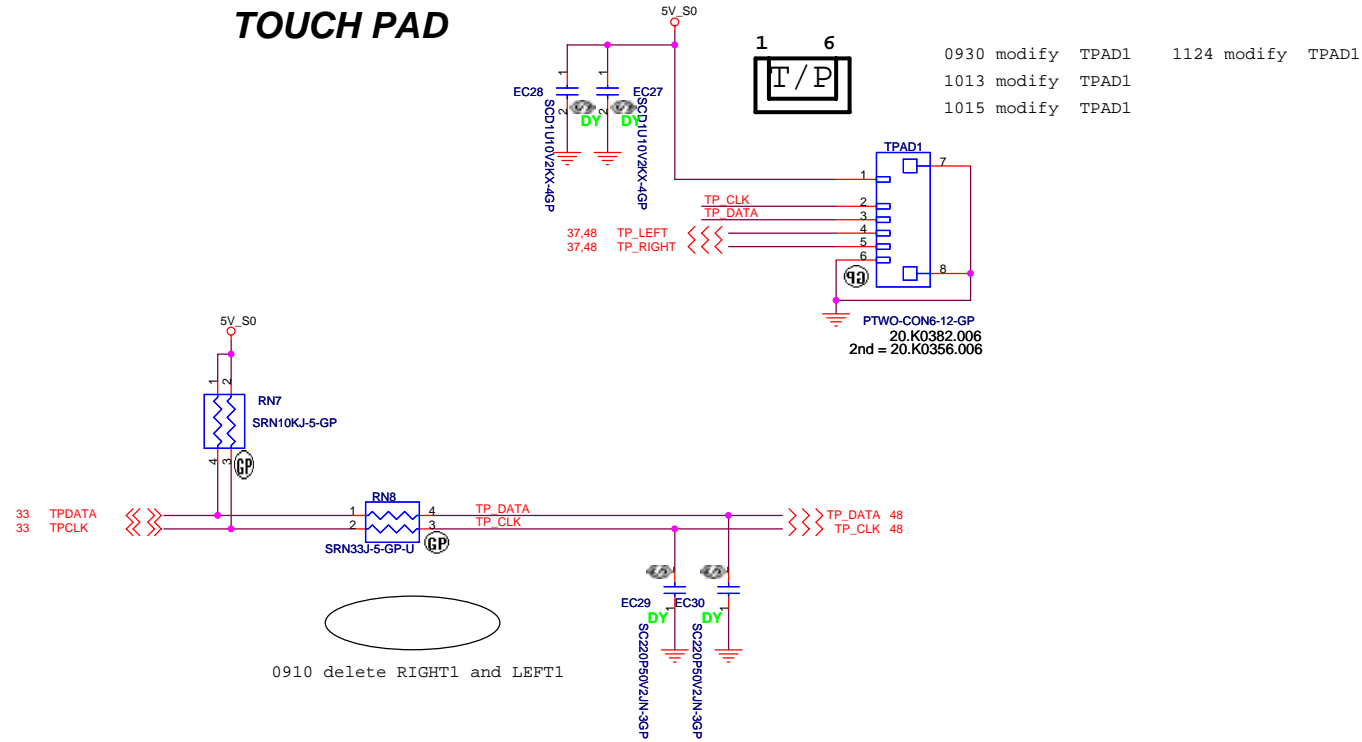








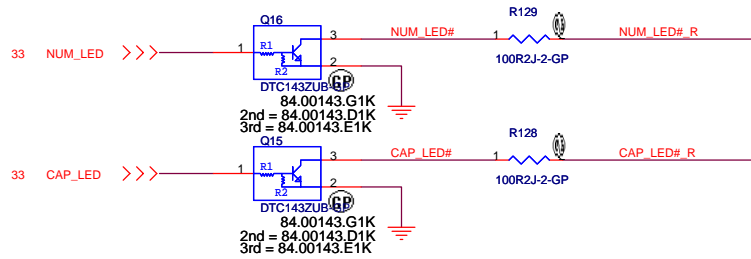
# TOUCH PAD



<Core Design>

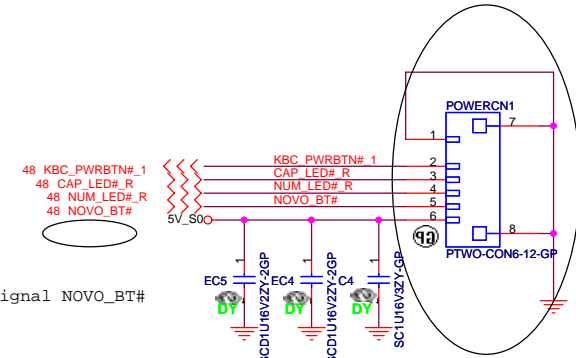
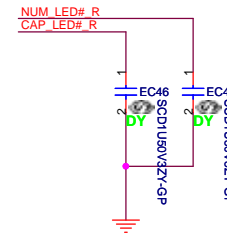
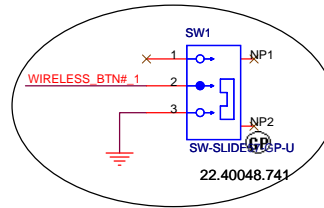
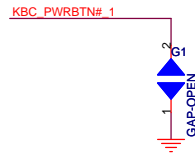
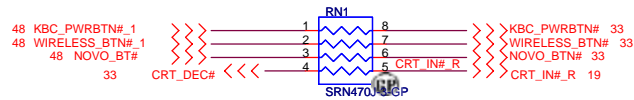
緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title			Touch pad
Size	Document Number	Rev	SB
	LA14		
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LA14\_SA

0205 remove signals(TP\_LOCK\_LED,TP\_LOCK\_LED#,TP\_LOCK\_LED#\_R)and R132,Q17



LA14\_SA

0205 ADD signal NOVO\_BT#

LA14\_SA

0205 modify POWERCN1 from 20.K0384.016 to 20.K0204.006

0223 modify POWERCN1 from 20.K0204.006 to 20.K0382.006

LA14\_SA  
0205 remove EC49

&lt;Core Design&gt;

緯創資通

Wistron Corporation

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Taipei Hsien 221, Taiwan, R.O.C.

Title

Power Board

Size

Document Number

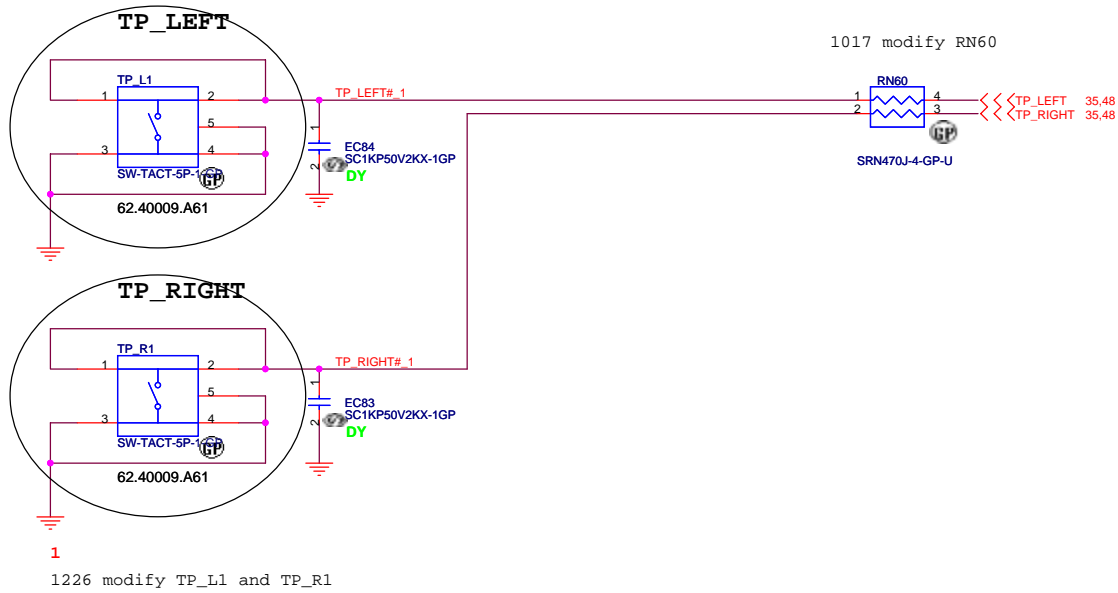
LA14

Rev

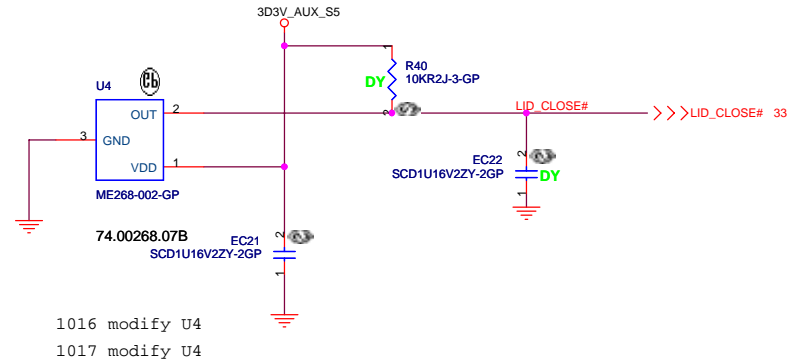
SB

Date: Thursday, May 07, 2009

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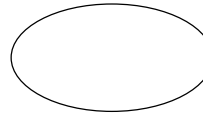


## Cover Up Switch



1017 add U61,R52,EC24 and EC23

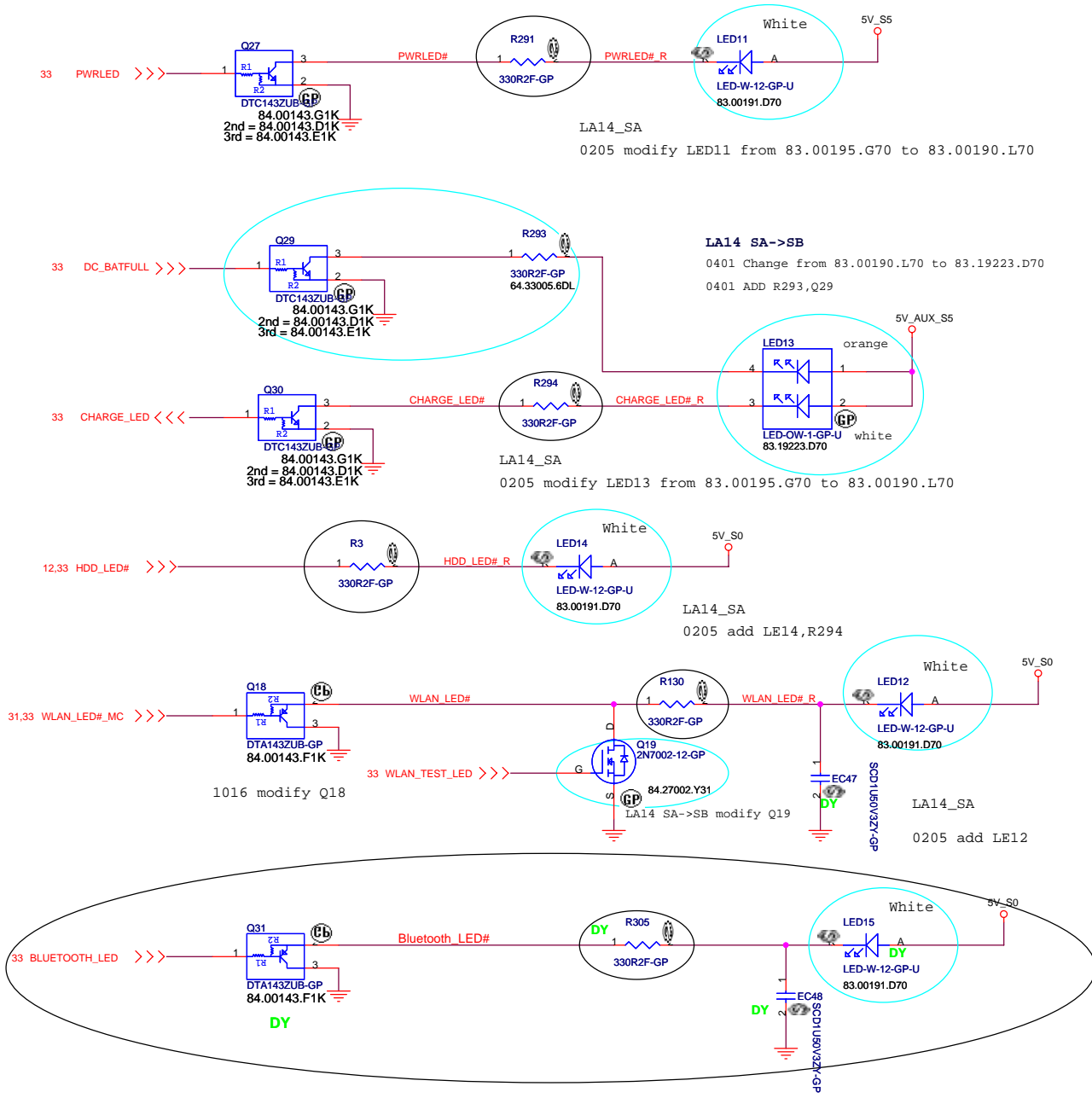
1020 delete U61,R52,EC24 and EC23



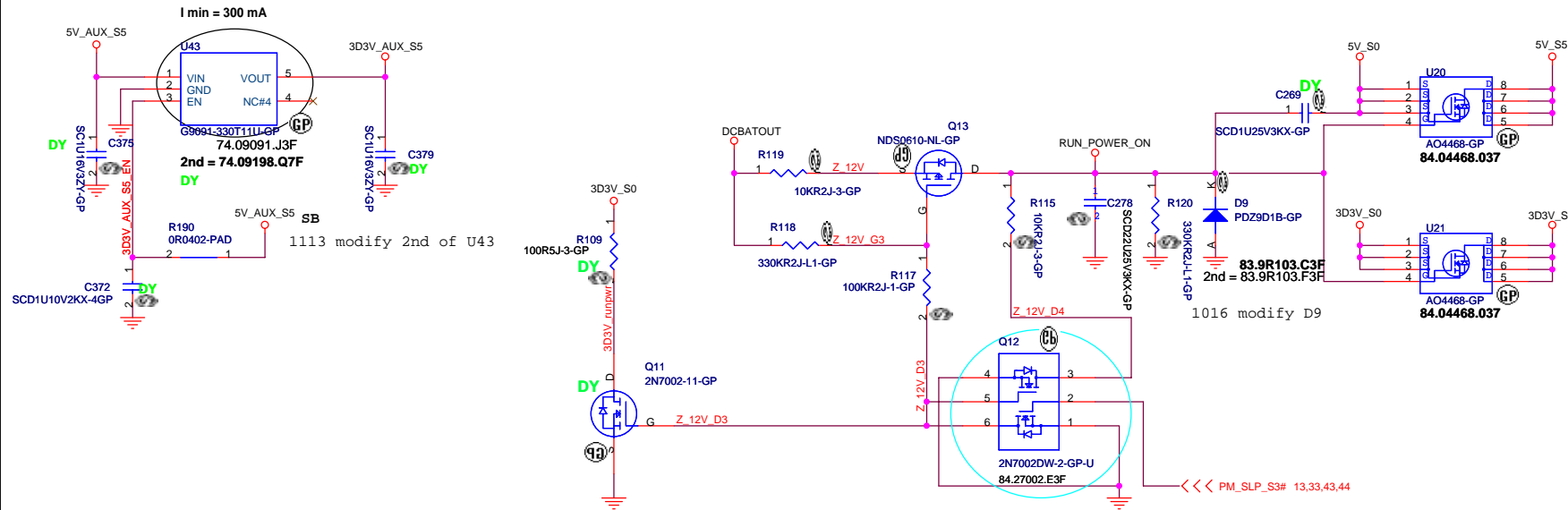
<Core Design>

緯創資通 Wistron Corporation  
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Taipei Hsien 221, Taiwan, R.O.C.

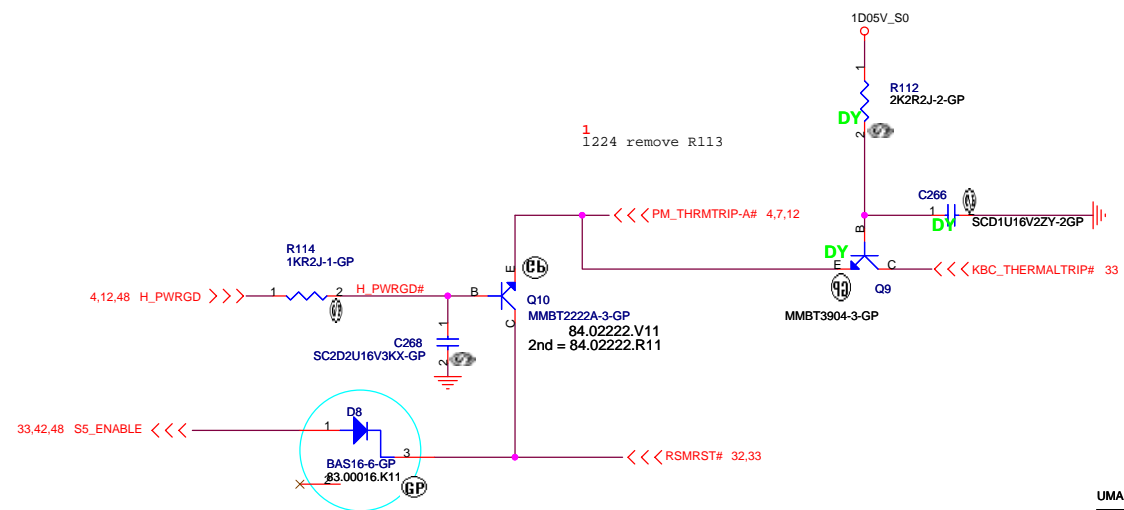
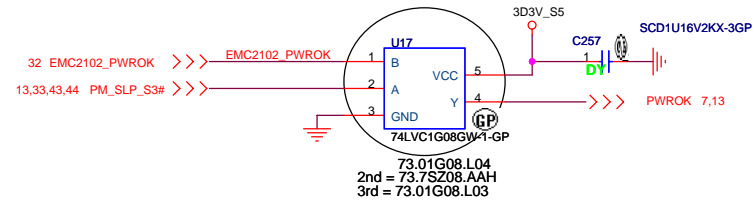
Title			SWITCHS	
Size	Document Number		LA14	Rev SB
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LA14\_SA  
 0205 modify LED11 from 83.00195.G70 to 83.00190.L70  
 LA14 SA->SB  
 0401 Change from 83.00190.L70 to 83.19223.D70  
 0401 ADD R293,Q29  
 LA14\_SA  
 0205 modify LED13 from 83.00195.G70 to 83.00190.L70  
 LA14\_SA  
 0205 add LE14,R294  
 1016 modify Q18  
 LA14 SA->SB modify Q19  
 LA14\_SA  
 0205 add LE12  
 LA14\_SA  
 0209 Change R305,R291,R294,R130,R3 from 29L2589AA to 64.33005.6DL  
 LA14 SA->SB  
 0331 Change LED11,LED12,LED14,LED15 from 83.19213.H70 to 83.00191.D70



LA14 SA->SB  
0403 Change Q12 from 84.27002.D3F to 84.27002.E3F

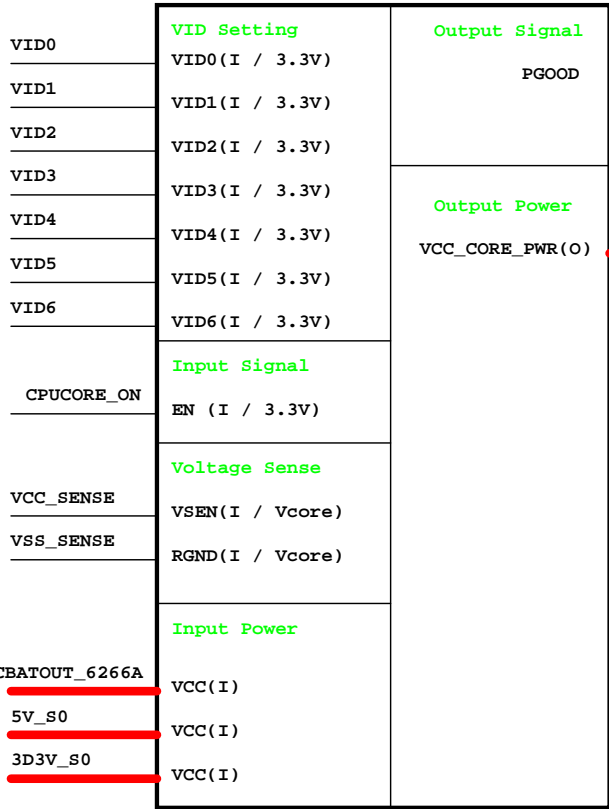


LA14 SA->SB  
0403 Change D8 from 83.00016.B11 to 83.00016.K11

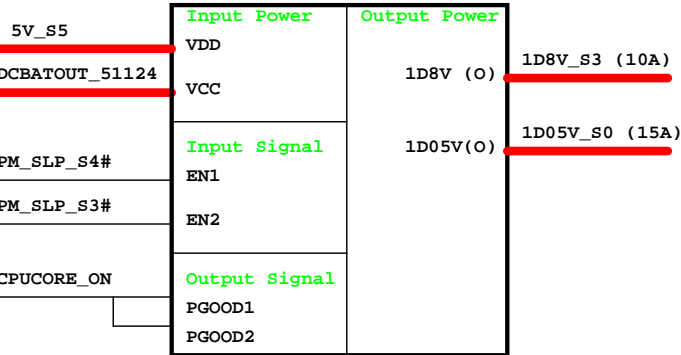
UMA Two Phase

<b>緯創資通 Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	<b>RUN POWER and 3D3V_AUX_S5</b>
Size	Document Number
Date:	Thursday, May 07, 2009
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Rev	SB

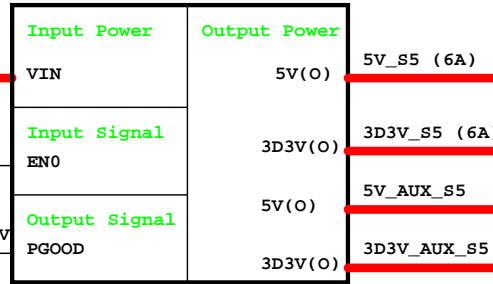
CPU\_CORE  
ISL6266A



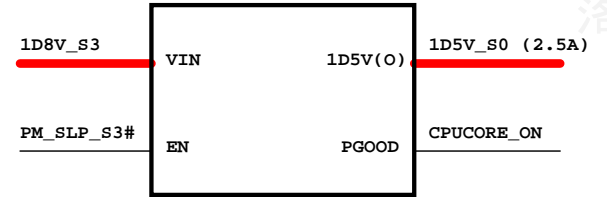
TPS51124  
1D8V/1D05V



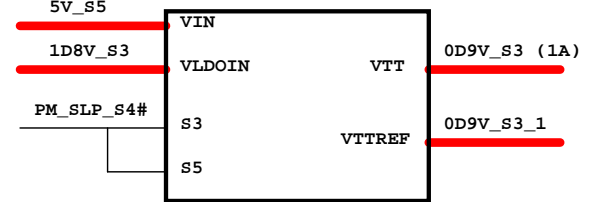
TPS51125  
5V/3D3V



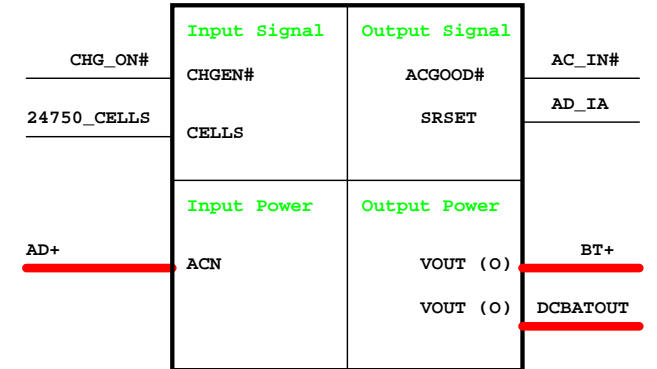
RT9018A  
1D5V\_S0



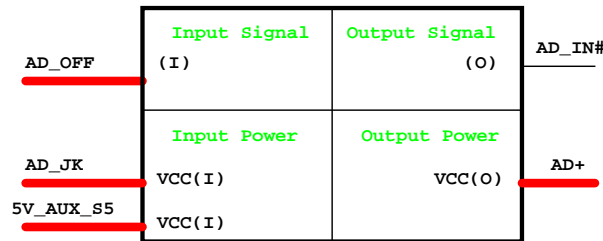
RT9026 0D9V\_S0



Charger BQ24745



Adapter



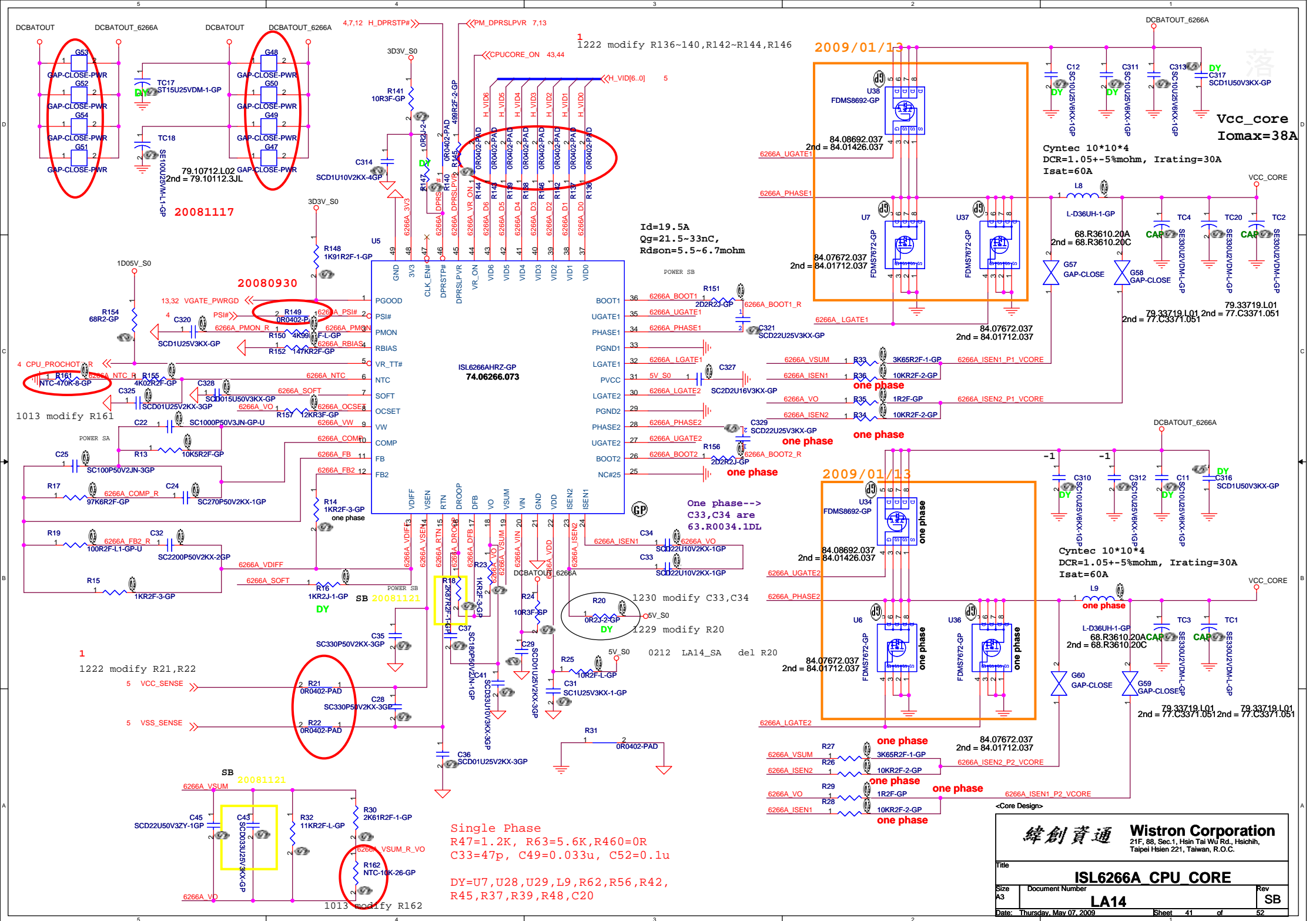
<Core Design>

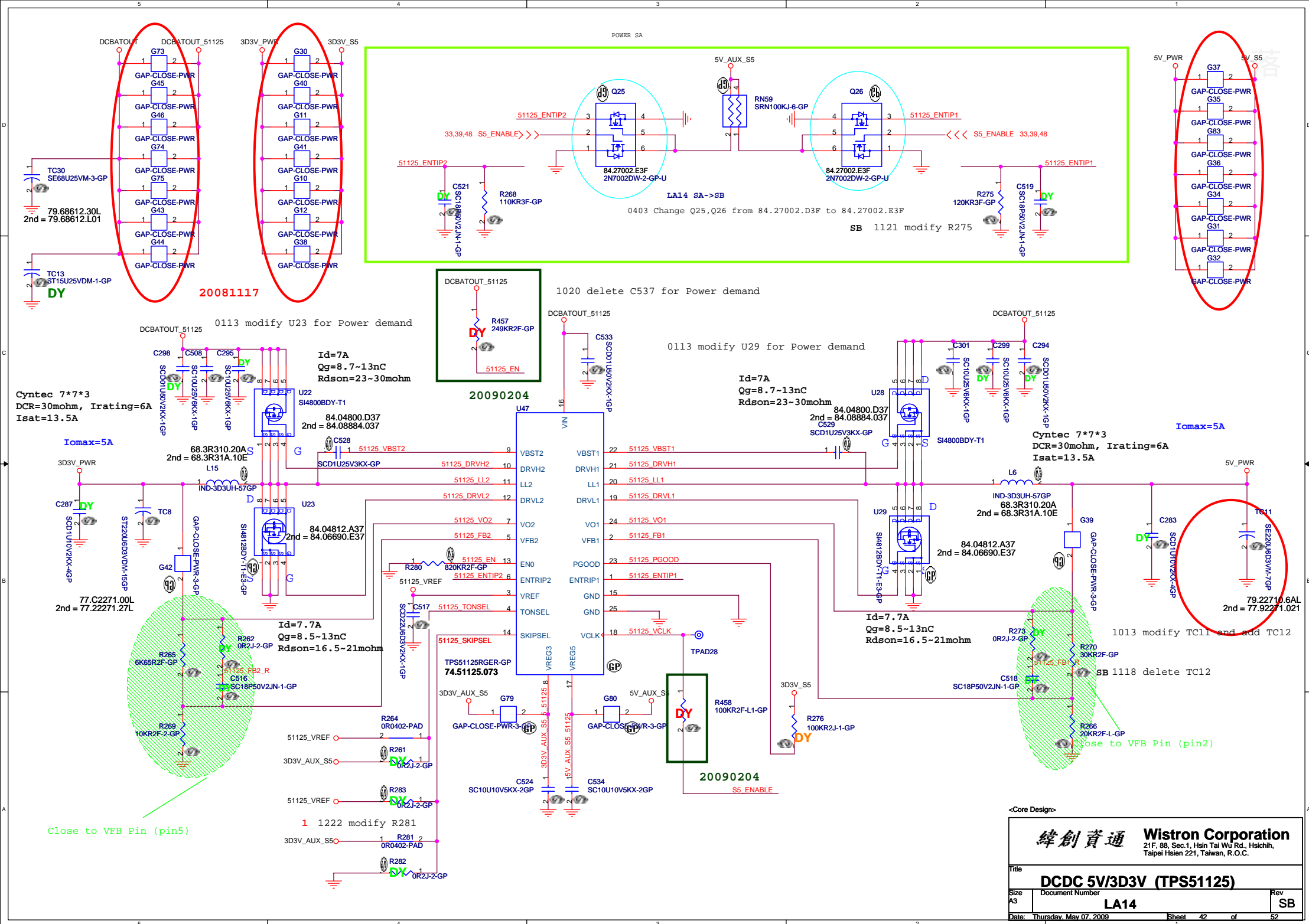
緯創資通

Wistron Corporation  
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Taipei Hsien 221, Taiwan, R.O.C.

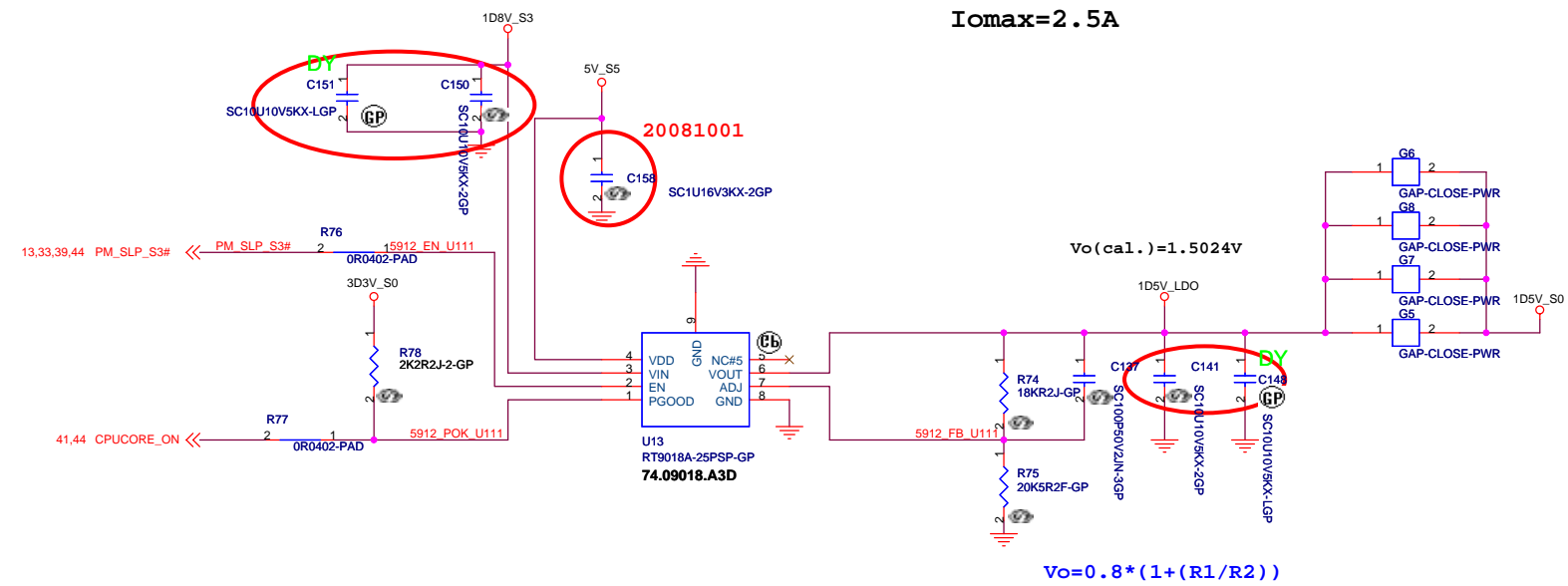
Title			Power Sequence Logic	
Size B	Document Number	LA14	Rev	SB
Date:	Thursday, May 07, 2009	Sheet 40	of	52





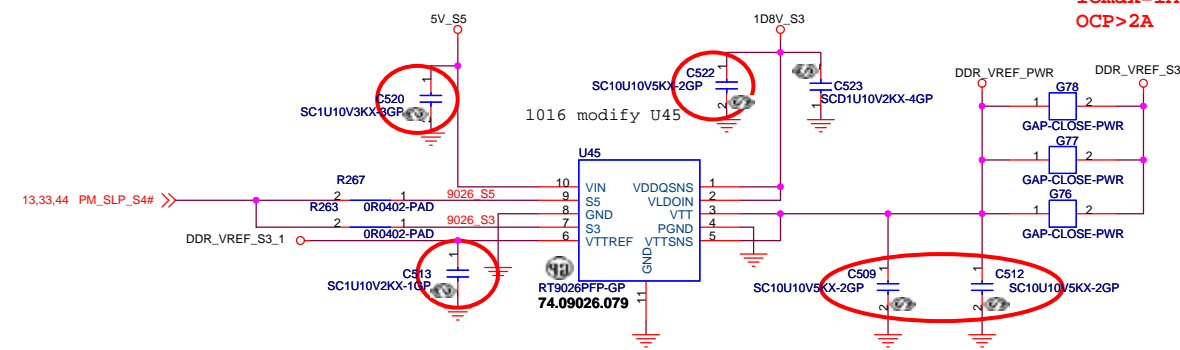


1D5V\_S0  
Iomax=2.5A



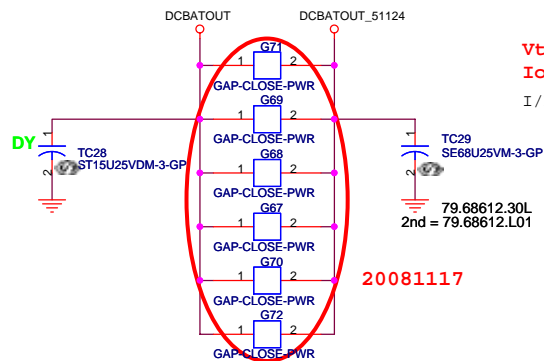
20081001

Iomax=1A  
OCP>2A



<Core Design>

<p>緯創資通 Wistron Corporation</p> <p>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</p>	
<p>Title</p> <p>1D5V &amp; 0D9V</p>	
Size	Document Number
A3	LA14
Date	Thursday, May 07, 2009
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Rev	SB

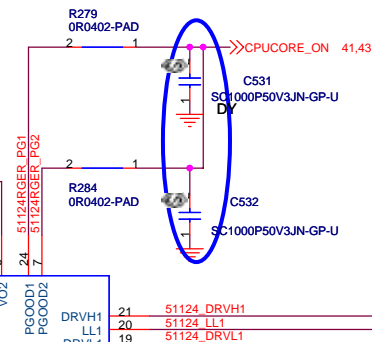


$$V_{trip}(mV) = R_{trip}(Kohm) * 10(uA)$$

$$I_{ocp} = (V_{trip}/R_{dson}) + ((1/(2*L*f)) * ((V_{in}-V_{out}) * V_{out}) / V_{in})$$

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L

1M  
0204 modify these symbol of C531 and C532  
2008/06/16

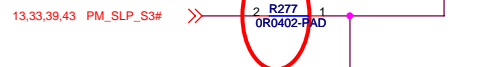
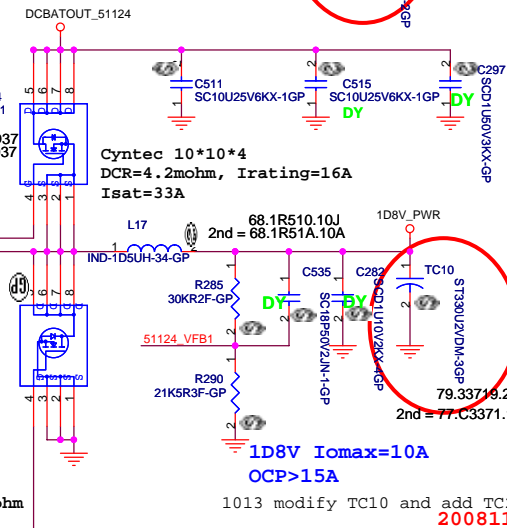


Id=7A  
Qg=8.7~13nC  
Rdson=23~30mohm

Id=7.7A  
Qg=8.5~13nC  
Rdson=16.5~21mohm

SB 1128 add TC26

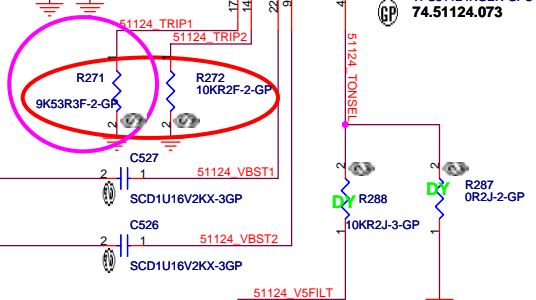
79.3971V.6AL  
2nd = 79.3971V.E0L



1222 modify R277, R278

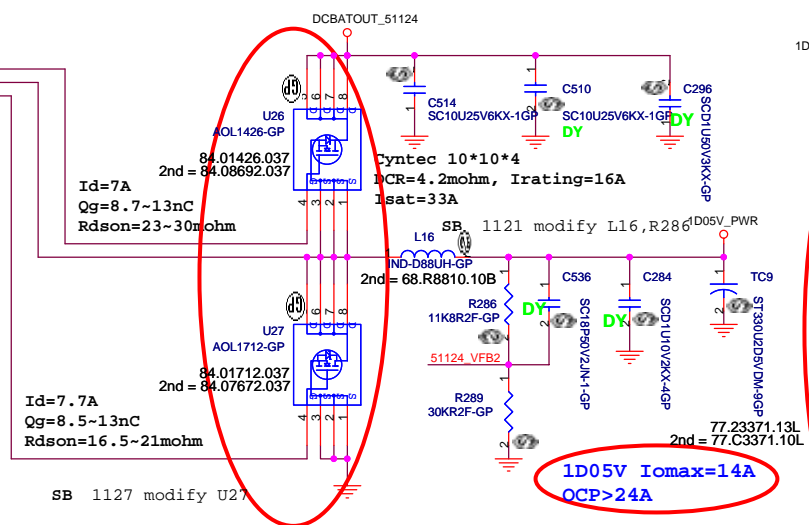
SB 1121 modify R271, R272

Modify 0429 R271 change to 64.95315.55L



	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

Vout=0.758V\*(R1+R2)/R2 --> PWM mode  
Vout=0.764V\*(R1+R2)/R2 --> Skip Mode



<Core Design>

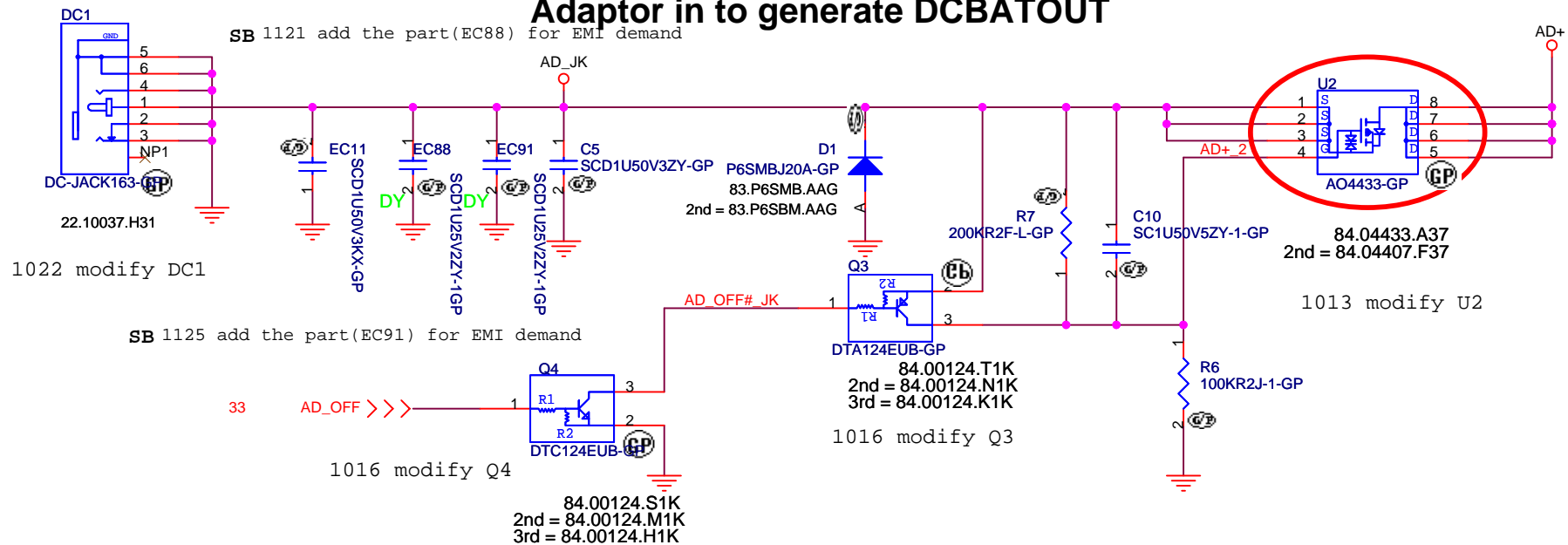
緯創資通

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TPS51124 1D8V 1D05V			
Size	Document Number	Rev	SB
A3	LA14		
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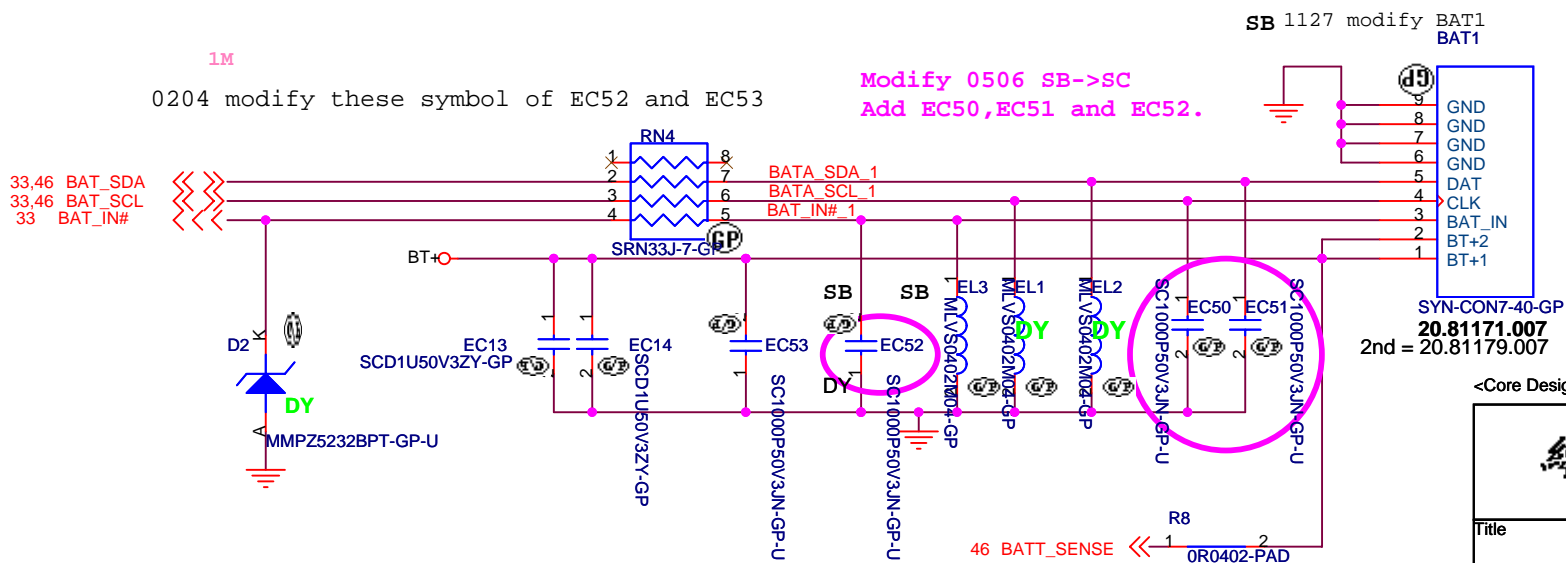
# Adaptor in to generate DCBATOUT



LA\_SA 0216 Change DC1 from 22.10037.F11 to 22.10037.H31

BATA\_SDA\_1 48  
BATA\_SCL\_1 48  
BAT\_IN#\_1 48

## BATTERY CONNECTOR



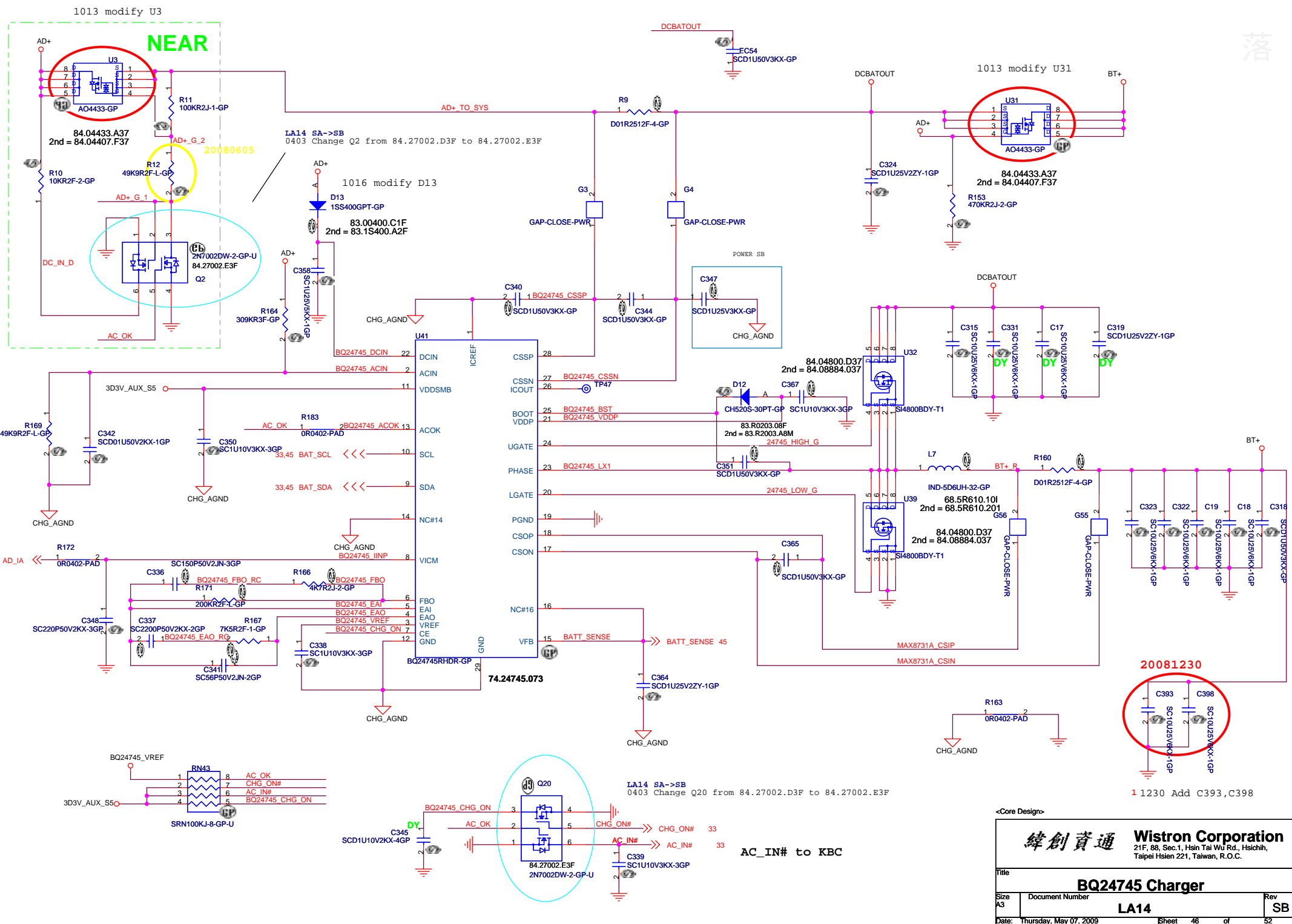
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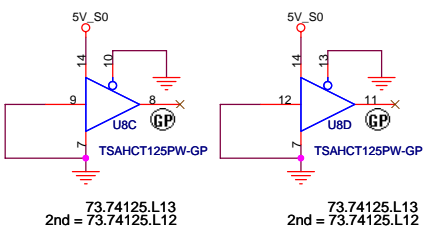
緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

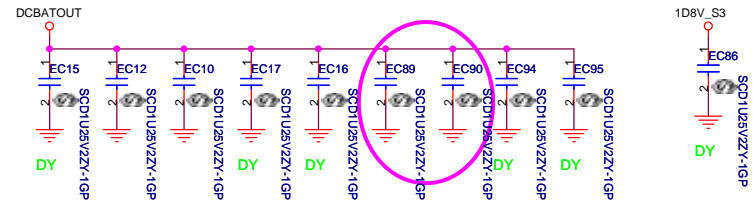
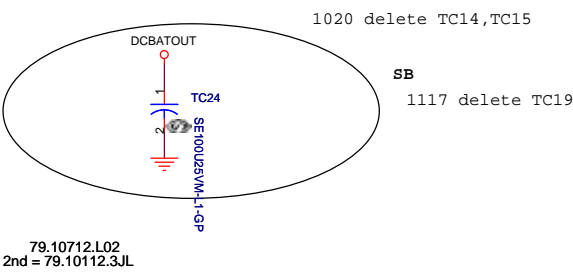
Title			
AD/BATT CONN			
Size	Document Number		Rev
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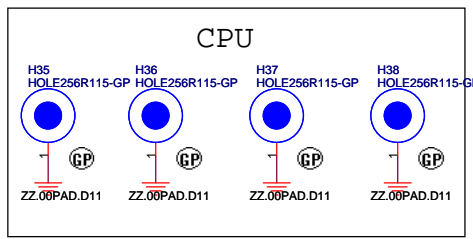
1016 modify U32

- 1017 add these parts(EC10,EC12,EC15~EC17,EC86) for EMI demand
- 1020 add the part(EC86) for EMI demand      1125 add the part(EC90) for EMI demand
- SB 1121 add the part(EC89) for EMI demand      1128 add EC94,EC95 for EMI demand

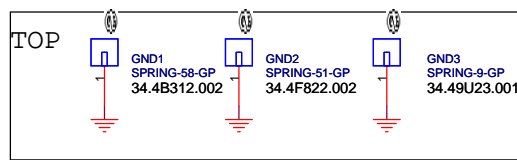


Modify 0506 SB->SC  
Add EC89 and EC90 for EMI demand

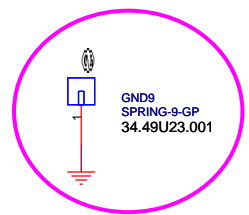
- 1016 add GND1 and GND2 for EMI demand
- 1017 add GND3 and modify GND2 for EMI demand



- 1016 modify H35~H38
- 1016 delete H9~H12



SB 1128 Add GND4,GND7,GND8



Modify 0506 SB->SC  
Add GND9 for EMI demand

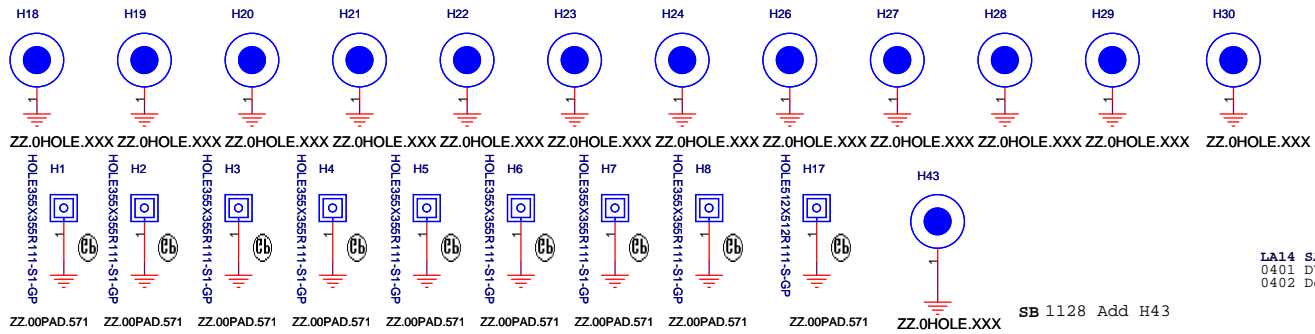
LA14 SB 0402 modify H35~H36

1016 modify H31 and H32

SB 1120 remove H31and H32

1 1230 Add GND9

LA\_SA 0218 Change H35~H38 from ZZ.00PAD.571 to ZZ.00PAD.801



SB 1128 Add H43

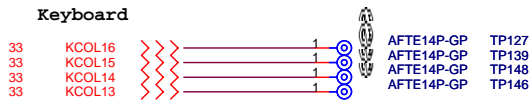
LA14 SA->SB  
0401 DY H8  
0402 Del H8

<Core Design>

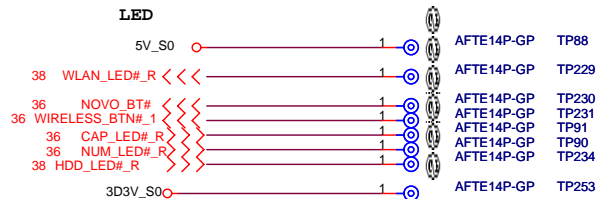
**緯創資通**      **Wistron Corporation**  
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Taipei Hsien 221, Taiwan, R.O.C.

Title		EMI/Spring/Boss	
Size	Document Number	Rev	
LA14		SB	
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1017 modify USB signal connection



**SB**

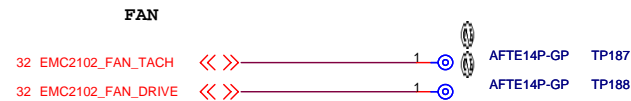
1112 remove the signal( STDBY\_LED#\_R)



## Check test point



Test Point放在Dimm Door打開可量測處



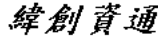
<Core Design>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
AFTE test point			
Size	Document Number		Rev
	LA14		SB
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0910 delete F4(Page 18)  
0910 update footprint of U15(Page 30)  
0910 delete RIGHT1 and LEFT1(Page 33)  
0910 modify net names of TP\_LEFT and TP\_RIGHT(Page 36)  
0910 modify test points of AFTE and TPAD  
0911 modify net name from LPC\_RST to PLT\_RST1#(Page 24)  
0911 add net name(RBIAS,LED\_DUPLEX#,SMDATA,SMCLK)(Page 24)  
0911 add net name(DVDD\_1\_8,ACZ\_SDATAIN0\_R,FLY\_P,FLY\_N,VREF\_LO,VREF\_HI)(Page 26)  
0911 add net name(EAPD#\_R)(Page 27)  
0912 modify the schematic of Page 33  
0912 delete GMCH\_TXB\*(Page 7& 18)  
0912 add these parts for EMI demand(page 7,18,20,21,23,26,28,29,30,32,33,34,35)  
0915 modify net name from 10M/100M/1G\_LED# to 10M/100M\_LED#(page24,25)  
0915 delete these parts for EMI demand(page 30)  
0915 add EC34 for EMI demand(page3)  
0915 add EC73 for EMI demand(page 12)  
0915 modify LEDs port  
0916 move net(SPI\_WP#) from U9 pin120 to pin25(page33)  
0930 modify BLUE1(page22)  
0930 add 2nd for SPK1, MIC1 and modify LOUT1 (page28)  
0930 modify FAN1(page32)  
0930 modify TPAD1(page35)  
0930 modify KB1(page33)  
0930 modify net name for BIOS demand(page33)  
1001 delete these parts for EMI demand(ED1~8)  
1009 modify net name for GND to AGND(page27)  
1009 add R4,R5 for AC decoupling(page27)  
1009 add R96(page30)  
1013 modify TPAD1(page35)  
1013 modify U40 from 72.25X16.001 to 72.25X16.A01(page 34)  
1013 modify TC11 and add TC12(page42)  
1013 modify TC10 and add TC26(page44)  
1013 modify U2(page45)  
1013 modify U3 and U31(page 46)  
1013 modify R161 and R162(page41)  
1013 modify card1(page 30)  
1014 modify these LEDs(LED11,LED12)(page38)  
1014 modify these nets(page 26)  
1014 modify R258 from 10k to 20k ohm(page26)  
1014 add ER5 for EMI deamnd(page3)  
1015 modify LCD1 pin define(page 18)  
1015 modify the power from 3D3V\_S5 to 5V\_S5(page38)  
1015 modify TPAD1(page35)  
1015 modify RN57(page28)  
1015 modify F1(page18)

<Core Design>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Change List			
Size	Document Number		Rev
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Date: Thursday, May 07, 2009		Sheet 49 of	52

1016 modify L1,L2 and L3(page 19)  
1016 modify XF1(page 25)  
1016 modify RN53 and U10(page 24)  
1016 modify U8(page19,47)  
1016 modify U4(page 37)  
1016 modify U23(page 43)  
1016 modify X2(page12)  
1016 modify X1(page 33)  
1016 modify X3(page 3)  
1016 modify D13(page 46)  
1016 modify D23(page 20)  
1016 modify D9(page 39)  
1016 modify D4(page 19)  
1016 modify Q3 and Q4(page45)  
1016 modify Q18(page 36)  
1016 modify Q15~Q17(page 36)  
1016 modify Q27~Q30(page38)  
1016 modify Q6 and Q14(page 32)  
1016 modify Q8(PAGE 24)  
1016 add GND1 nad GND2 for EMI demand(page 47)  
1016 modify LCD1 pin define(page 18)  
1016 delete H9~H12 and modify H35~H38,H31,H32(page 47)  
1017 add these parts for EMI demand(page 47)  
1017 delete these parts(EC208~EC210)(page 7)  
1017 modify BLUE1(page 22)  
1017 modify FAN1(page 32)  
1017 modify R291 and R293(page 38)  
1017 add U61,R52,EC23 and EC24(page 37)  
1017 modify RN60(page37)  
1017 add TC25(page 44)  
1017 add GND3 and modify GND2 for EMI demand(page 47)  
1017 modify USB signal connection(page13,18,22,23,30,31,48)  
1020 delete C537 for Power demand(page42)  
1020 add the part(EC86) for EMI demand(page 47)  
1020 delete U61,R52,EC24 and EC23(page 37)  
1020 delete TC14,TC15(page 47)  
1021 modify TC16(page 31)  
1021 delete TC23(page 23)  
1021 modify TC5(page 20)  
1021 modify and swap these parts(USB1 and USB2)(page 23)  
1021 modify SATA1(page 20)  
1022 modify DC1(page 45)

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SB to 1

1222 modify U42 for customer demand(page32)

1222 modify these names of nets (BMC2102\_DN2,DP2,DN3,DP3,PWROK,FAN\_TACH,FAN\_DRIVE) (page32)

1222 modify RN58 from 68 to 56 ohm for customer demand(page28)

1222 modify PCB Ver. from SB to -1(page33)

1222 modify TC5 for HDD side(page20)

1222 modify card1 from 20.I0043.001 to 20.I0043.011for CE demand(PAGE30)

1223 modify the net(EMC2102\_CLK\_SEL) for reducing component (page32)

1223 modify the net(RSMRST#) for reducing component(page33)

1224 dummy C6(page27)

1224 add R306 for FSB Dynamic ODT(dummy) (page7)

1224 add R307 and R308 for LAN co-layout demand(page24)

1224 modify FAN1for CE demand(page32)

1224 remove R113 for reducing component (page39)

1224 modify RN54 for reducing component (page12)

1224 modify R191,RN48 and this net AD\_OFF for reducing component (page33)

1224 modify D5(dummy) (page20)

1224 delete R165 and add RN64 for reducing component (page32)

1226 modify TP\_L1 and TP\_R1 for ME demand(page37)

1226 modify R100 and C240(dummy) (page30)

1226 delete R96 for reducing component (page30)

1229 modify C76,C77 from 12pF to 15pF for vender demand(page12)

1229 modify L19 for vender demand(page24)

1229 modify U30 for cost down(page18)

1229 modify U44 for cost down(page10)

1229 modify R20 for power team demand(page41)

1230 modify the name of net(RST#\_CHIP)(beacuse R97 was removed)(page30)

1230 modify ODD1 for CE demand(page21)

1230 modify C33,C34 for power team demand (page41)

1230 modify D14 for CE demand(page33)

1230 Add C393,C398 for power team demand(page46)

1230 Add GND9 for EMI demand(page47)

1230 dummy C507(page26)

1230 delete Q1 and modify U1 for new AMP IC(page27)

1230 delete RN35 and add R309(page27)

1231 modify R80 for clock gen voltage(3.3V to 1.05V) (page3)

1231 modify ODD1 for ME demand(page21)

0105 modify R3,R128,R129,R130,R132 and R133 for LED brightness conrtol(page36)

0105 modify R291,R292,R293 and R294 for LED brightness conrtol (page38)

0105 modify L1,L2 and L3 for EMI demand(page19)

0112 modify TC10(page44)

0113 modify ODD1 for ME demand(page21)

0113 modify U34,U38,U6,U7,U36 and U37 for power demand(page41)

0113 modify U23 and U29 for power demand(page42)

0113 modify U25,U27,TC10 and L16 for power demand(page44)

1 to 1M

0121 modify PCB Ver. from 1 to 1M(page33)

0121 add R310(page26)

0204 add R457,R458 for power demand(co-layout) (page42)

0204 modify R130,R132 and R133 for LED brightness conrtol(page36)

0204 modify KB1 for CE demand(add mylar) (page33)

0204 modify the symbol of C22 (page41)

0204 modify these symbol of C531and C532 (page44)

0204 modify these symbol of EC52 and EC53 (page45)

0204 modify the symbol of EC74 (page23)

0 ohm to short pad

1222 modify R277,R278(page44)

1222 modify R135,R5(page27)

1222 modify R58(page25)

1222 modify R136~140,R142~R144,R146,R149(page41)

1222 modify R21,R22(page41)

1222 modify R80,R87(page3)

1222 modify R252(page10)

1222 modify R209(page13)

1222 modify R68,R69,R79(page24)

1222 modify R97(page30)

1222 modify R159(page31)

1222 modify R189(page33)

1222 modify R281(page42)

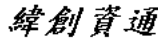
1222 modify ER1~ER4(page28)

1224 modify R91(page3)

1224 modify R67,R71(page24)

1224 modify ERN2(page34)

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