Compal Confidential

VALEA/VALEB Schematics Document

AMD APU Richland FS1r2 + FCH Bolton-M3 + GPU Sun Pro M2

2012-11-22

REV:1.0

Security Classification	Compal Secret Data		
Issued Date	2012/11/22	Deciphered Date	2015/11/22

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Title: Cover Page

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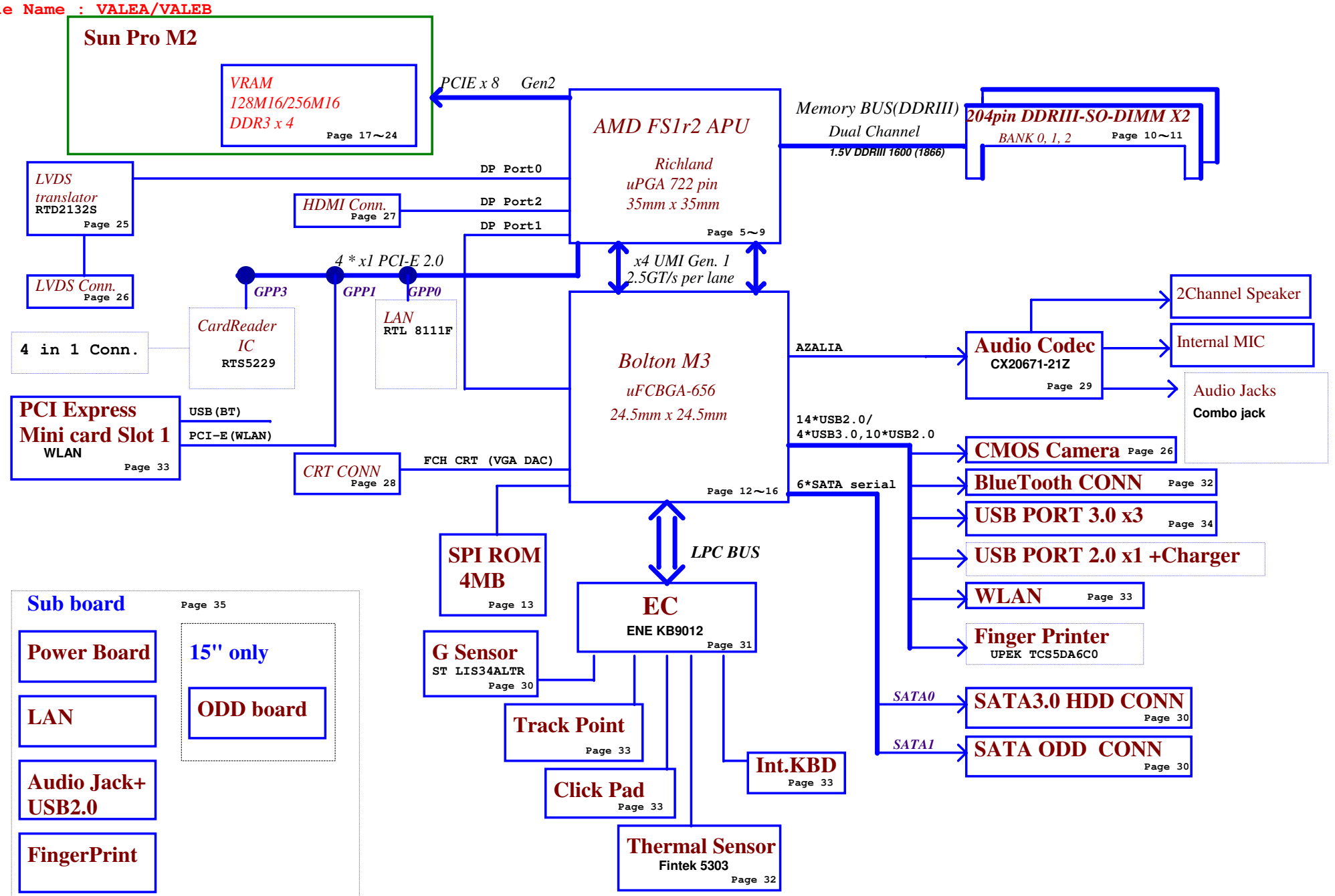
File Name : VALEA/VALEB



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Title: Block Diagrams

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Voltage Rails

Power Plane	Description	S0	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+APU_CORE	Core voltage for APU	ON	OFF	OFF
+APU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+1.5V	1.5V power rail for APU VDDIO and DDR	ON	ON	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+1.2VS	1.2V (VDDR, VDDP) switched power rail for APU	ON	OFF	OFF
+2.5VS	2.5V for APU VDDA	ON	OFF	OFF
+1.1VALW	1.1V switched power rail for FCH	ON	ON	ON*
+1.1VS	1.1V switched power rail for FCH	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+1.5VGS	1.5V switched power rail	ON	OFF	OFF
+1.8VGS	1.8V switched power rail	ON	OFF	OFF
+0.95VGS	0.95V switched power rail for VGA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS_WLAN	3.3V power rail for WLAN	ON	OFF	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

FCH Hudson-M2/3 SATA Port List

SATA0	HDD
SATA1	ODD
SATA2	NC
SATA3	NC
SATA4	NC
SATA5	NC

Comal PCIE Port List

APU	PCIE0	LAN
	PCIE1	WLAN
	PCIE2	NC
	PCIE3	Card Reader
FCH	PCIE0	NC
	PCIE1	NC
	PCIE2	NC
	PCIE3	NC

FCH Hudson-M2/3 USB Port List

USB1.1	
Port0	NC
Port1	NC
USB2.0	
Port0	USB2.0 Port
Port1	NC
Port2	NC
Port3	NC
Port4	NC
Port5	WLAN
Port6	CMOS
Port7	FP
Port8	BT
Port9	NC
Port10	USB 3.0
Port11	USB 3.0
Port12	USB 3.0
Port13	NC

EC SM Bus1 address

Device	Address	HEX
Smart Battery	0001-011xb	15H

EC SM Bus2 address

Device	Address	HEX
F75303 (DDR,VRAM,CPUCORE)	1001-101xb	9AH
SB-TSI	1001-100xb	98H
Sun Pro M2	1000-0010b	82H
LVDS translator		

FCH SMB0

(FCH_SMB0)

Device	Address	HEX
DDR DIMM1 (FCH_SMB0)	1001-000xb	90
DDR DIMM2 (FCH_SMB0)	1001-001xb	92
WLAN (FCH_SMB0)		
Security ROM		

Stencil Memo

BOM Structure

UMA@ : UMA only
DIS@ : DIS muxless

CMOS@ : USB camera

CONN@ : ME components
X76@, H1G@, S1G@ : VRAM

BOM option and stencil

SDV:
CMOS@/DIS@ + X76@

PJ201,PJ401,PJ502,PJ503,PJ504,PJ601,PJ603,PJ604,
PJ701,PJ702,PJ703,PJ704,J1,J2301,J2401,J2402,J2403
PJ402,PJ403,PJ501,PJ602,PJ801,PJ802,PJ803,PJ805

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Title: Notes List

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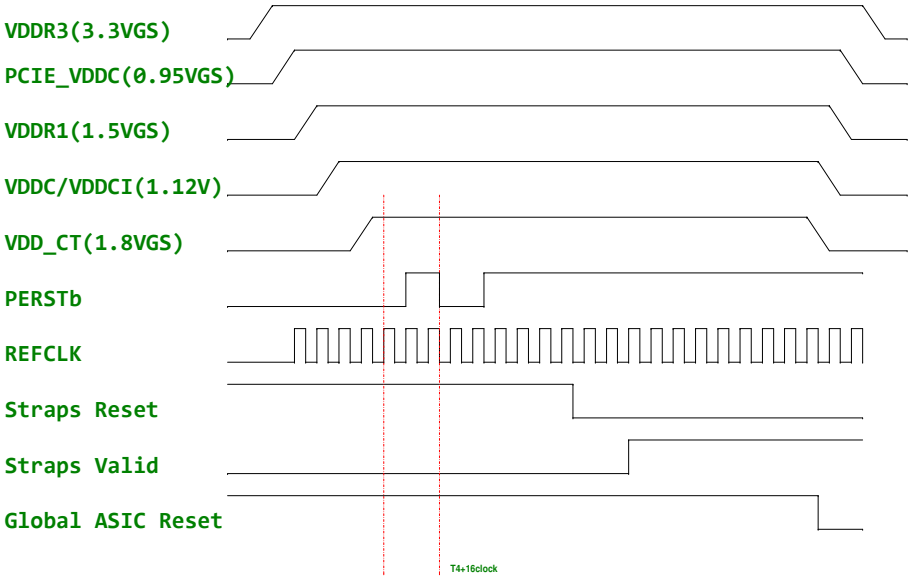
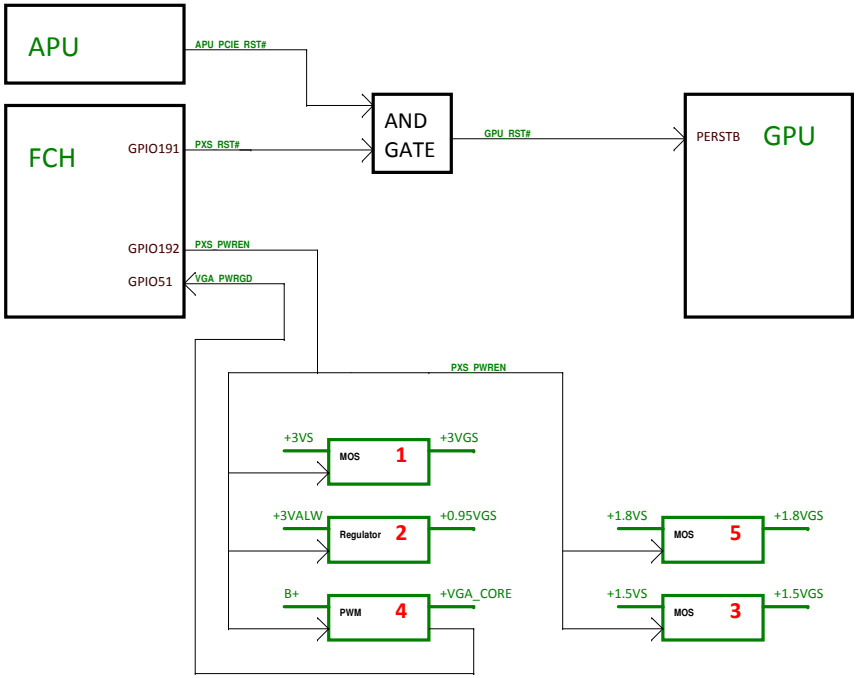
Power-Up/Down Sequence

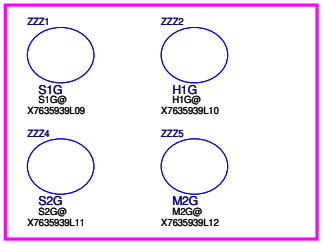
- All the ASIC supplies, except for VDDR3, must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. There is no timing requirement on the ramp up of VDDR3 relative to other power rails.
- The external pull-up resistors on the DDC/AUX signals (if applicable) should ramp up before or after both VDDC and VDD_CT have ramped up.
- VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).
- For power down, reversing the ramp-up sequence is recommended.





SUN PRO VRAM STRAP

	Vendor	PS_3[2]	PS_3[1]	PS_3[0]	R_pu	R_pd
	H5TQ2G63DFR-11C SA00003YO70	0	0	0	R1430 NC	R1436 4.75K
1G	K4W2G1646E-BC11 SA00005SH00	0	0	1	R1430 8.45K	R1436 2K
	MT41J128M16JT-093G SA000067510 FBGA Code:D9PTD	0	1	0	R1430 4.53K	R1436 2K
2G	K4W4G1646B-HC11 SA000068R00	0	1	1	R1430 6.98K	R1436 4.99K
	MT41K256M16HA-107G SA000065D00 FBGA Code:D9PZD	1	0	0	R1430 4.53k	R1436 4.99K
1G	MT41J128M16JT-107G SA00005SM30 FBGA Code:D9PRS	1	0	1	R1430 3.24k	R1436 5.62k
	K4W2G1646E-BC1A SA000068U10	1	1	0	R1430 3.4k	R1436 10k
		1	1	1	R1430 4.75K	R1436 NC



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Title: dGPU Block Diagram

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[17] PCIE_CRX_GTX_P[0..7]
[17] PCIE_CRX_GTX_N[0..7]

PCIE_CTX_GRX_P[0..7] [17]
PCIE_CTX_GRX_N[0..7] [17]

JCPU1A

PCI EXPRESS

PCIE_CRX_GTX_P0	AB8	P_GFX_RXP0	P_GFX_TXP0	AB2	PCIE_CTX_C_GRX_P0	C1	DIS@	1	2	.1U_0402_16V7K	PCIE_CTX_GRX_P0
PCIE_CRX_GTX_N0	AB7	P_GFX_RXN0	P_GFX_TXN0	AB1	PCIE_CTX_C_GRX_N0	C2	DIS@	1	2	.1U_0402_16V7K	PCIE_CTX_GRX_N0
PCIE_CRX_GTX_P1	AA9	P_GFX_RXP1	P_GFX_TXP1	AA3	PCIE_CTX_C_GRX_P1	C3	DIS@	1	2	.1U_0402_16V7K	PCIE_CTX_GRX_P1
PCIE_CRX_GTX_N1	AA8	P_GFX_RXN1	P_GFX_TXN1	AA2	PCIE_CTX_C_GRX_N1	C4	DIS@	1	2	.1U_0402_16V7K	PCIE_CTX_GRX_N1
PCIE_CRX_GTX_P2	AA5	P_GFX_RXP2	P_GFX_TXP2	Y5	PCIE_CTX_C_GRX_P2	C5	DIS@	1	2	.1U_0402_16V7K	PCIE_CTX_GRX_P2
PCIE_CRX_GTX_N2	AA6	P_GFX_RXN2	P_GFX_TXN2	Y4	PCIE_CTX_C_GRX_N2	C6	DIS@	1	2	.1U_0402_16V7K	PCIE_CTX_GRX_N2
PCIE_CRX_GTX_P3	Y8	P_GFX_RXP3	P_GFX_TXP3	Y2	PCIE_CTX_C_GRX_P3	C7	DIS@	1	2	.1U_0402_16V7K	PCIE_CTX_GRX_P3
PCIE_CRX_GTX_N3	Y7	P_GFX_RXN3	P_GFX_TXN3	Y1	PCIE_CTX_C_GRX_N3	C8	DIS@	1	2	.1U_0402_16V7K	PCIE_CTX_GRX_N3
PCIE_CRX_GTX_P4	W9	P_GFX_RXP4	P_GFX_TXP4	W3	PCIE_CTX_C_GRX_P4	C9	DIS@	1	2	.1U_0402_16V7K	PCIE_CTX_GRX_P4
PCIE_CRX_GTX_N4	W8	P_GFX_RXN4	P_GFX_TXN4	W2	PCIE_CTX_C_GRX_N4	C10	DIS@	1	2	.1U_0402_16V7K	PCIE_CTX_GRX_N4
PCIE_CRX_GTX_P5	W5	P_GFX_RXP5	P_GFX_TXP5	V5	PCIE_CTX_C_GRX_P5	C11	DIS@	1	2	.1U_0402_16V7K	PCIE_CTX_GRX_P5
PCIE_CRX_GTX_N5	W6	P_GFX_RXN5	P_GFX_TXN5	V4	PCIE_CTX_C_GRX_N5	C12	DIS@	1	2	.1U_0402_16V7K	PCIE_CTX_GRX_N5
PCIE_CRX_GTX_P6	V8	P_GFX_RXP6	P_GFX_TXP6	V2	PCIE_CTX_C_GRX_P6	C13	DIS@	1	2	.1U_0402_16V7K	PCIE_CTX_GRX_P6
PCIE_CRX_GTX_N6	V7	P_GFX_RXN6	P_GFX_TXN6	V1	PCIE_CTX_C_GRX_N6	C14	DIS@	1	2	.1U_0402_16V7K	PCIE_CTX_GRX_N6
PCIE_CRX_GTX_P7	U9	P_GFX_RXP7	P_GFX_TXP7	U3	PCIE_CTX_C_GRX_P7	C15	DIS@	1	2	.1U_0402_16V7K	PCIE_CTX_GRX_P7
PCIE_CRX_GTX_N7	U8	P_GFX_RXN7	P_GFX_TXN7	U2	PCIE_CTX_C_GRX_N7	C16	DIS@	1	2	.1U_0402_16V7K	PCIE_CTX_GRX_N7

GRAPHICS

U5 P_GFX_RXP8 P_GFX_TXP8 T5
U6 P_GFX_RXN8 P_GFX_TXN8 T4
T8 P_GFX_RXP9 P_GFX_TXP9 T2
T7 P_GFX_RXN9 P_GFX_TXN9 T1
R9 P_GFX_RXP10 P_GFX_TXP10 R3
R8 P_GFX_RXN10 P_GFX_TXN10 R2
R5 P_GFX_RXP11 P_GFX_TXP11 P5
R6 P_GFX_RXN11 P_GFX_TXN11 P4
P8 P_GFX_RXP12 P_GFX_TXP12 P2
P7 P_GFX_RXN12 P_GFX_TXN12 P1
N9 P_GFX_RXP13 P_GFX_TXP13 N3
N8 P_GFX_RXN13 P_GFX_TXN13 N2
N5 P_GFX_RXP14 P_GFX_TXP14 M5
N6 P_GFX_RXN14 P_GFX_TXN14 M4
M8 P_GFX_RXP15 P_GFX_TXP15 M2
M7 P_GFX_RXN15 P_GFX_TXN15 M1

SDV/FVT, NO.1

SDV/FVT, NO.1

GPP

	AE5	P_GPP_RXP0	P_GPP_TXP0	AD5	PCIE_CTX_C_DRX_P0	C33	1	2	.1U_0402_16V7K	PCIE_CTX_DRX_P0	[35]
[35] PCIE_CRX_DTX_P0	AE6	P_GPP_RXN0	P_GPP_TXN0	AD4	PCIE_CTX_C_DRX_N0	C34	1	2	.1U_0402_16V7K	PCIE_CTX_DRX_N0	[35]
[35] PCIE_CRX_DTX_N0	AD8	P_GPP_RXP1	P_GPP_TXP1	AD2	PCIE_CTX_C_DRX_P1	C123	1	2	.1U_0402_16V7K	PCIE_CTX_DRX_P1	[33]
[33] PCIE_CRX_DTX_P1	AD7	P_GPP_RXN1	P_GPP_TXN1	AD1	PCIE_CTX_C_DRX_N1	C124	1	2	.1U_0402_16V7K	PCIE_CTX_DRX_N1	[33]
[33] PCIE_CRX_DTX_N1	AC9	P_GPP_RXP2	P_GPP_TXP2	AC3							
	AC8	P_GPP_RXN2	P_GPP_TXN2	AC2							
[35] PCIE_CRX_DTX_P3	AC5	P_GPP_RXP3	P_GPP_TXP3	AB5	PCIE_CTX_C_DRX_P3	C35	1	2	.1U_0402_16V7K	PCIE_CTX_DRX_P3	[35]
[35] PCIE_CRX_DTX_N3	AC6	P_GPP_RXN3	P_GPP_TXN3	AB4	PCIE_CTX_C_DRX_N3	C36	1	2	.1U_0402_16V7K	PCIE_CTX_DRX_N3	[35]

UMI

[12] UMI_RXP0	AG8	P_UMI_RXP0	P_UMI_TXP0	AG2	UMI_TXP0_C	C37	1	2	.1U_0402_16V7K	UMI_TXP0	[12]
[12] UMI_RXN0	AG9	P_UMI_RXN0	P_UMI_TXN0	AG3	UMI_TXN0_C	C38	1	2	.1U_0402_16V7K	UMI_TXN0	[12]
[12] UMI_RXP1	AG6	P_UMI_RXP1	P_UMI_TXP1	AF4	UMI_TXP1_C	C39	1	2	.1U_0402_16V7K	UMI_TXP1	[12]
[12] UMI_RXN1	AG5	P_UMI_RXN1	P_UMI_TXN1	AF5	UMI_TXN1_C	C40	1	2	.1U_0402_16V7K	UMI_TXN1	[12]
[12] UMI_RXP2	AF7	P_UMI_RXP2	P_UMI_TXP2	AF1	UMI_TXP2_C	C41	1	2	.1U_0402_16V7K	UMI_TXP2	[12]
[12] UMI_RXN2	AF8	P_UMI_RXN2	P_UMI_TXN2	AF2	UMI_TXN2_C	C42	1	2	.1U_0402_16V7K	UMI_TXN2	[12]
[12] UMI_RXP3	AE8	P_UMI_RXP3	P_UMI_TXP3	AE2	UMI_TXP3_C	C43	1	2	.1U_0402_16V7K	UMI_TXP3	[12]
[12] UMI_RXN3	AE9	P_UMI_RXN3	P_UMI_TXN3	AE3	UMI_TXN3_C	C44	1	2	.1U_0402_16V7K	UMI_TXN3	[12]

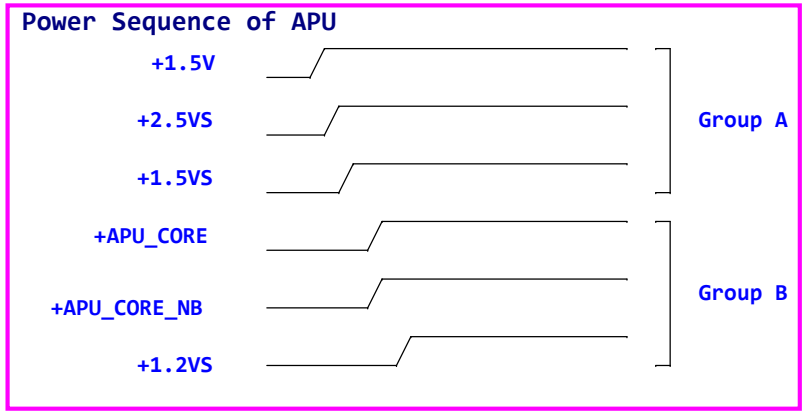
LAN
WLAN
Card Reader

+1.2VS — 1 R1 2 P_ZVDDP 196_0402_1% — AG11 P_ZVDDP

AH11 P_ZVSS — 1 R2 2 196_0402_1% — P_ZVSS

LOTES_ACA-ZIF-109-P12-A_FS1R2
CONN@

Power Sequence of APU



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Title: FS1r2 PCIE/UMI

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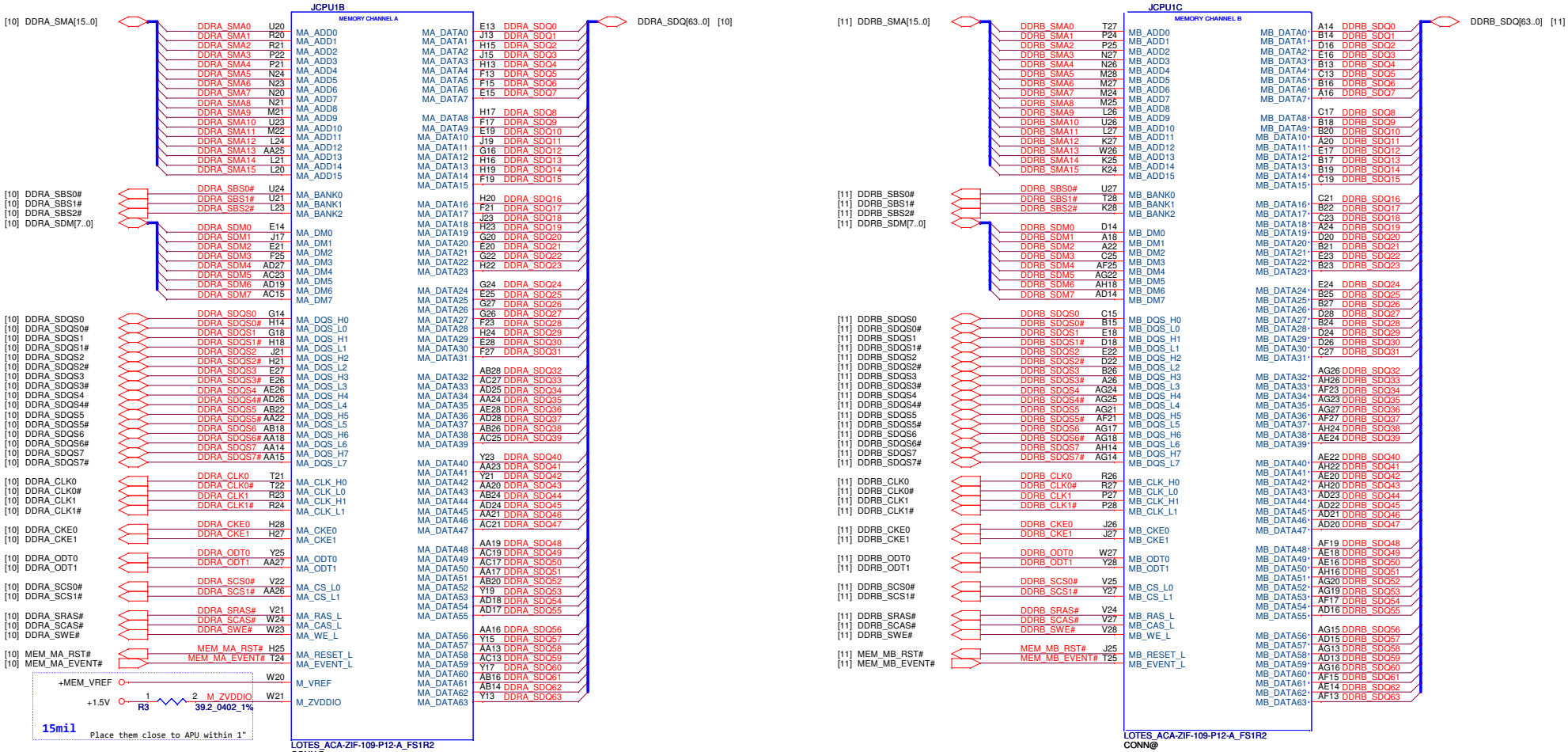
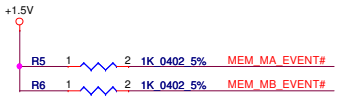
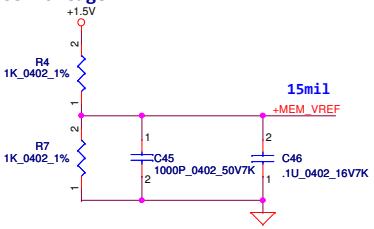


EVENT# pull high



0.75V reference voltage



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Title: FS1r2 DDRIII Memory I/F

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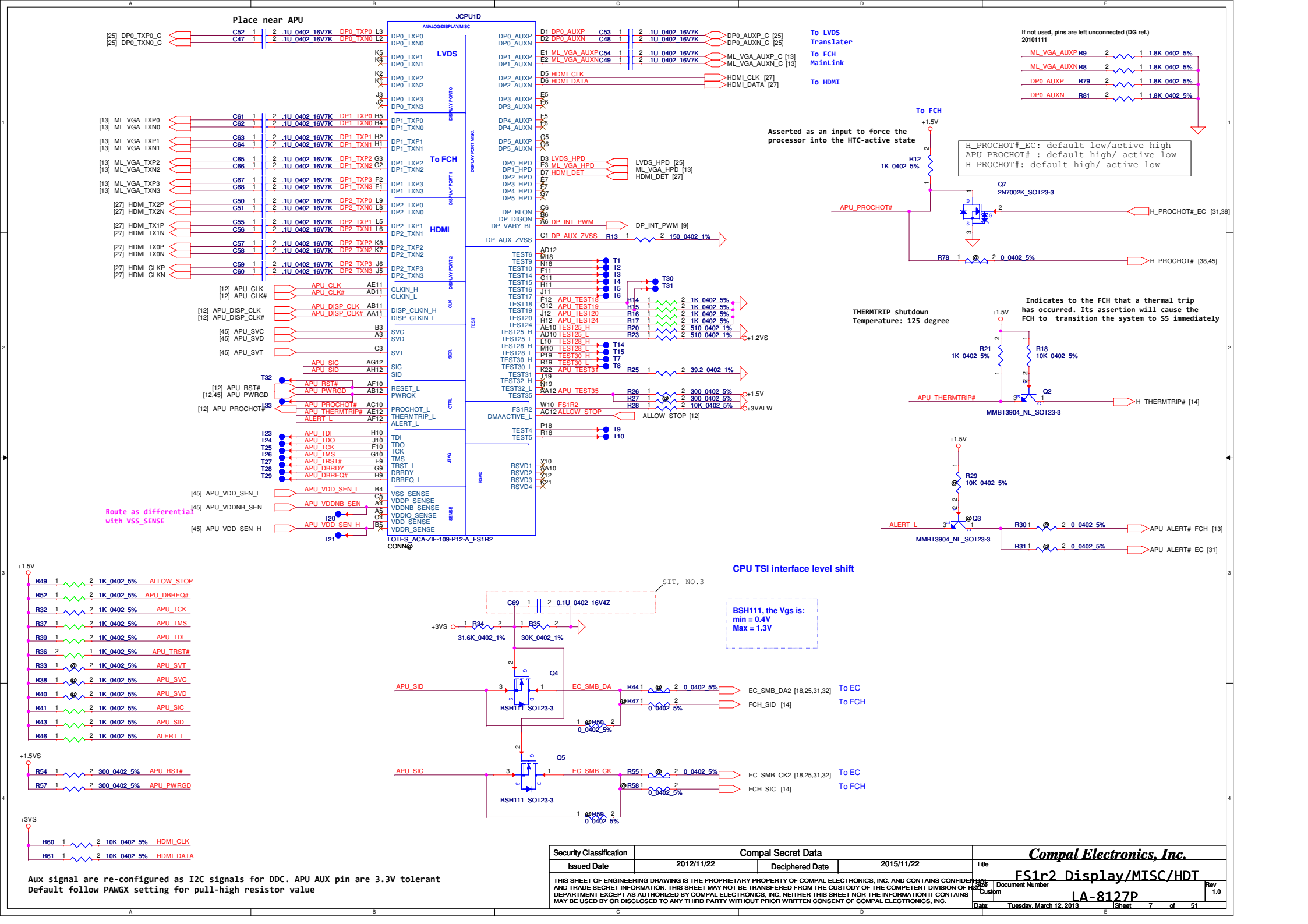

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Compal Electronics, Inc.			
Title: FS1r2 Display/MISC/HDT			
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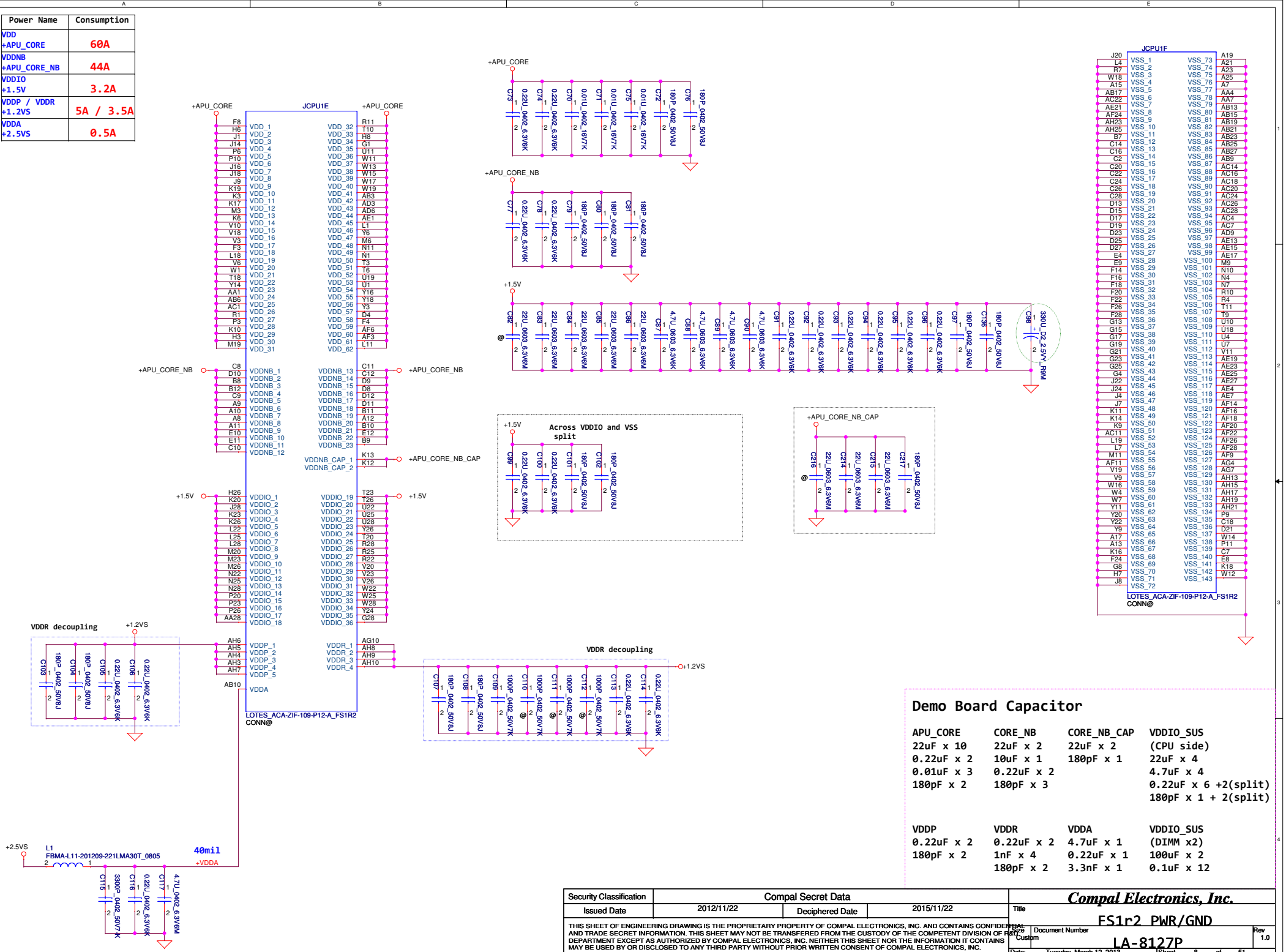
Power Name	Consumption
VDD +APU_CORE	60A
VDDNB +APU_CORE_NB	44A
VDDIO +1.5V	3.2A
VDDP / VDDR +1.2VS	5A / 3.5A
VDDA +2.5VS	0.5A



Demo Board Capacitor

APU_CORE	CORE_NB	CORE_NB_CAP	VDDIO_SUS
22uF x 10	22uF x 2	22uF x 2	(CPU side)
0.22uF x 2	10uF x 1	180pF x 1	22uF x 4
0.01uF x 3	0.22uF x 2		4.7uF x 4
180pF x 2	180pF x 3		0.22uF x 6 +2(split)
			180pF x 1 + 2(split)

VDDP	VDDR	VDDA	VDDIO_SUS
0.22uF x 2	0.22uF x 2	4.7uF x 1	(DIMM x2)
180pF x 2	1nF x 4	0.22uF x 1	100uF x 2
	180pF x 2	3.3nF x 1	0.1uF x 12

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Title: FS1r2 PWR/GND

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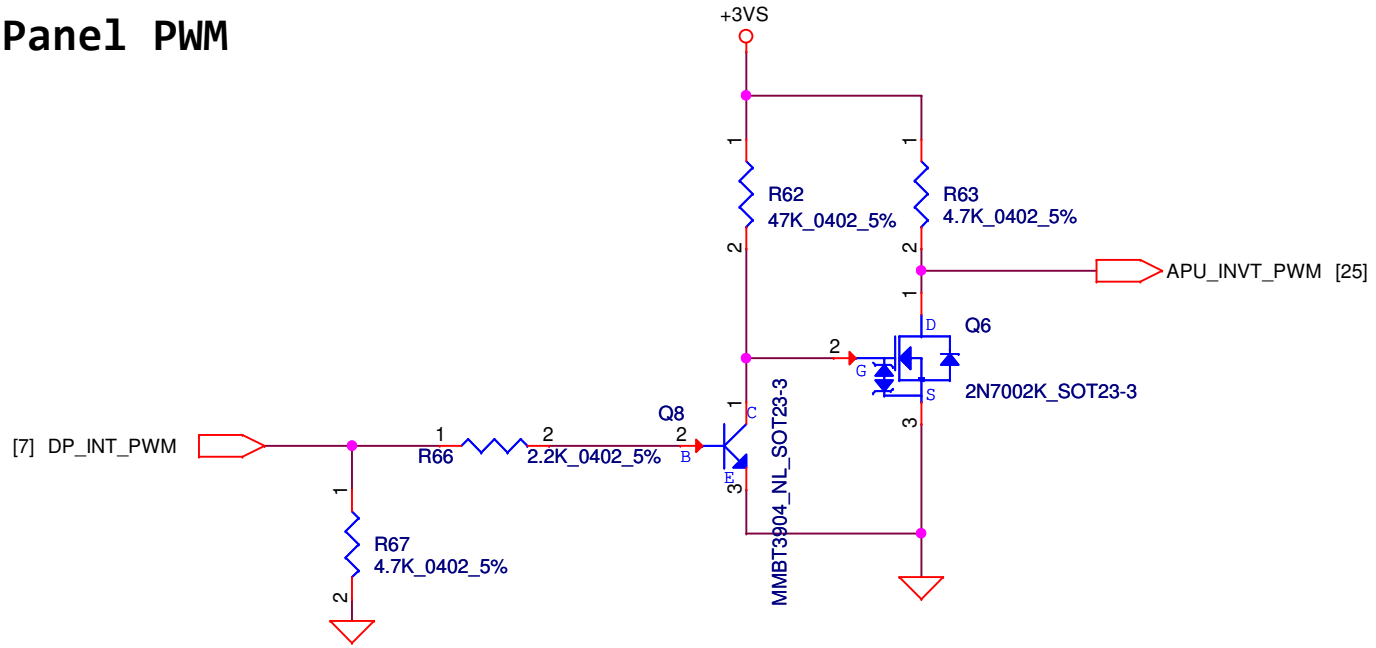
Panel PWM



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Title: FS1r2 Signal Level Shifter

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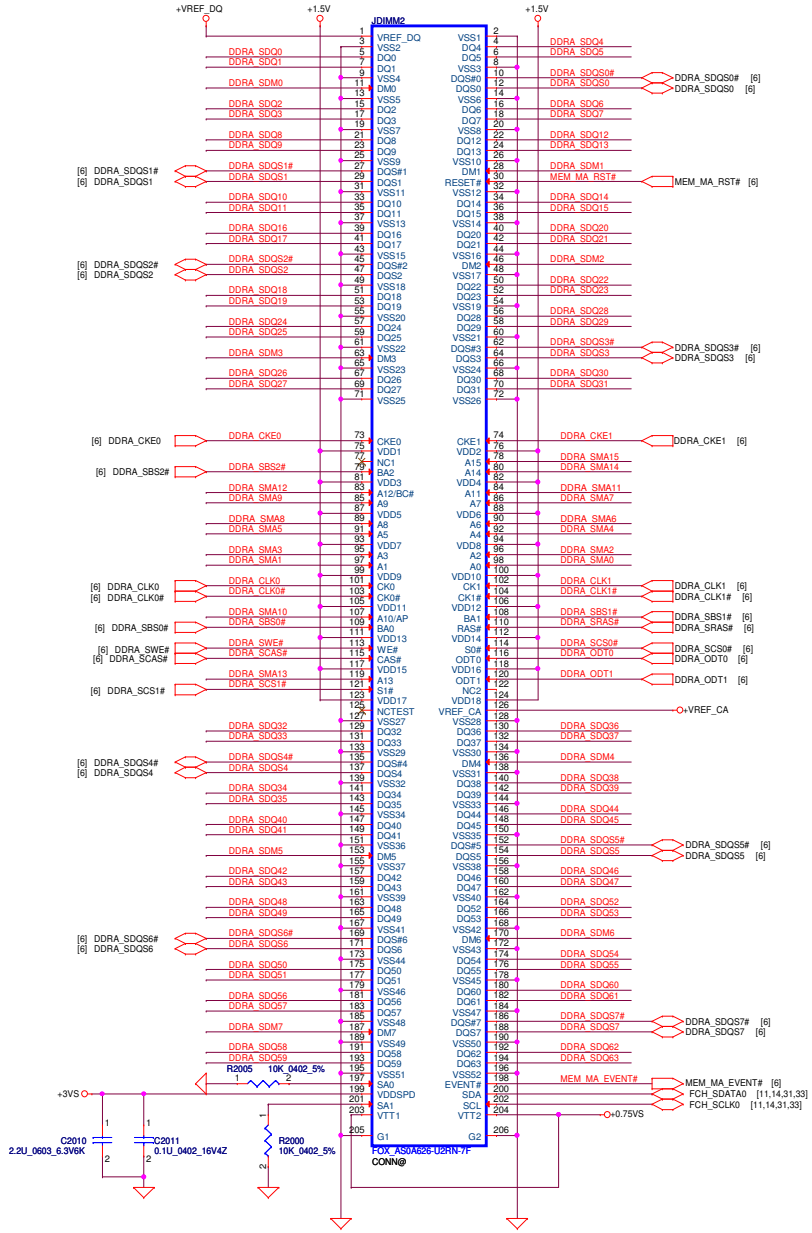
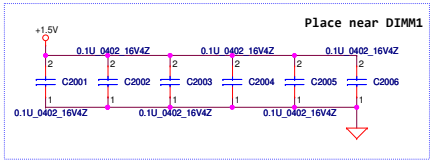
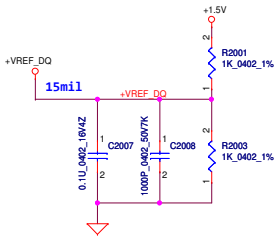
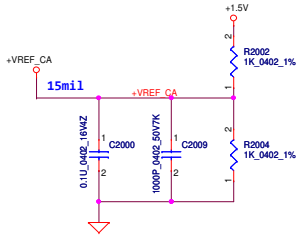
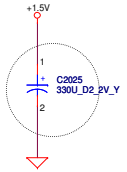


Reverse H:5.2mm









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Compal Electronics, Inc.

Title: DDRIII SO-DIMM 1

Size	Document Number	Rev
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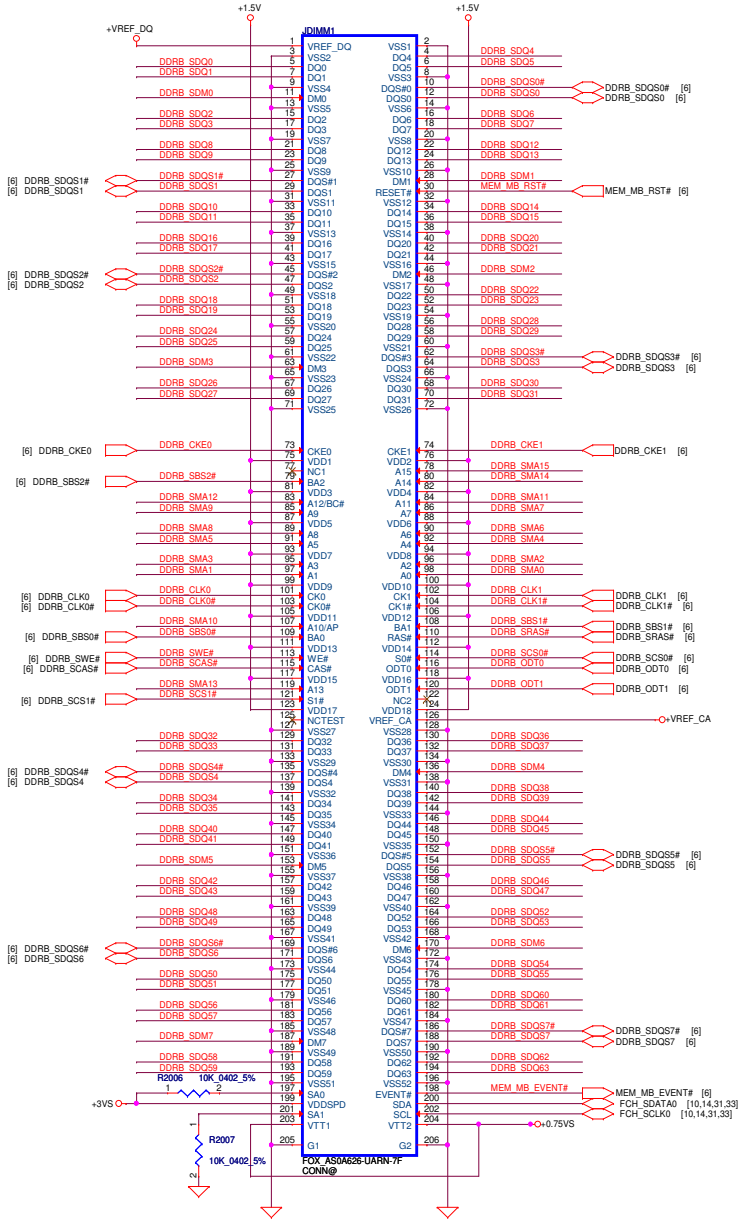

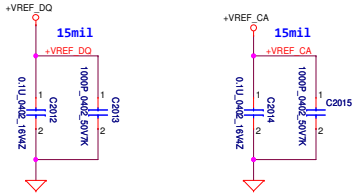

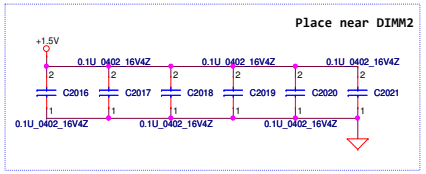

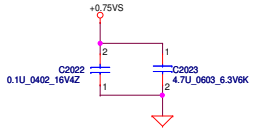

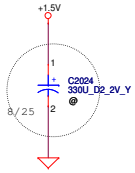

Security Classification	Compal Secret Data		
Issued Date	2012/11/22	Deciphered Date	2015/11/22

Compal Electronics, Inc.

Title: DDRIII SO-DIMM 2

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SDV/FVT, NO.12

U2A

HUDSON-2

R90/ C146 close to FCH

C125 150P_0402_50V8J

PLT_RST# → R73 33_0402_5% → APU_PCIE_RST# _C → A_RST#

PCIE_RST#

UMI_RXP0 C126 .1U_0402_16V7K → UMI_RXP0_C
UMI_RXN0 C118 .1U_0402_16V7K → UMI_RXN0_C
UMI_RXP1 C119 .1U_0402_16V7K → UMI_RXP1_C
UMI_RXN1 C120 .1U_0402_16V7K → UMI_RXN1_C
UMI_RXP2 C127 .1U_0402_16V7K → UMI_RXP2_C
UMI_RXN2 C121 .1U_0402_16V7K → UMI_RXN2_C
UMI_RXP3 C128 .1U_0402_16V7K → UMI_RXP3_C
UMI_RXN3 C122 .1U_0402_16V7K → UMI_RXN3_C

UMI_TX0P UMI_TX0N UMI_TX1P UMI_TX1N UMI_TX2P UMI_TX2N UMI_TX3P UMI_TX3N

UMI_RX0P UMI_RX0N UMI_RX1P UMI_RX1N UMI_RX2P UMI_RX2N UMI_RX3P UMI_RX3N

R71 590_0402_1% PCIE_CALRP
R73 2K_0402_1% PCIE_CALRN
+VDDAN_11_PCIE

PCIE_CALRP PCIE_CALRN

GPP_TX0P GPP_TX0N GPP_TX1P GPP_TX1N GPP_TX2P GPP_TX2N GPP_TX3P GPP_TX3N

GPP_RX0P GPP_RX0N GPP_RX1P GPP_RX1N GPP_RX2P GPP_RX2N GPP_RX3P GPP_RX3N

PCI EXPRESS INTERFACES

C129 22P_0402_50V8J 32K_X1
R75 20M_0402_5%
Y1 32.768KHZ_12.5PF_CM31532768DZFT
C130 22P_0402_50V8J 32K_X2
Close to HUDSON-M2/3

R74 2K_0402_1% CLK_CALRN
+1.1VS_CKVDD

CLK_CALRN

C131 10P_0402_50V8J 25M_X1
X1 25MHZ_10PF_X3G025000DA1H-X
R88 1M_0402_5%
C134 10P_0402_50V8J 25M_X2

PCIE_RCLKP PCIE_RCLKN

[7] APU_DISP_CLK → R26 DISP_CLKP
[7] APU_DISP_CLK# → T26 DISP_CLKN

H33 DISP2_CLKP
H31 DISP2_CLKN

[7] APU_CLK → T24 APU_CLKP
[7] APU_CLK# → T23 APU_CLKN

[17] CLK_PCIE_VGA → R76 0_0402_5% CLK_PCIE_VGA_R → J30 SLT_GFX_CLKP
[17] CLK_PCIE_VGA# → R77 0_0402_5% CLK_PCIE_VGA#_R → K29 SLT_GFX_CLKN

GPP_CLK0P GPP_CLK0N GPP_CLK1P GPP_CLK1N

WLAN
[33] CLK_PCIE_WLAN → R150 0_0402_5% CLK_PCIE_WLAN_R → F33 GPP_CLK2P
[33] CLK_PCIE_WLAN# → R142 0_0402_5% CLK_PCIE_WLAN#_R → F31 GPP_CLK2N

LAN
[35] CLK_PCIE_LAN → R80 33_0402_5% CLK_PCIE_LAN_R → E33 GPP_CLK3P
[35] CLK_PCIE_LAN# → R82 33_0402_5% CLK_PCIE_LAN#_R → E31 GPP_CLK3N

GPP_CLK4P GPP_CLK4N GPP_CLK5P GPP_CLK5N

Card Reader
[35] CLK_PCIE_CARD → R83 33_0402_5% CLK_PCIE_CARD_R → N25 GPP_CLK6P
[35] CLK_PCIE_CARD# → R84 33_0402_5% CLK_PCIE_CARD#_R → N26 GPP_CLK6N

GPP_CLK7P GPP_CLK7N GPP_CLK8P GPP_CLK8N

[35] CLK_LAN_25M → R86 22_0402_5% CLK_LAN_25M_R → J26 14M_25M_48M_OSC

25M_X1 C31 25M_X1
25M_X2 C33 25M_X2

CLOCK GENERATOR

PCI_CLK1 [16]
PCI_CLK3 [16]
PCI_CLK4 [16]

PCICLK0 PCICLK1/GPO36 PCICLK2/GPO37 PCICLK3/GPO38 PCICLK4/14M_OSC/GPO39

PCIRST#

AD0/GPIO0 AD1/GPIO1 AD2/GPIO2 AD3/GPIO3 AD4/GPIO4 AD5/GPIO5 AD6/GPIO6 AD7/GPIO7 AD8/GPIO8 AD9/GPIO9 AD10/GPIO10 AD11/GPIO11 AD12/GPIO12 AD13/GPIO13 AD14/GPIO14 AD15/GPIO15 AD16/GPIO16 AD17/GPIO17 AD18/GPIO18 AD19/GPIO19 AD20/GPIO20 AD21/GPIO21 AD22/GPIO22

PCI_AD23 [16]
PCI_AD24 [16]
PCI_AD25 [16]
PCI_AD26 [16]
PCI_AD27 [16]

AD23/GPIO23 AD24/GPIO24 AD25/GPIO25 AD26/GPIO26 AD27/GPIO27 AD28/GPIO28 AD29/GPIO29 AD30/GPIO30 AD31/GPIO31

CBE0# CBE1# CBE2# CBE3# FRAME# DEVSEL# IRDY# TRDY# PAR STOP# PERR# SERR# REQ0#

REQ1#/GPIO40
REQ2#/CLK_REQ8#/GPIO41
REQ3#/CLK_REQ5#/GPIO42
GNT0#
GNT1#/GPO44
GNT2#/SD_LED/GPO45
GNT3#/CLK_REQ7#/GPIO46
CLKRUN#
LOCK#

T11
R209 0_0402_5% → PXS_RST# [14,17]
R208 0_0402_5% → PXS_PWREN [14,19,43,44]
T22

INTE#/GPIO32 INTF#/GPIO33 INTG#/GPIO34 INTH#/GPIO35

PCI INTERFACE

R110 0_0402_5% → CLK_PCI_DB [33,35]
R215 33_0402_5% → CLK_PCI_EC [16,31]

LPCCLK0

LPCCLK1 LAD0 LAD1 LAD2 LAD3 LFRAME# LDRQ0# LDRQ1#/CLK_REQ6#/GPIO49 SERIRQ/GPIO48

LPC_CLK1 [16]
LPC_AD0 [31,33,35]
LPC_AD1 [31,33,35]
LPC_AD2 [31,33,35]
LPC_AD3 [31,33,35]
LPC_FRAME# [31,33,35]
SERIRQ [31]

LPC

DMA_ACTIVE# PROCHOT# APU_PG LDT_STP# APU_RST#

R85 0_0402_5% APU_PROCHOT#_R
ALLOW_STOP [7]
APU_PROCHOT# [7]
APU_PWRGD [45,7]
APU_RST# [7]

APU

S5_CORE_EN RTCCLK INTRUDER_ALERT# VDDBT_RTC_G

RTC_CLK [16,31]
+RTCBATT
W=20mils
R87 510_0402_5%
C132 1U_0402_6.3V6K
JCMOS1 @ SHORT PADS
for Clear CMOS

32K_X1 32K_X2

S5 PLUS

For PCIE device reset on FS1
(GFX,GLAN,WLAN,LVDS Travis)
APU_PCIE_RST #: Reset PCIE device on APU

+3V_FCH
C133 0.1U_0402_16V4Z
MC74VHC1G08DFT2G_SC70-5 U3
APU_PCIE_RST# C → R89 33_0402_5% → APU_PCIE_RST# [17,33,35]
R89/ C135 close to FCH
C135 150P_0402_50V8J
R90 @ 8.2K_0402_5%
@R92 0_0402_5%
R91 0_0402_5% @ → PLT_RST# [31,35]

218-0844000 A0 BOLTON-M3

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Compal Electronics, Inc.

Title: FCH_PCIE/CLK/PCI/LPC/RTC

Size: Custom | Document Number: LA-8127P | Rev: 1.0

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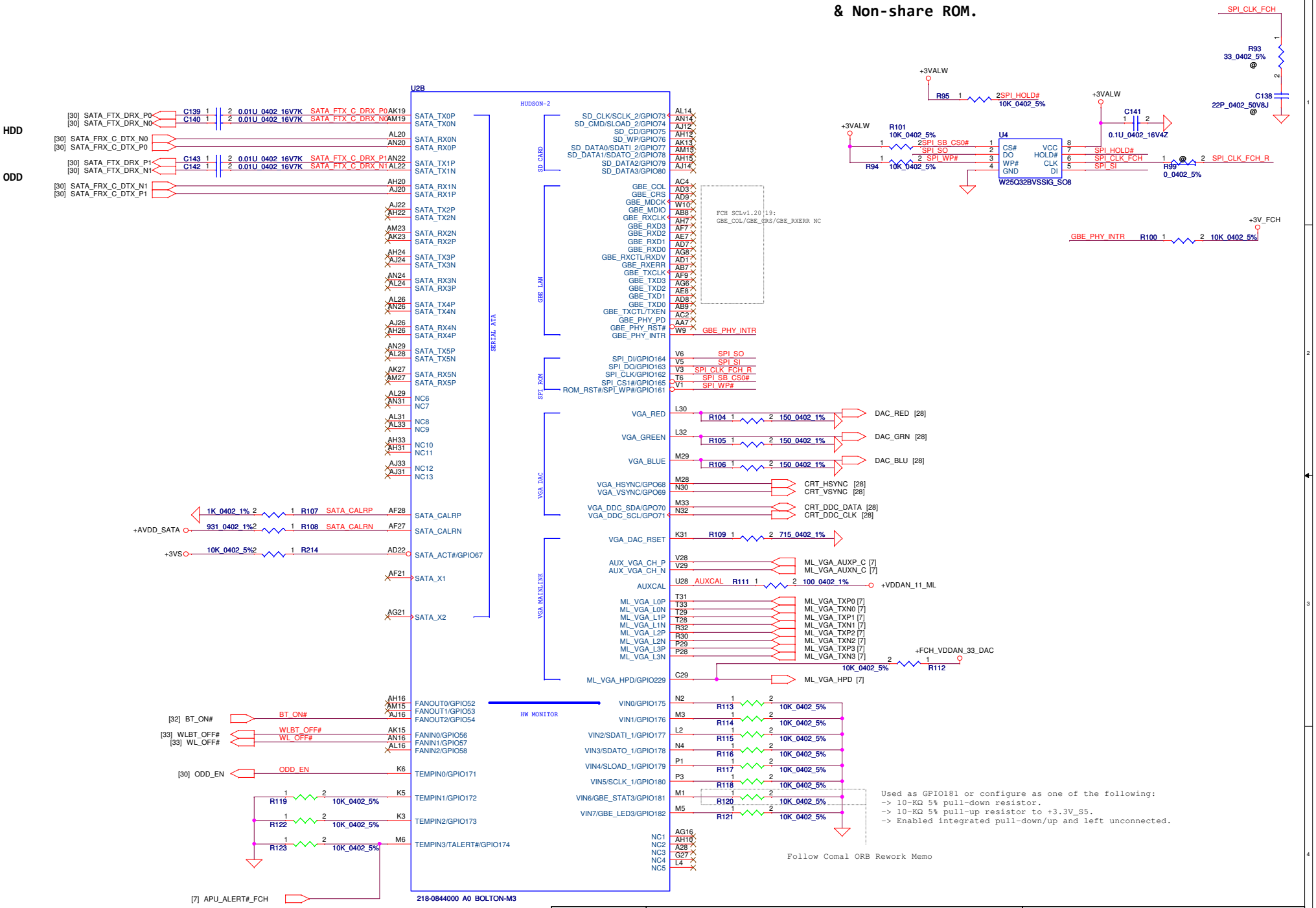
4MB SPI ROM & Non-share ROM.



Security Classification	Compal Secret Data		
Issued Date	2012/11/22	Deciphered Date	2015/11/22

Compal Electronics, Inc.

Title: FCH_SATA/SPI/VGA/HWM/SD

Size	Document Number	Rev
B25 Custom	LA-8127P	1.0

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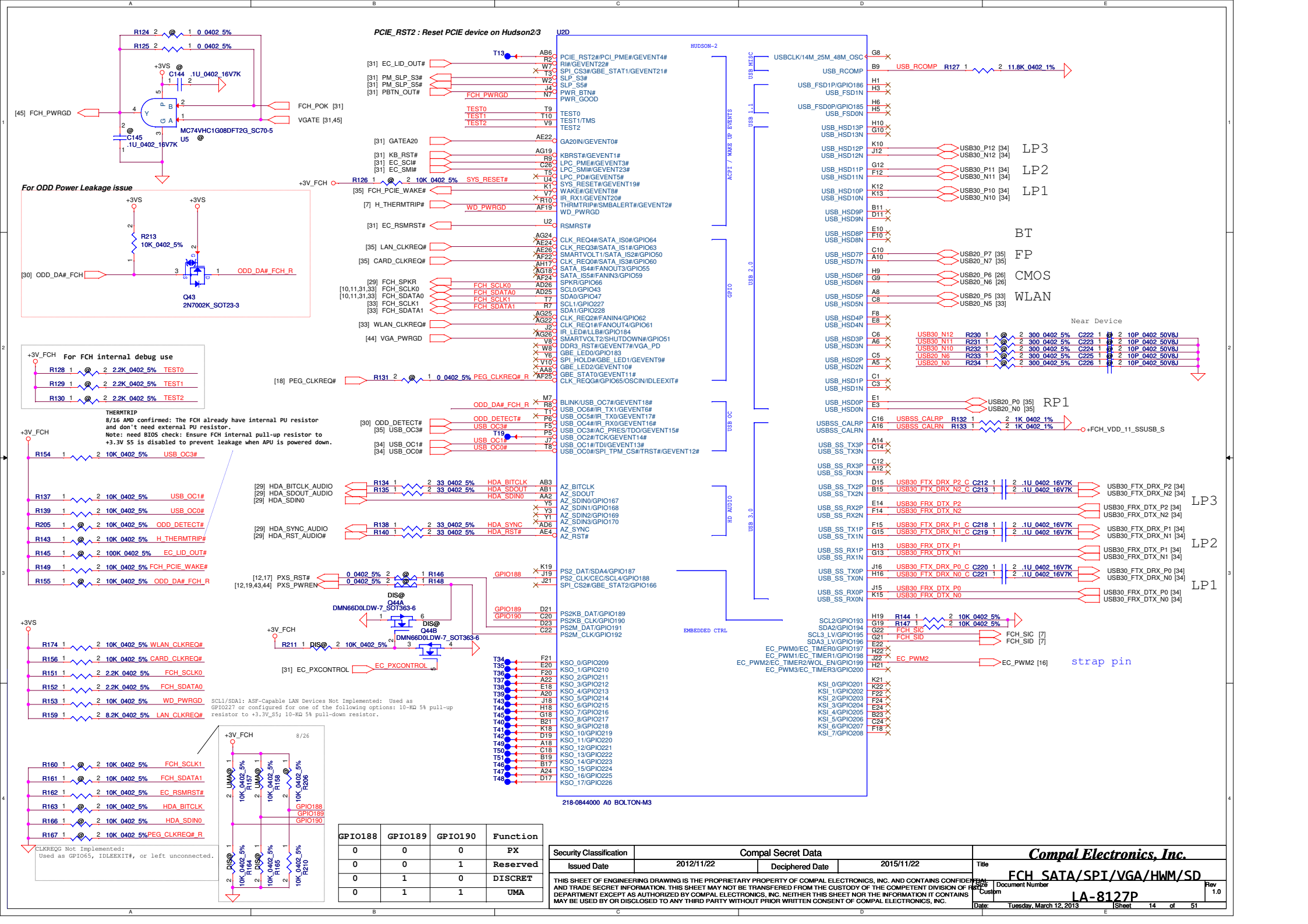

GPIO188	GPIO189	GPIO190	Function
0	0	0	PX
0	0	1	Reserved
0	1	0	DISCRET
0	1	1	UMA

Compal Electronics, Inc.

Title: FCH_SATA/SPI/VGA/HWM/SD

Size: B2S Custom | Document Number: LA-8127P | Rev: 1.0

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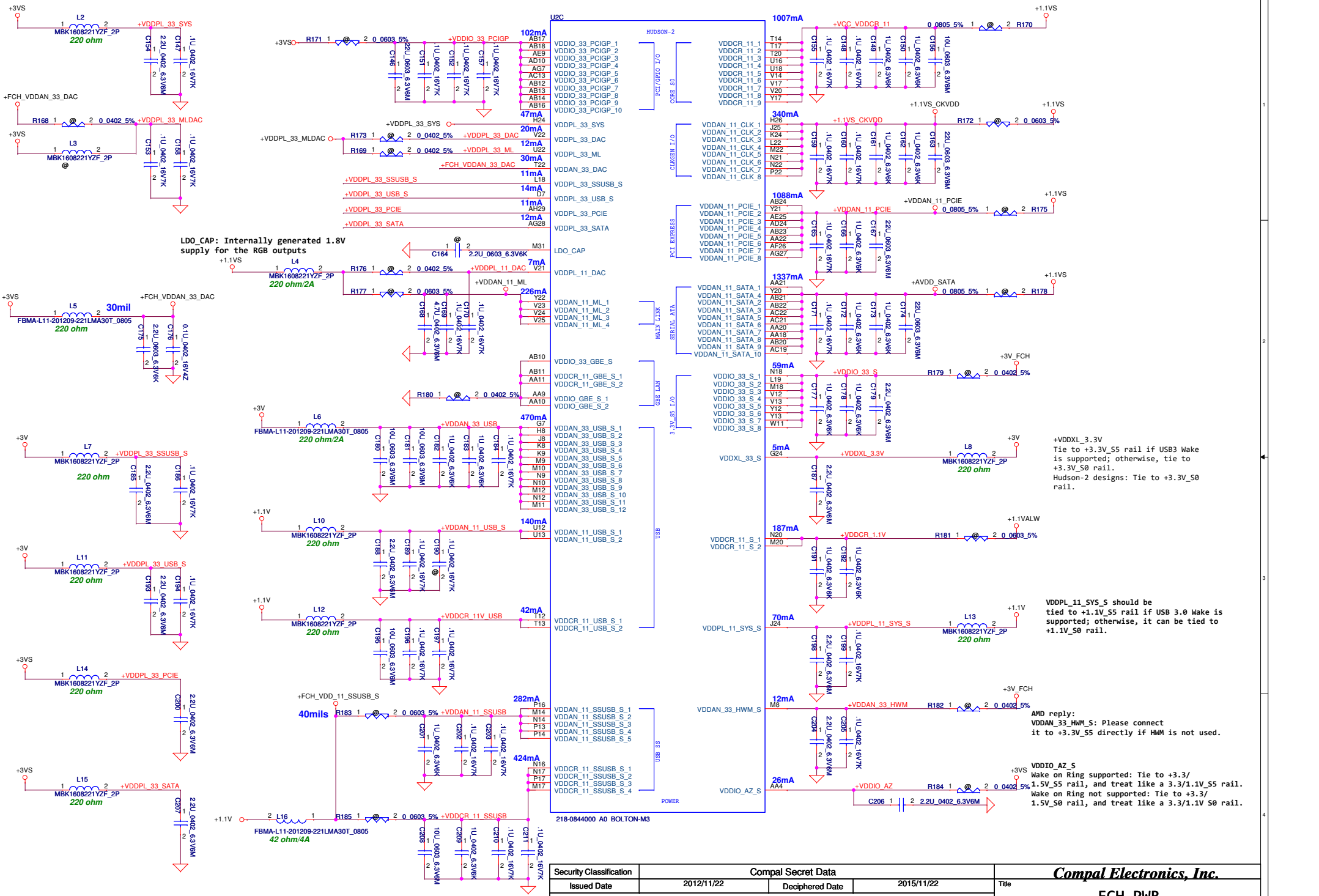

Security Classification	Compal Secret Data		
Issued Date	2012/11/22	Deciphered Date	2015/11/22

Compal Electronics, Inc.			
Title: FCH_PWR			
Size: Custom	Document Number: LA-8127P		Rev: 1.0
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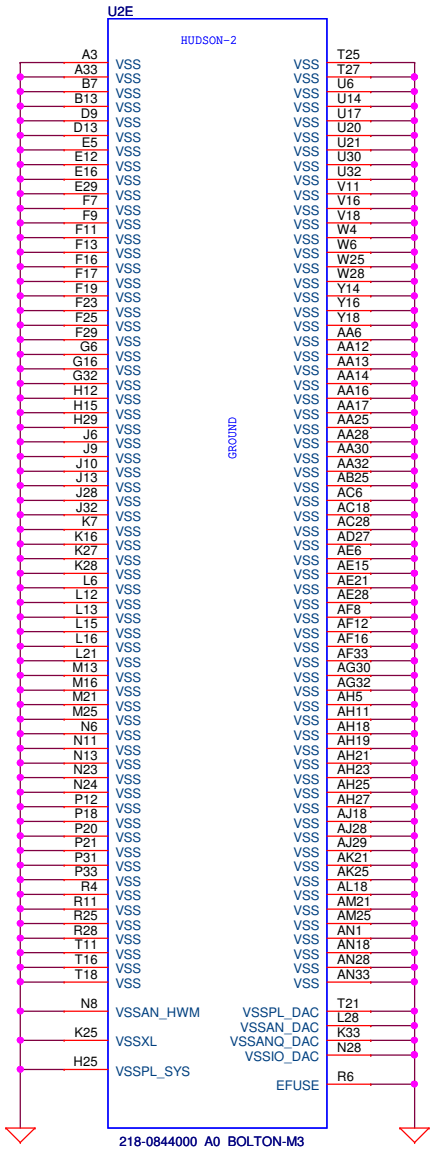


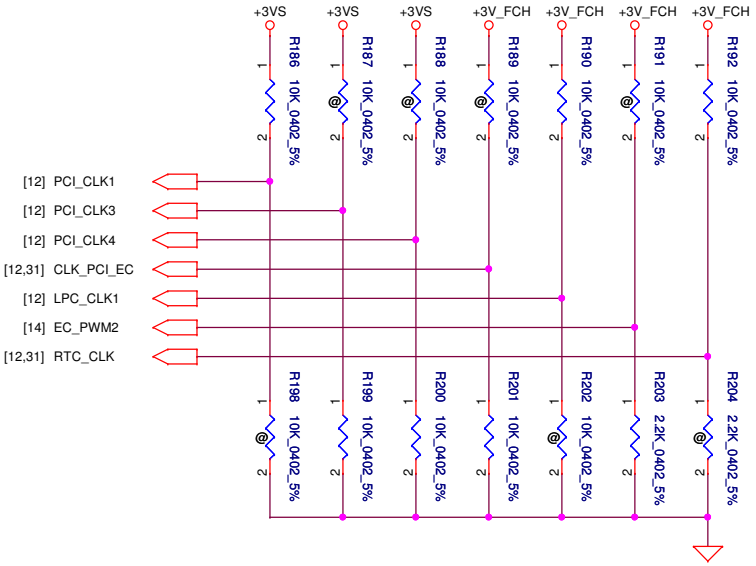
STRAP PINS

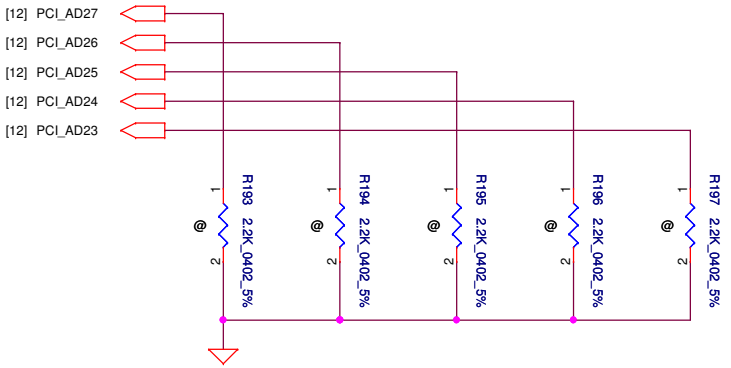
	PCI_CLK1	PCI_CLK3	PCI_CLK4	CLK_PCI_EC	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT





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Compal Electronics, Inc.

Title: FCH-VSS/Strap

Size: B | Document Number: LA-8127P | Rev: 1.0

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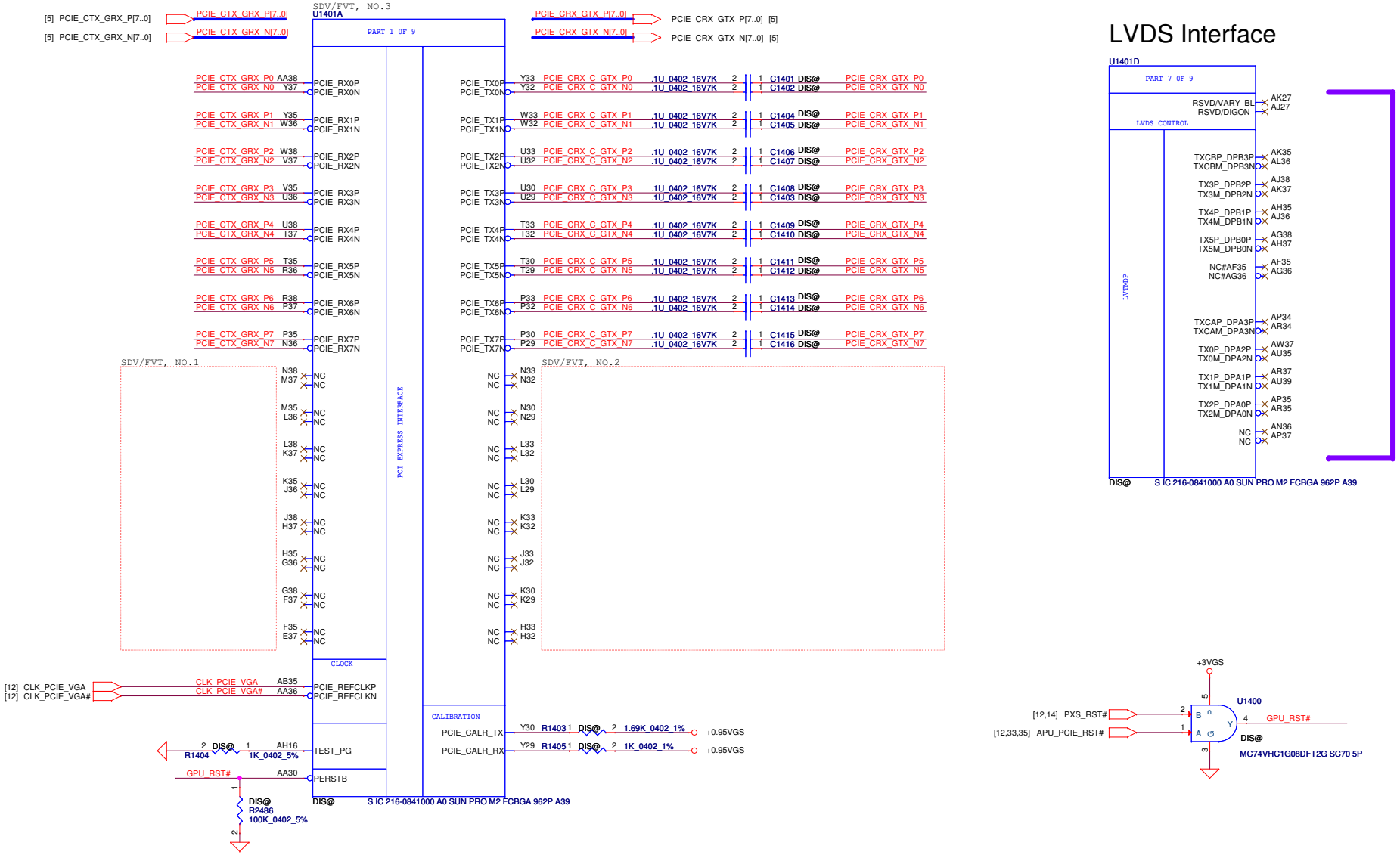

LVDS Interface

SUN NC

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Issued Date	2012/11/22	Deciphered Date 2015/11/22	Title: ATI_Sun Pro_M2_PCIE/LVDS
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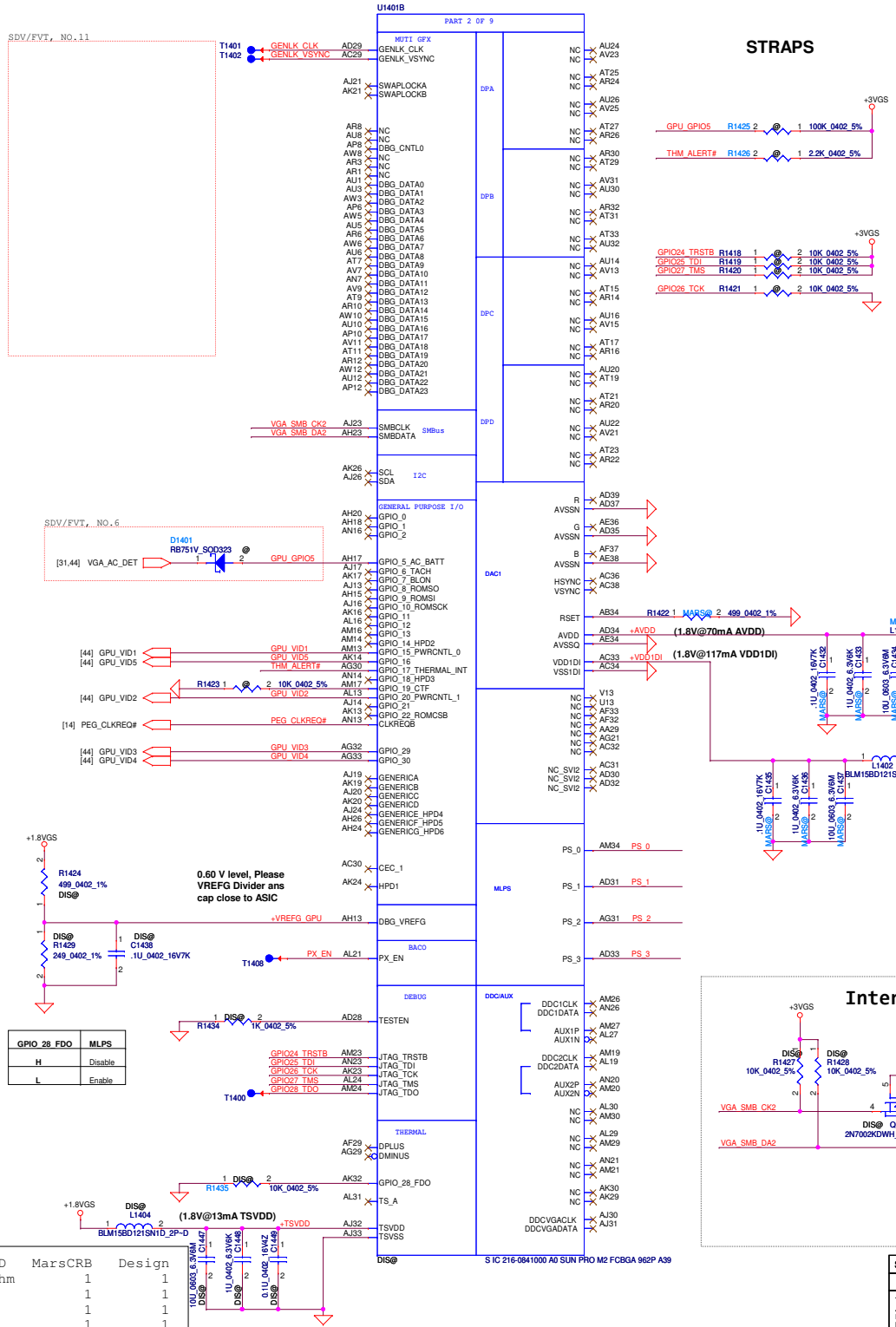


STRAPS

Resistor Divider Lookup Lable		
R_pu (ohm) R1430	R_pd (ohm) R1436	Bitd [3:1]
NC	4.75k	000
8.45k	2k	001
4.53k	2k	010
6.98k	4.99k	011
4.53k	4.99k	100
3.24k	5.62k	101
3.4k	10k	110
4.75k	NC	111

0402 1% resistors are equired

Capacitor Divider Lookup Lable		
Cap (nF) C1439	Bitd [5:4]	Compal PN
680nF	00	SE00000YJ80
82nF	01	SE076823K80
10nF	10	SE074103KN0
NC	11	

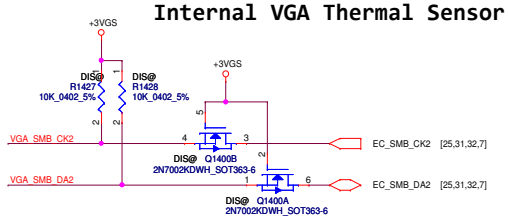
AVDD	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

VDD1DI	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

TSVDD	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

GPIO_28_FDO	MLPS
H	Disable
L	Enable

Internal VGA Thermal Sensor



CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

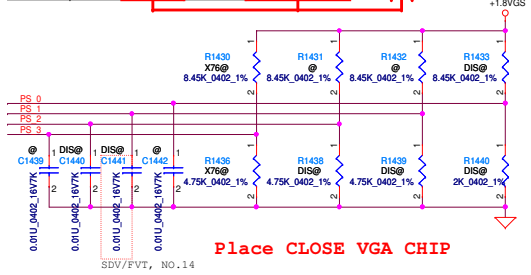
RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	MLPS	DESCRIPTION OF DEFAULT SETTINGS	Default Setting
TX_PWRS_ENB	PS_1[4]	Transmitter Power Savings Enable 0:50% Tx output swing 1:Full Tx output swing	X
TX_DEEMPH_EN	PS_1[5]	PCIE Transmitter De-emphasis Enable 0:Tx de-emphasis disabled 1:Tx de-emphasis enabled	X
BIF_GEN3_EN_A	PS_1[1]	PCIE Gen3 Enable (NOTE:RESERVED for Thames/Seymour and should be strapped to 0) 0:GEN3 not support at power-on 1:GEN3 supported at power-on	1
BIF_VGA DIS	PS_2[4]	VGA control 0:VGA controller capacity enabled 1:VGA controller capacity disabled (for multi-GPU)	0
ROMIDCFG[2:0]	PS_0[3..1]	Serial ROM type or Memory Aperture Size Select If PS_2[3]=0, defines memory aperture size If PS_2[3]=1, defines ROM type 100 - 512Kbit M25P05A (ST) 101 - 1Mbit M25P10A (ST) 101 - 2Mbit M25P20 (ST) 101 - 4Mbit M25P40 (ST) 101 - 8Mbit M25P80 (ST) 100 - 512Kbit Pm25LV010 (Chingis) 101 - 1Mbit Pm25LV010 (Chingis)	XXX
BIOS_ROM_EN	PS_2[3]	Enable external BIOS ROM device 0:Disabled 1:Enabled	X
AUD[1] AUD[0]	NA NA	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled. It isthe responsibility of the system designer to ensure that the system is entitled to support this feature.	XX
CEC_DIS	PS_0[4]	Reserved for future ASIC	0
		NOTE:ALLOW FOR PULLUP PADS FOR THE RESERVED STRAPS BUT DO NOT INSTALL RESISTOR IF THESE GPIOS ARE USEED, THEY MUST KEEP LOW AND NOT CONFLICT DURING RESET	
RESERVED	PS_1[3]	Reserved	0
RESERVED	PS_1[2]	Reserved	0
RESERVED	NA	Reserved	0
RESERVED	NA	Reserved (for Thames/Whistler/Seymour only)	0
AUD_PORT_CONN_PINSTRAP[2] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[0]	PS_3[5] PS_3[4] PS_0[5]	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	XXX

MLPS Strap

	Bits[5:4]	Bits[3:1]	Capacitor	R_pu	R_pd
PS_0[5:1]	1 1	0 0 1	NC	8.45K	2K
PS_1[5:1]	1 1	0 0 0	NC	NC	4.75K
PS_2[5:1]	0 0	0 0 0	680 nF	NC	4.75K
PS_3[5:1]	1 1	X X X	NC	X	X

Mapping to VRAM type please refer to page 04



Security Classification	Compal Secret Data		
Issued Date	2012/11/22	Deciphered Date	2015/11/22

Compal Electronics, Inc.

Title: ATI_Sun Pro_M2_Main_MSIC

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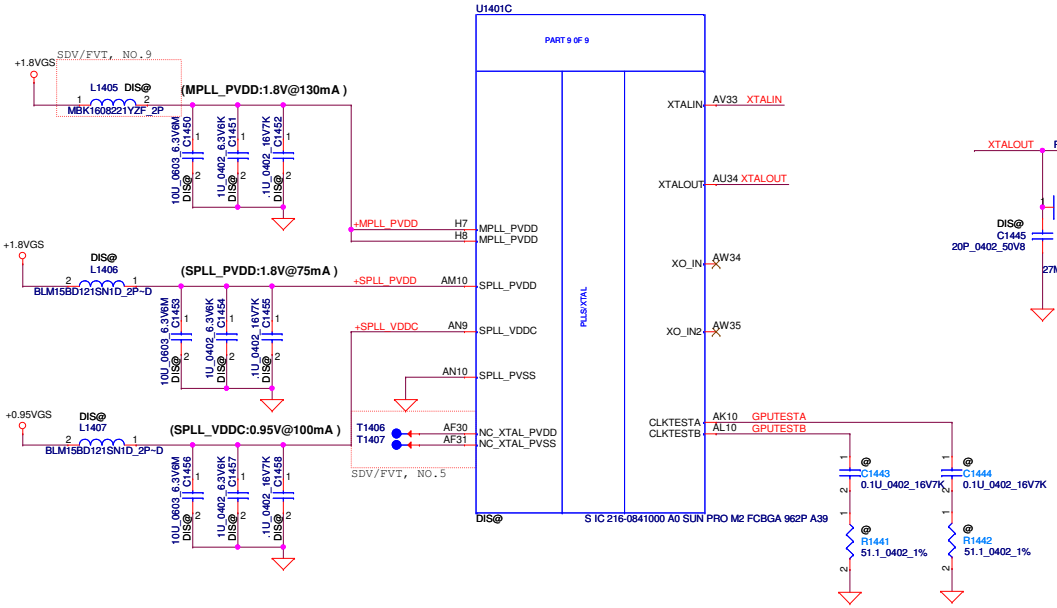
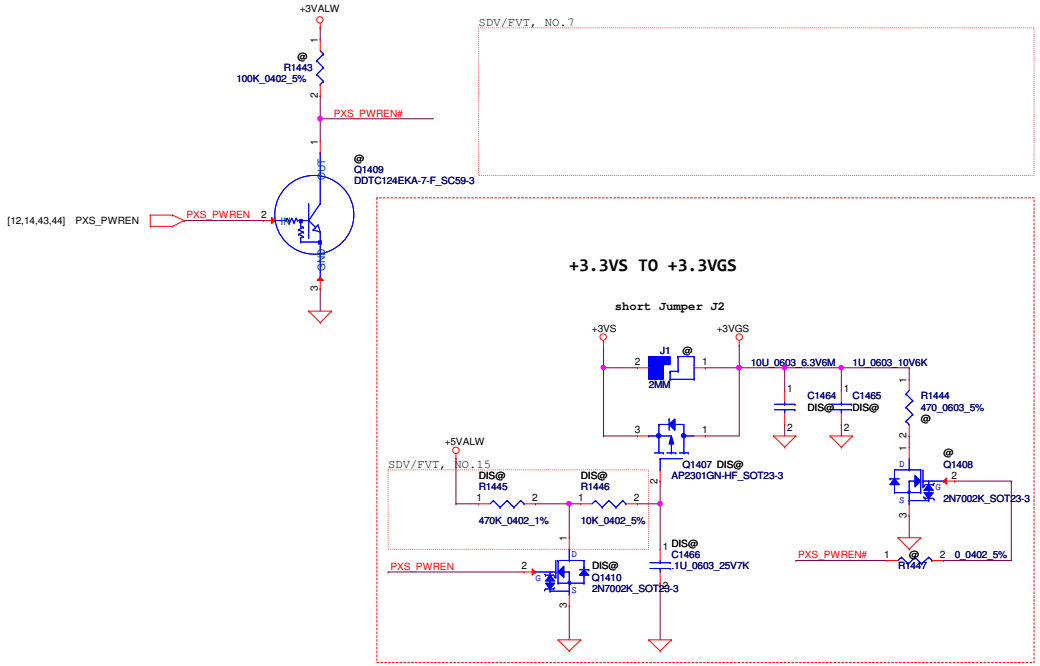
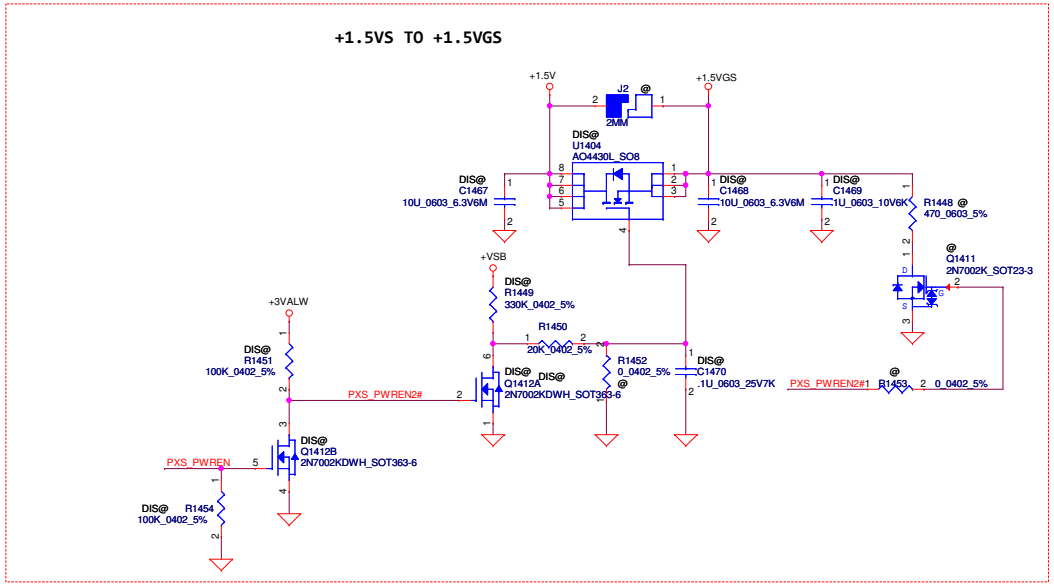
MPLL_PVDD	MarsCRB	Design
220ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

SPLL_PVDD	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

SPLL_VDDC	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1







Security Classification	Compal Secret Data		
Issued Date	2012/11/22	Deciphered Date	2015/11/22

Compal Electronics, Inc.

Title: ATI_Sun Pro_M2_BACO POWER

Size: Custom | Document Number: LA-8127P | Rev: 1.0

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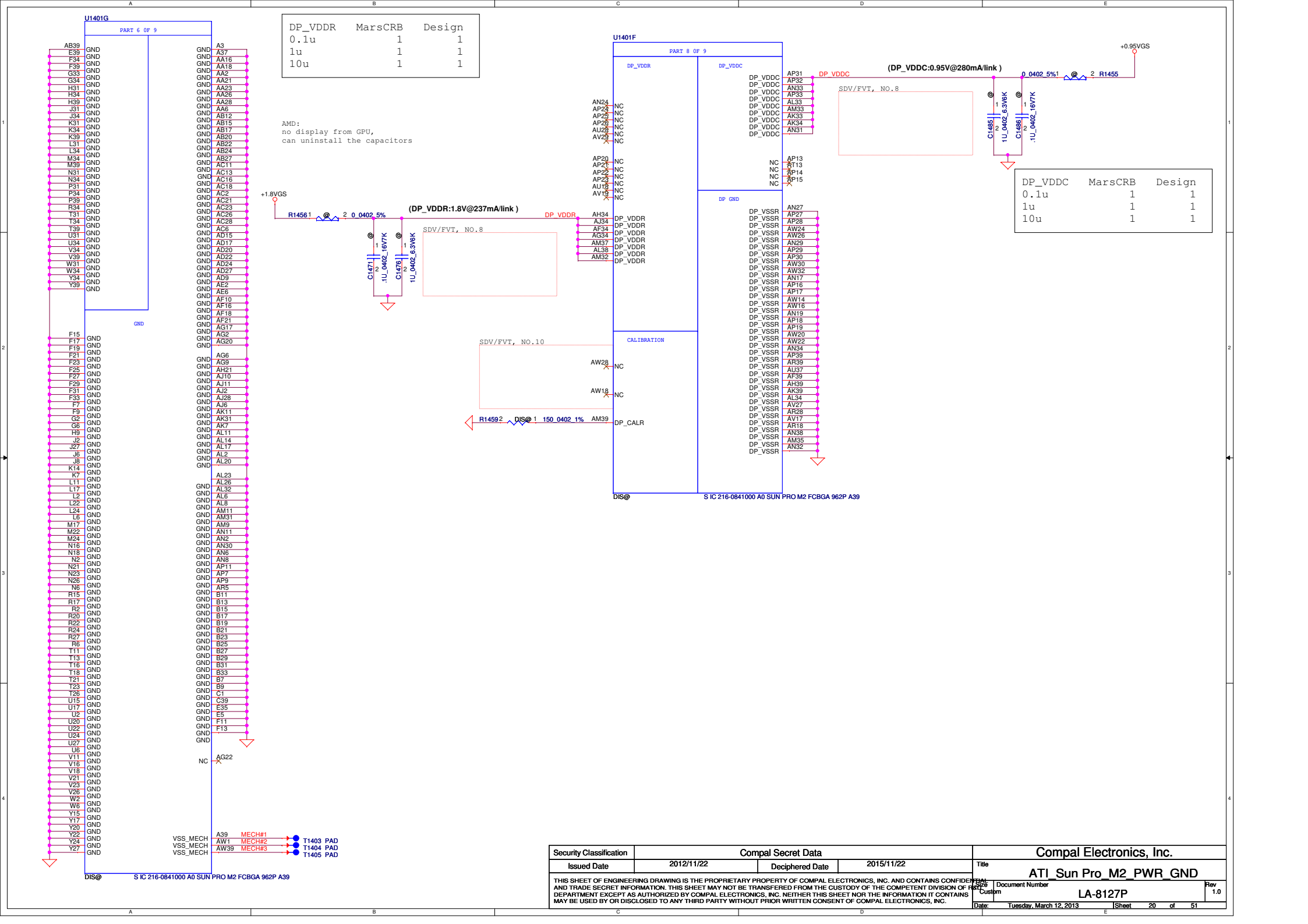

Security Classification	Compal Secret Data		
Issued Date	2012/11/22	Deciphered Date	2015/11/22

Compal Electronics, Inc.

Title: ATI_Sun Pro_M2_PWR_GND

Size: Custom | Document Number: LA-8127P | Rev: 1.0

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For GDDR5, MVDDQ = 1.5V

(VDDR1:1.5V@3A,GDDR5:1125MHz)

VDDR1	MarsCRB	Design
0.01u	5	0
0.1u	5	5
1u	0	5
2.2u	5	0
10u	3	5
220u	0	1

VDD_CT	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	3
10u	1	1

VDDR3	MarsCRB	Design
120ohm	1	0
0.1u	1	0
1u	2	3
10u	0	1

VDDR4	MarsCRB	Design
220ohm	1	1
0.1u	1	1
1u	1	1
10u	1	0

for Sun Pro Ball name AD12,AF11,AF12,AF13,AF15,AG11,AG13,AG15 is NC

Route as differential pair

PCIE_VDDR	MarsCRB	Design
0.1u	0	2
1u	2	3
10u	1	1

PCIE_VDDC	MarsCRB	Design
1u	7	5
10u	2	1

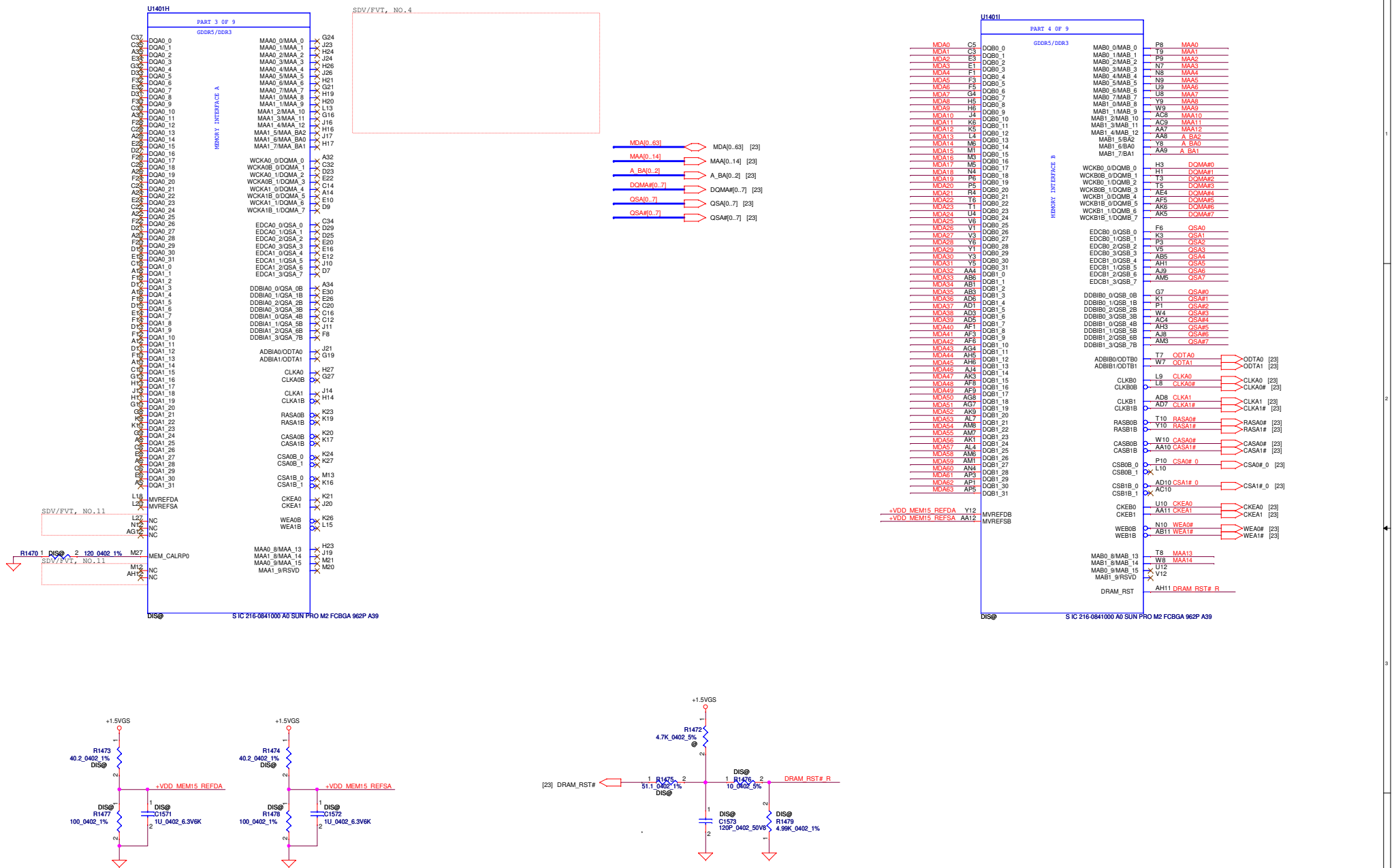
Security Classification	Compal Secret Data		
Issued Date	2012/11/22	Deciphered Date	2015/11/22

Compal Electronics, Inc.

Title: ATI_Sun Pro_M2_Power

Size	Document Number	Rev
C	LA-8127P	1.0

Date: Tuesday, March 12, 2013 Sheet 21 of 51



DRAM_RST# is a daisy-chain net that connects to all VRAM

This basic topology should be used for DRAM_RST for DDR3/GDDR5.These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.
Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

Security Classification	Compal Secret Data		
Issued Date	2012/11/22	Deciphered Date	2015/11/22

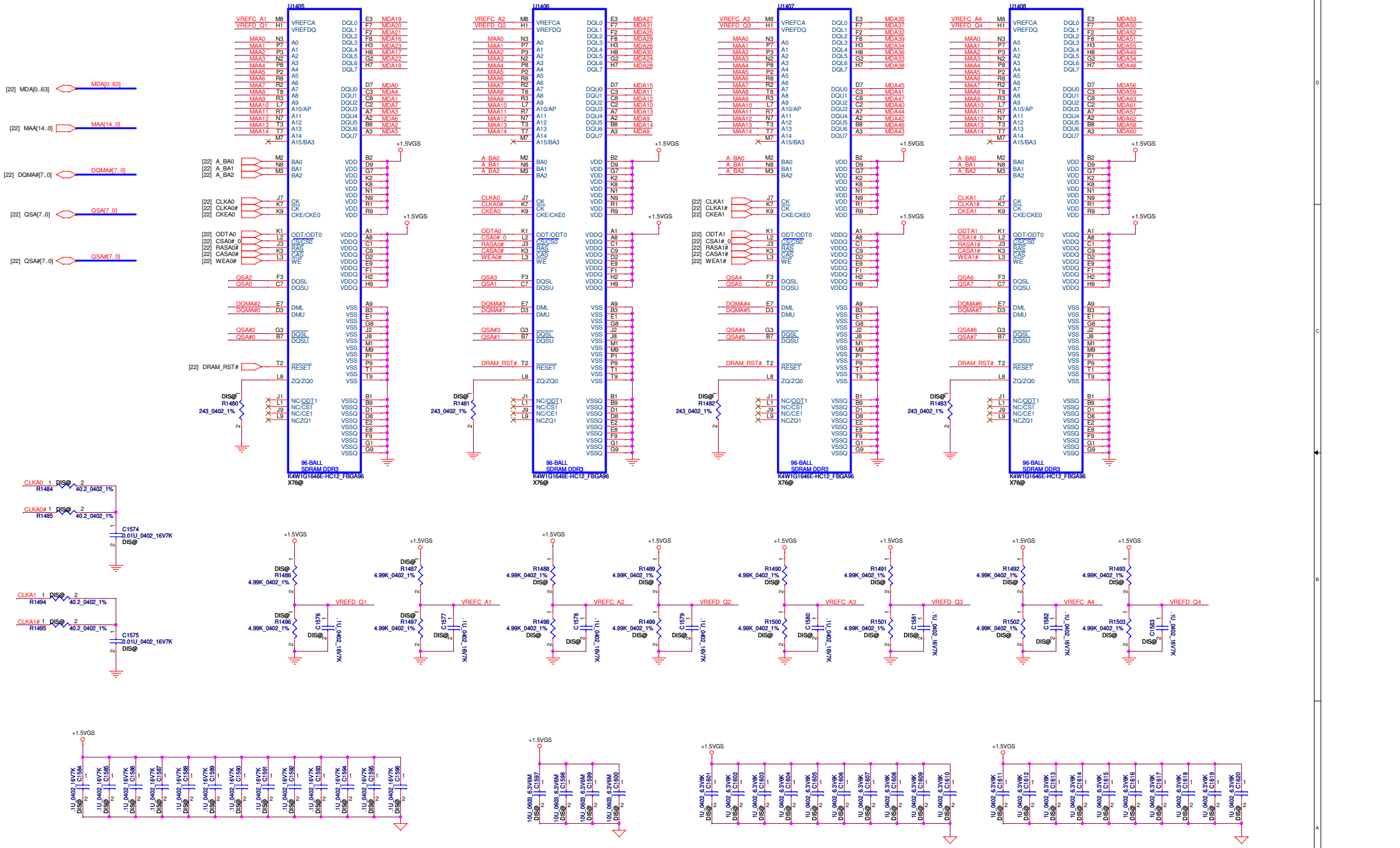
Compal Electronics, Inc.

Title: ATI_Sun Pro_M2_MEM IF

Size	Document Number	Rev
C	LA-8127P	1.0

Date: Tuesday, March 12, 2013 Sheet 22 of 51

The Seymour M2 only support channel B (64 bit),
this page unmount all parts



Security Classification	Compal Secret Data		
Issued Date	2012/11/22	Deciphered Date	2015/11/22

Compal Electronics, Inc.

Title: ATI_Sun_Pro_M2_VRAM_A

Size	Document Number	Rev
C	LA-8127P	1.0

Date: Tuesday, March 12, 2013 Sheet 23 of 51

The Mars Pro M2 only support channel B (64 bit)

SDV/FVT, NO.4

Security Classification	Compal Secret Data		
Issued Date	2012/11/22	Deciphered Date	2015/11/22

Compal Electronics, Inc.

Title: ATI_Sun_Pro_M2_VRAM_B

Size	Document Number	Rev
C	LA-8127P	1.0

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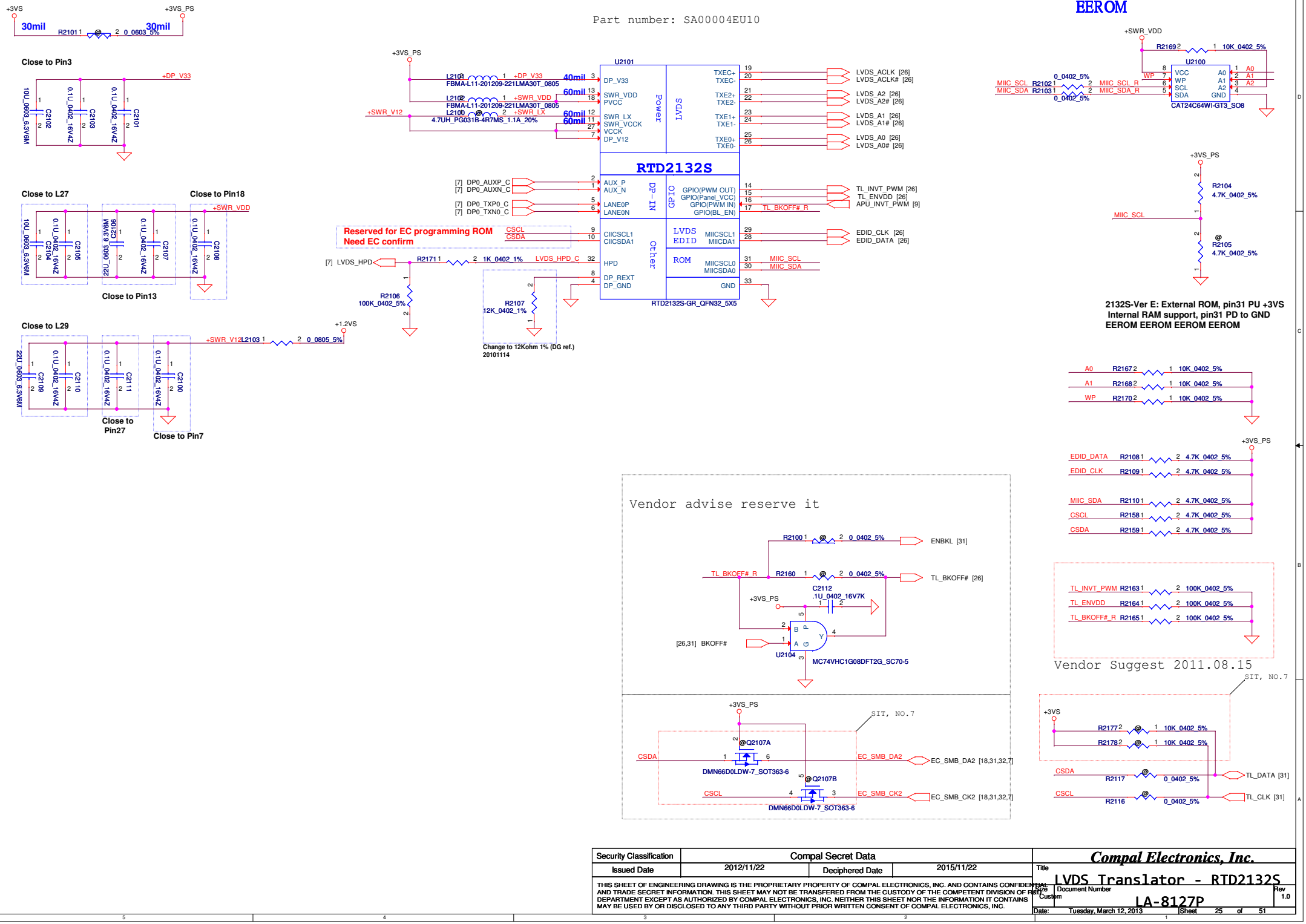
Part number: SA00004EU10

EEROM



Security Classification	Compal Secret Data		
Issued Date	2012/11/22	Deciphered Date	2015/11/22

Compal Electronics, Inc.

Title: LVDS Translator - RTD2132S

Size	Document Number	Rev
Custom	LA-8127P	1.0

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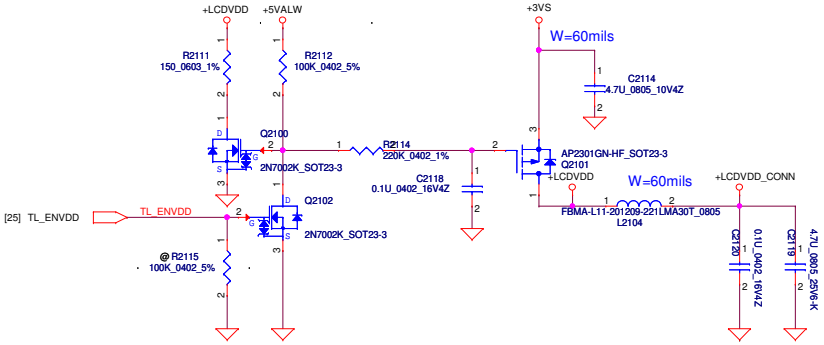
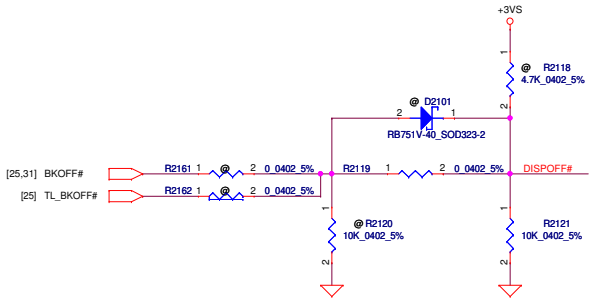
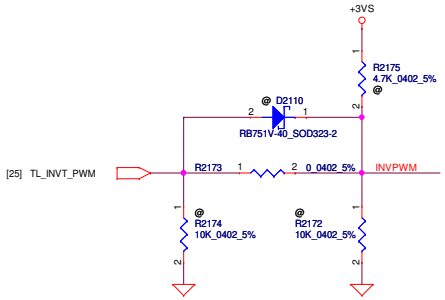
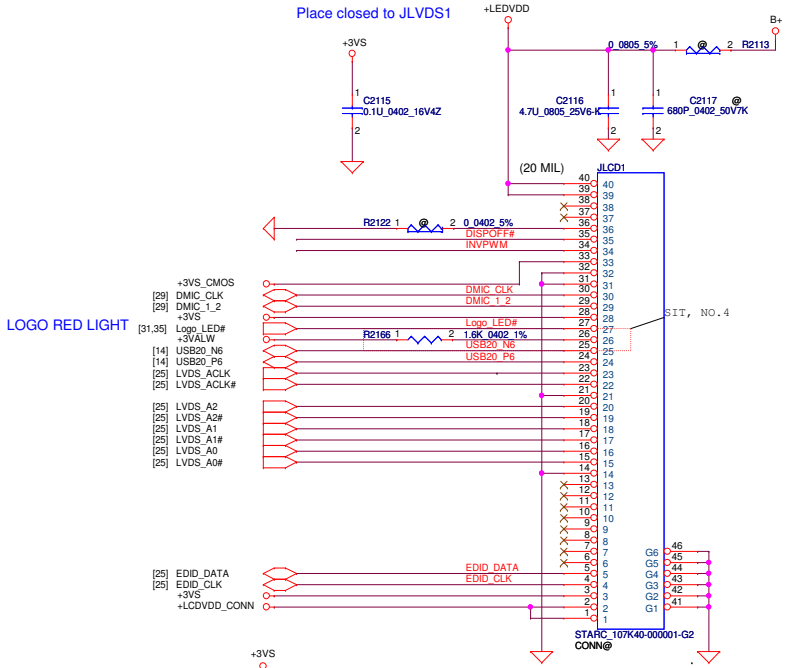
LCD POWER CIRCUIT

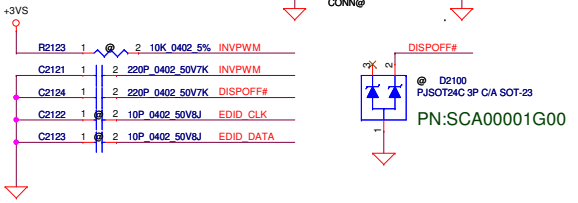


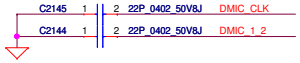




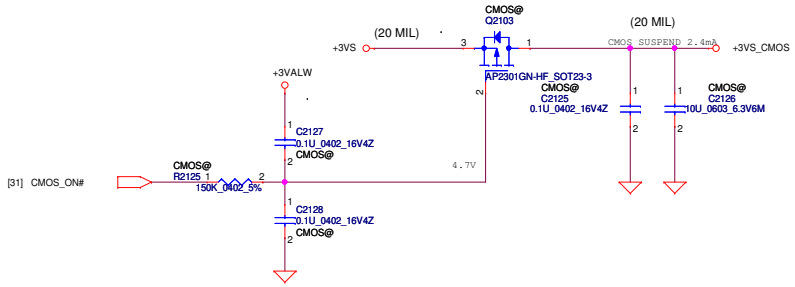
LCD/LED PANEL Conn.







CMOS Camera Conn



Security Classification	Compal Secret Data		
Issued Date	2012/11/22	Deciphered Date	2015/11/22

Compal Electronics, Inc.

Title: LVDS_CONN/CAMERA

Size: Custom | Document Number: LA-8127P | Rev: 1.0

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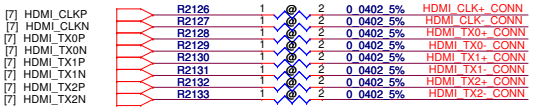
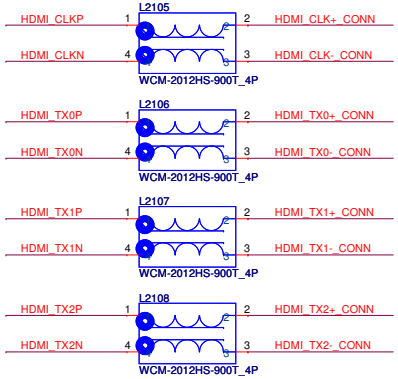
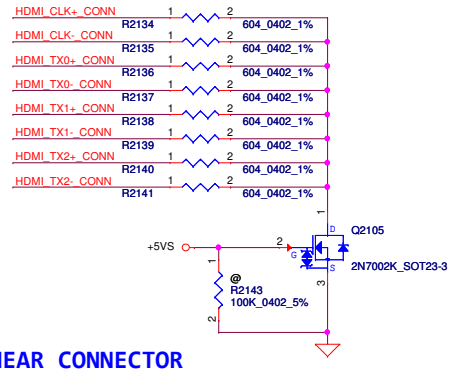
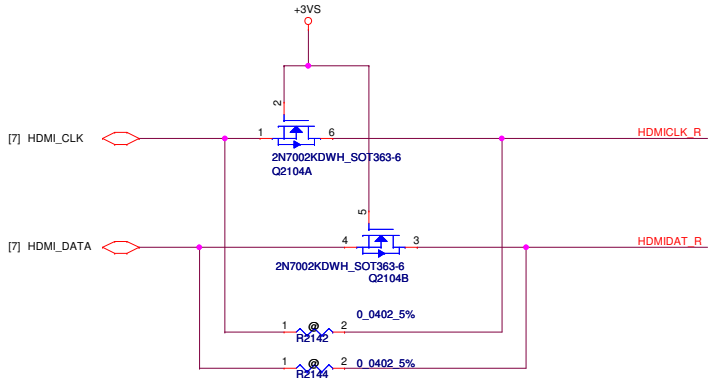
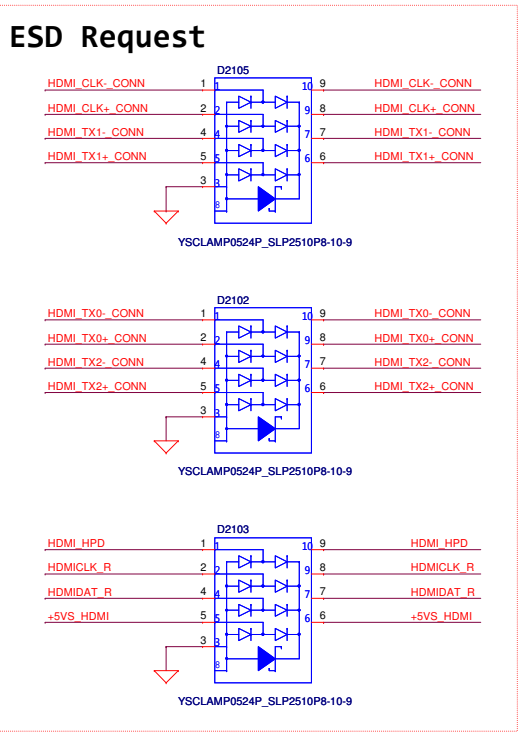
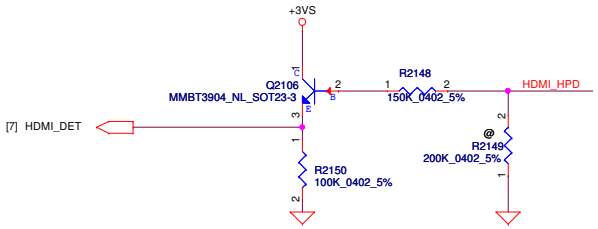


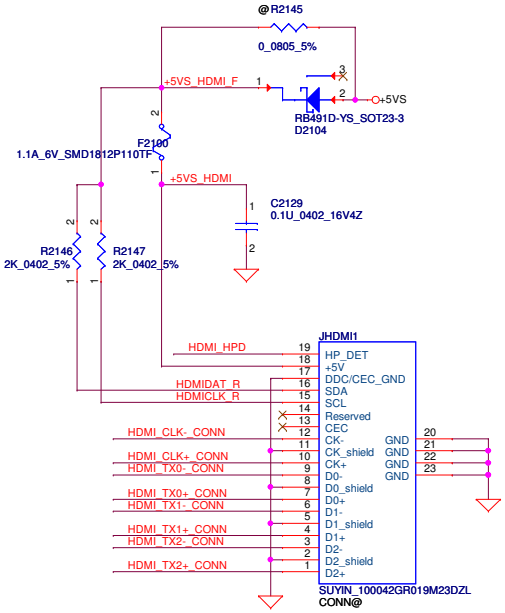










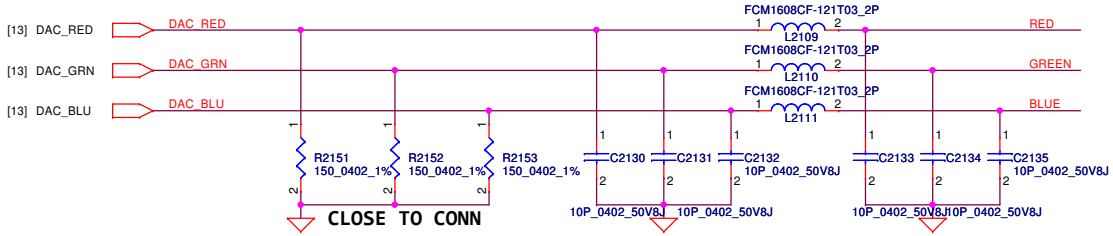


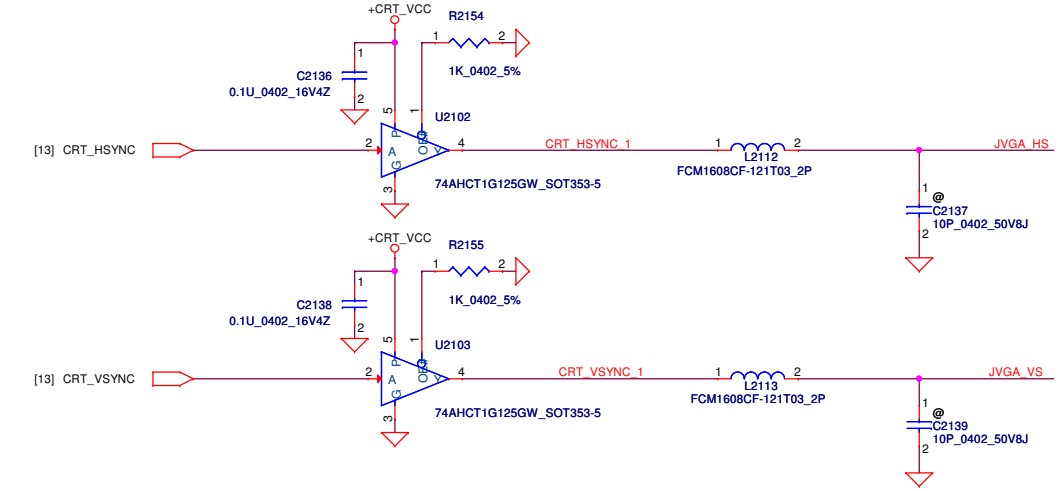
Security Classification	Compal Secret Data		
Issued Date	2012/11/22	Deciphered Date	2015/11/22

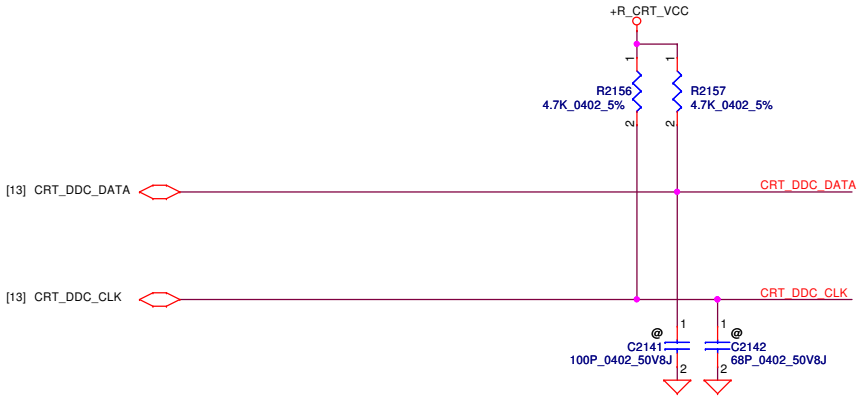
Compal Electronics, Inc.

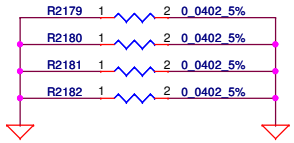
Title: HDMI Connector

Size: Custom	Document Number: LA-8127P	Rev: 1.0
Date: Tuesday, March 12, 2013	Sheet 27 of 51	

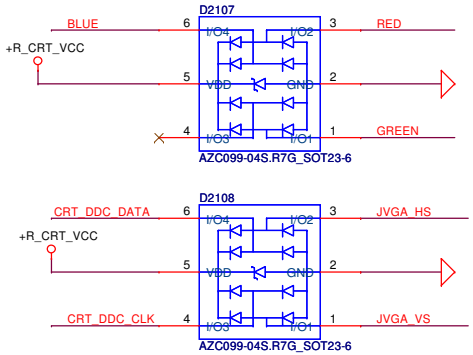




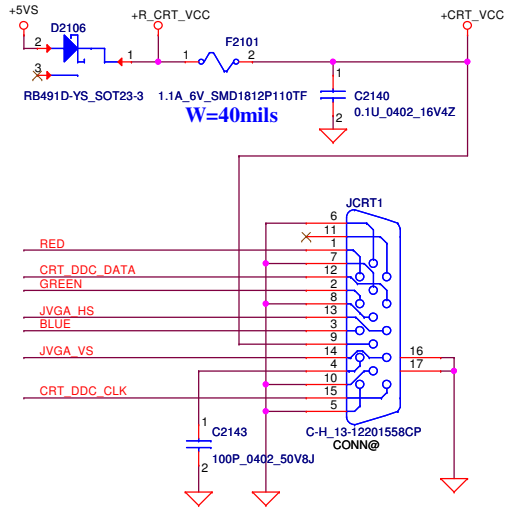




ESD Request



CRT Connector



AMD check list update
20101110

Security Classification	Compal Secret Data		
Issued Date	2012/11/22	Deciphered Date	2015/11/22

Compal Electronics, Inc.

Title: CRT Connector

Size	Document Number	Rev
Custom	LA-8127P	1.0

Date: Tuesday, March 12, 2013 Sheet 28 of 51

CX20671
High Definition Audio Codec SoC
With Integrated Class-D Stereo
Amplifier.
An integrated 5 V to 3.3 V Low-dropout
voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout
voltage regulator (LDO).

Layout Note:Path from +5VS to Pin12, Pin15 must be very low resistance (<0.01 ohms)

To support Wake-on-Jack or Wake-on-Ring, the CODEC VAUX_3.3 & VDD_IO pins must be powerd by a rail that is not removed unless AC power is removed.
*DSH page42 has more detail.

PC Beep

EC Beep [31] BEEP#

ICH Beep [14] FCH_SPKR

D1102 RB751V-40_SOD323-2
C1111 @ 0.1U_0402_16V4Z
C1141 @ 0.1U_0402_16V4Z
D1101 RB751V-40_SOD323-2
R1120 33_0402_5% PC_BEEP_C
C1142 0.1U_0402_16V4Z
PC_BEEP
R1121 10K_0402_5%

Combo Jack detect (normal close)

MIC_JD
Q1103 LBSS138LT1G_SOT-23-3
R1130 33K_0402_5%
EXT_MIC
C1146 1U_0402_6.3V6K
[35] PLUG_IN
CX_GPIO0
R1129 @ 33K_0402_5%
C1147 1U_0402_6.3V6K

Internal DMIC

Internal SPEAKER

potential leakage concern

+5VS
Q1104 BSS138_NL_SOT23-3
[14] HDA_SYNC_AUDIO
HDA_SYNC_AUDIO
R1136 0_0402_5%

Decoupling CAP

+CLASSD_5V
C1115 0.1U_0402_16V4Z
C1117 10U_0603_6.3V6M
C1118 0.1U_0402_16V4Z
C1120 @ 10U_0603_6.3V6M
Near Pin 12
Near Pin 15

EMI

HDA_RST#_AUDIO C1123 @ 22P_0402_50V8J
HDA_SYNC_AUDIO C1126 @ 22P_0402_50V8J
HDA_SDOUT_AUDIO C1128 @ 22P_0402_50V8J
HDA_BITCLK_AUDIO R1123 @ 33_0402_5% HDA_BITCLK_AUDIO_R C1131 @ 22P_0402_50V8J

+3VS
C1121 0.1U_0402_16V4Z @C1119 4.7U_0603_6.3V6K Near Pin 2
C1116 0.1U_0402_16V4Z @C1114 1U_0402_6.3V6K Near Pin 7
C1132 0.1U_0402_16V4Z C1130 4.7U_0603_6.3V6K Near Pin 3

FILT_1.65_R C1135 1U_0402_6.3V6K C1136 0.1U_0402_16V4Z Near Pin 29
+LDO_OUT_3.3V C1133 4.7U_0603_6.3V6K C1134 0.1U_0402_16V4Z Near Pin 27
+5VS C1113 0.1U_0402_16V4Z @C1112 4.7U_0603_6.3V6K Near Pin 28
FILT_1.8_R
+3VS C1124 4.7U_0603_6.3V6K @C1129 0.1U_0402_16V4Z Near Pin 26

10K only needed if supply to VAUX_3.3 is removed during system re-start.

U1101 CX20671-21Z_QFN40_6X6

[14] HDA_RST_AUDIO# R1112 4.7K_0402_5% HDA_RST#_AUDIO
[14] HDA_BITCLK_AUDIO HDA_BITCLK_AUDIO
[14] HDA_SDIN0 R1115 33_0402_5%
[14] HDA_SDOUT_AUDIO HDA_SDOUT_AUDIO

EAPD active low
0=power down ex AMP
1=power up ex AMP

PC_BEEP
[31] EAPD R1111 0_0402_5% CX_GPIO0
[31] EC_MUTE# R1131 0_0402_5%
[26] DMIC_CLK R1138 FBMA-10-100505-301T_2P DMIC_CLK_R
[26] DMIC_1_2 R1139 0_0402_5% DMIC_1_2_R
SPK_L2+ SPK_L1-
SPK_R2+ SPK_R1-

Near Pin 17
LPWR_5.0 RPWR_5.0 CLASS-D_REF C1107 0.1U_0402_16V4Z +CLASSD_5V R1137 0_0805_5% +5VS
SENSE_A R1113 5.11K_0402_1% R1114 20K_0402_1% R1116 39.2K_0402_1% MIC_JD PLUG_IN +3VS
PORTB_R PORTB_L B_BIAS C1108 2.2U_0603_6.3V6K R1133 100_0402_1% EXT_MIC +MICBIASB
C_BIAS PORTC_R PORTC_L EXT_MIC R1132 2K_0402_5% R1128 4.7K_0402_5%
PORTA_R PORTA_L HP_OUTR_R R1117 39_0402_5% HP_OUTR HP_OUTR [35]
HP_OUTL_R R1118 39_0402_5% HP_OUTL HP_OUTL [35]
NC NC NC
AVEE FLY_P FLY_N C1110 1U_0603_10V4Z
C1122 0.1U_0402_16V4Z C1125 4.7U_0603_6.3V6K Near Pin 21

Sense resistors must be connected same power that is used for VAUX_3.3

Port B
Port A
External MIC
EXT_MIC [35]
Headphone

Changed from 5.1ohm to 15ohm for "zi zi"noise.

Rdc < 0.05 ohms
Rated Current > 2A

Internal Speaker

Width 20 mil

[31] SPK_RT_Detect#
SPK_R1- L1102 0_0603_5% SPK_R1-_CONN
SPK_R2+ L1103 0_0603_5% SPK_R2+_CONN
SPK_L1- L1104 0_0603_5% SPK_L1-_CONN
SPK_L2+ L1105 0_0603_5% SPK_L2+_CONN
SPK_RT_Detect# R1140 0_0402_5% SPK_RT_Detect#_R

JSPK1 E-T_4070K-G06N-00L CONN@
GND GND

EMI
@C1137 1000P_0402_50V7K
@C1138 1000P_0402_50V7K
@C1139 1000P_0402_50V7K
@C1140 1000P_0402_50V7K

Note.
QALEA 14" => JSPK1 => 4Pin
QALEB 15" => JSPK1 => 6Pin

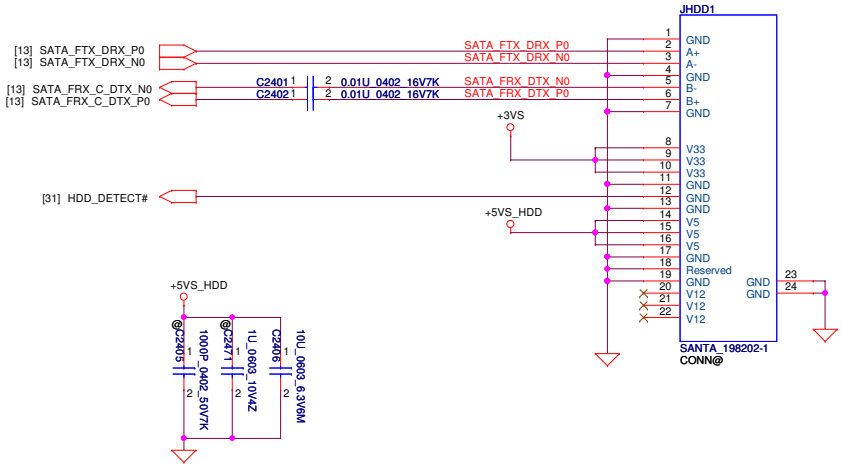
EMI

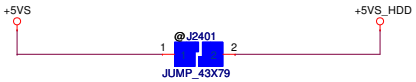
C1102 @ 0.1U_0402_16V4Z
C1103 @ 0.1U_0402_16V4Z
C1104 @ 0.1U_0402_16V4Z
R1102 @ 0_0402_5%
R1104 @ 0_0402_5%
R1105 @ 0_0402_5%
GND GND GNDA

Security Classification	Compal Secret Data		
Issued Date	2012/11/22	Deciphered Date	2015/11/22

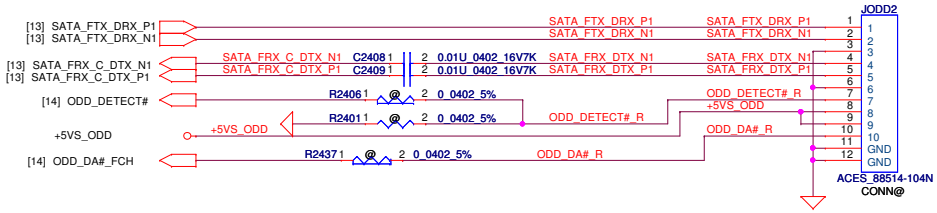
Compal Electronics, Inc.
Title: HD Audio Codec CX20671
Size: Custom | Document Number: LA-8127P | Rev: 1.0
Date: Tuesday, March 12, 2013 | Sheet 29 of 51

SATA HDD Conn.



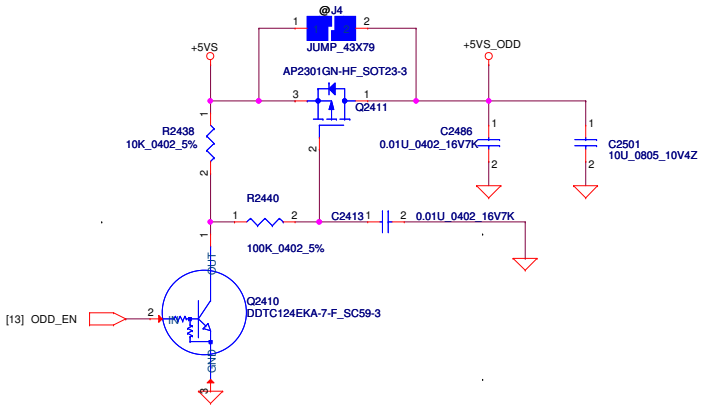


SATA ODD Conn.

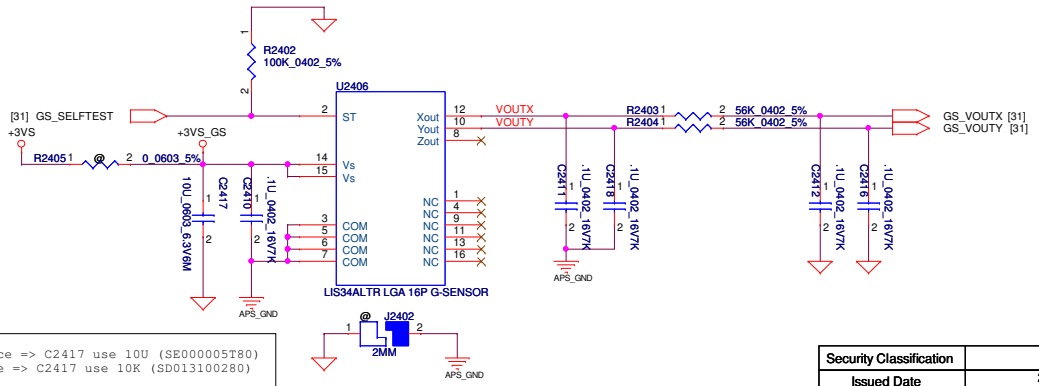


Note.
QALEA 14" => JODD1
QALEB 15" => JODD2

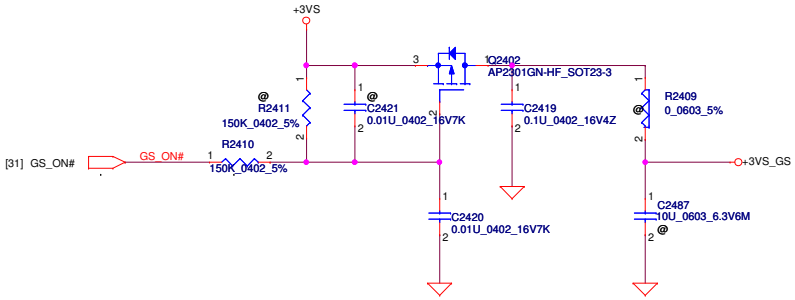
ODD Power Control



APS G-Sensor



Note.
Main Source => C2417 use 10U (SE000005T80)
2nd Source => C2417 use 10K (SD013100280)



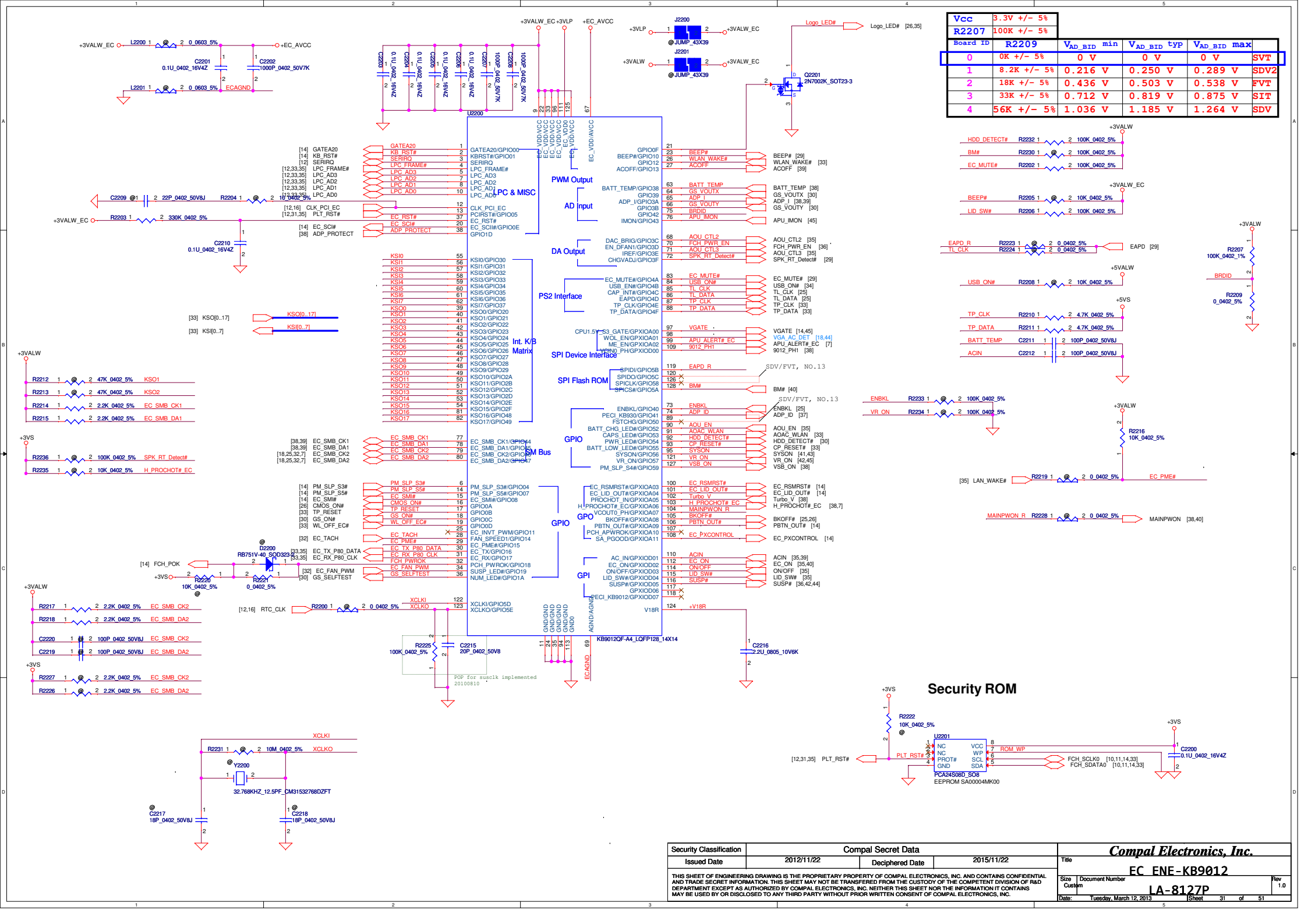
Security Classification	Compal Secret Data		
Issued Date	2012/11/22	Deciphered Date	2015/11/22

Compal Electronics, Inc.

Title: HDD/ODD/G-Sensor

Size	Document Number	Rev
B	LA-8127P	1.0

Date: Tuesday, March 12, 2013 | Sheet 30 of 51



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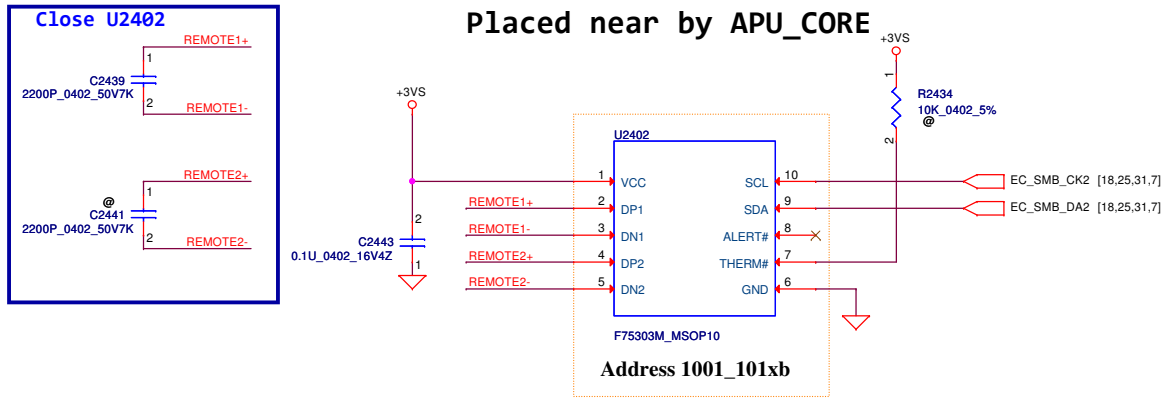
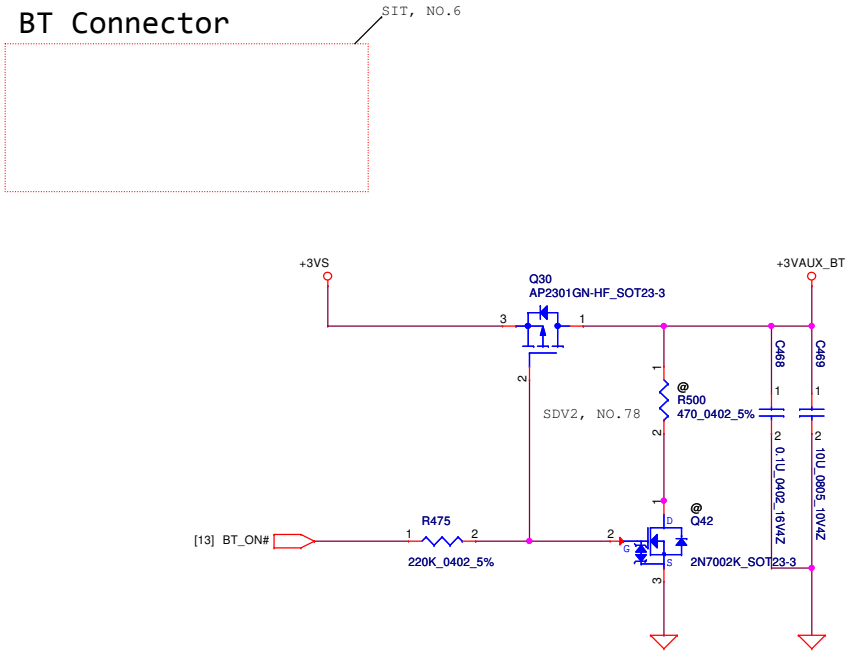
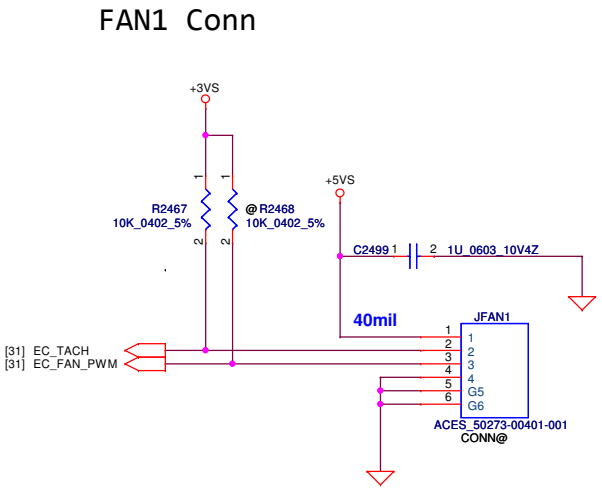






Security Classification	Compal Secret Data		
Issued Date	2012/11/22	Deciphered Date	2015/11/22

Compal Electronics, Inc.

Title: Thermal/FAN/BT

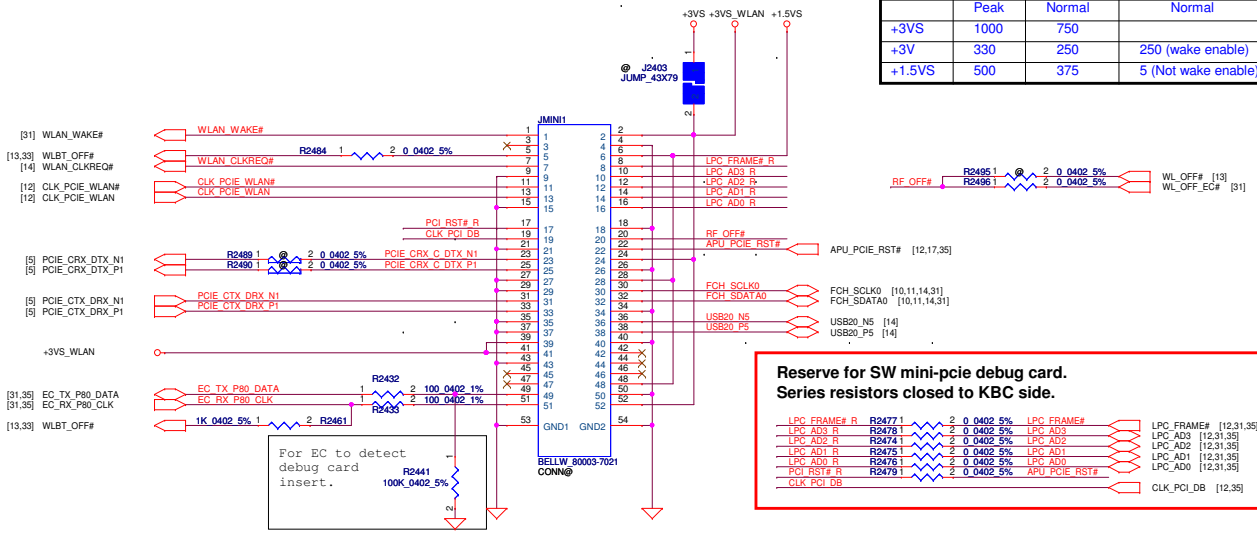
Size	Document Number	Rev
B	LA-8127P	1.0

Date: Tuesday, March 12, 2013 Sheet 32 of 51

WLAN Conn

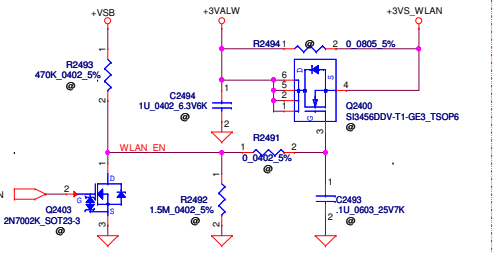
Mini Card Power Rating

Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)



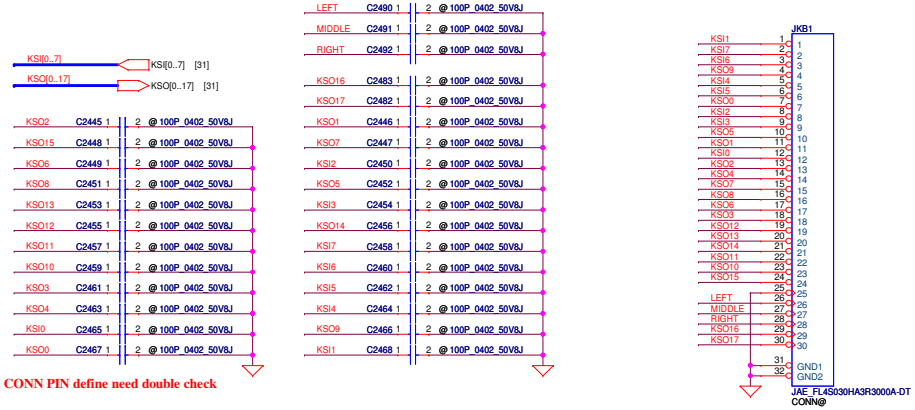
Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.

AOAC function



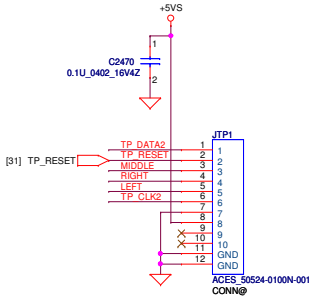
For AOAC assessment
+3VS_WLAN path:
1. +3VS (default)
2. +3VALW
3. +3VALW + Switch

INT_KBD Conn.

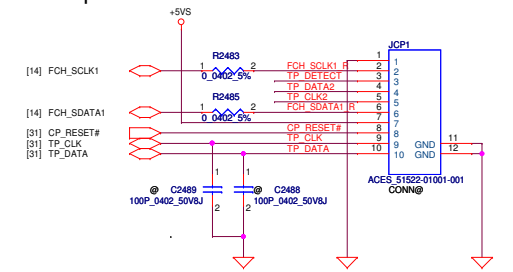


CONN PIN define need double check

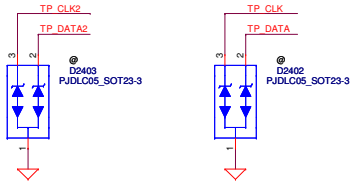
Track Point Conn

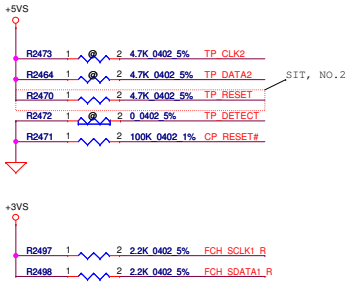


Click pad 10PIN

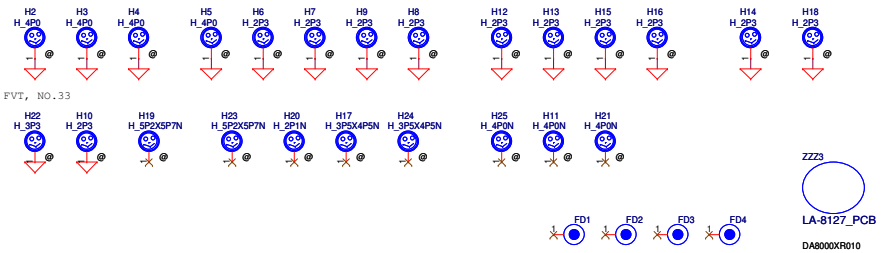


ESD Request





Screw Holes



ZZZ3
LA-8127_PCB
DA8000XR010

Security Classification	Compal Secret Data		
Issued Date	2012/11/22	Deciphered Date	2015/11/22

Compal Electronics, Inc.

Title: TP/KBD/Screw Hole/Debug

Size: C | Document Number: LA-8127P | Rev: 1.0

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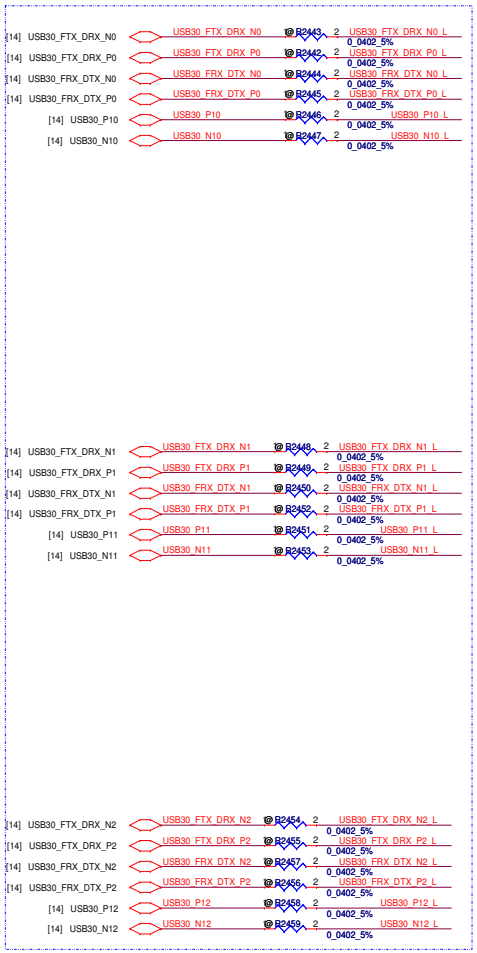
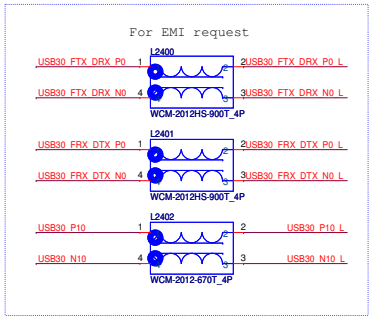
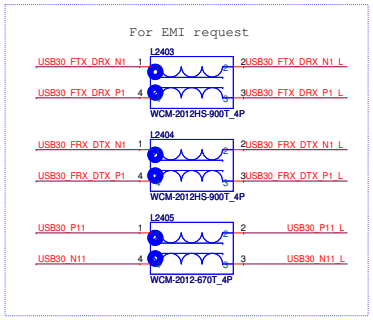
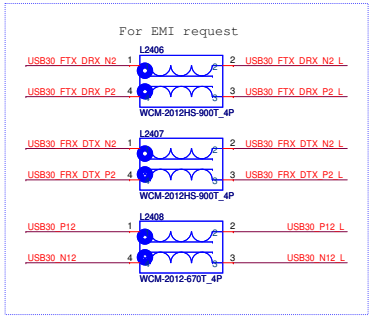
USB3.0 Conn *3

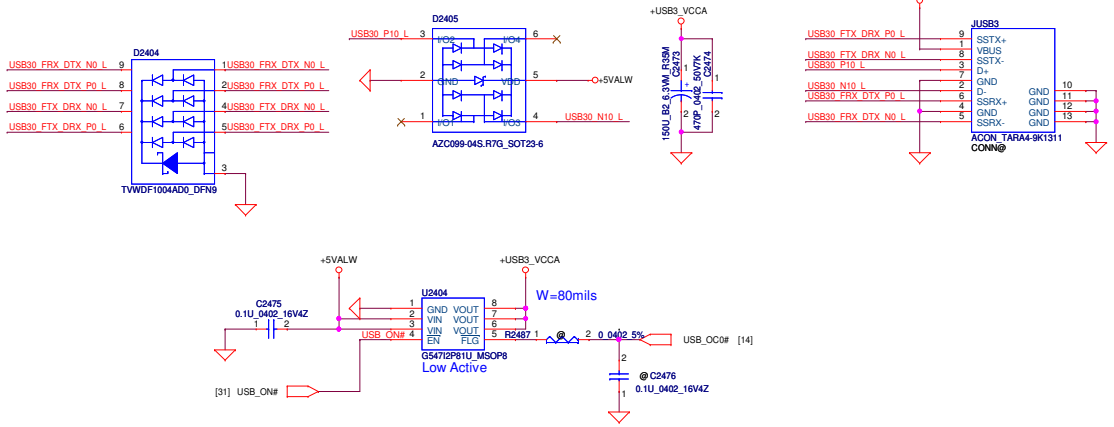




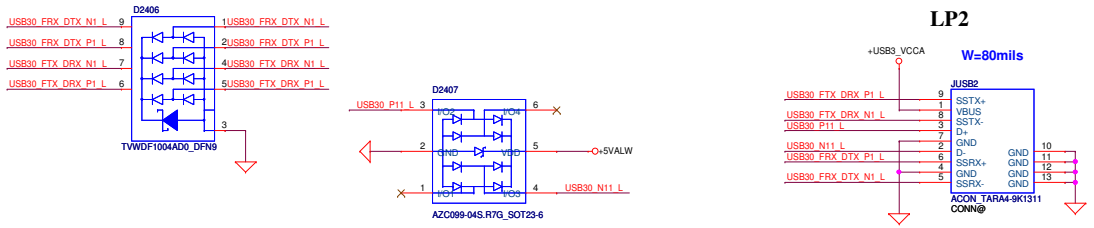


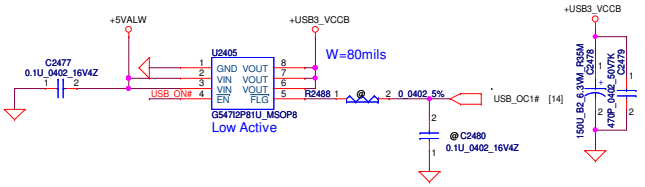


LP1

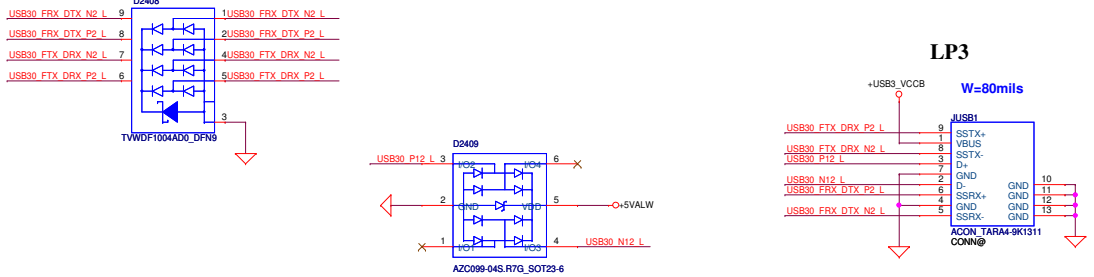


LP2





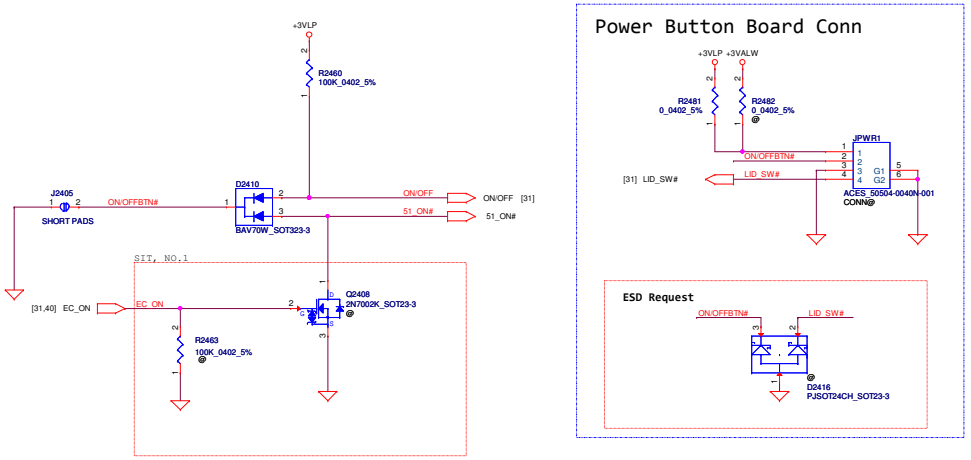
LP3



Security Classification	Compal Secret Data		
Issued Date	2012/11/22	Deciphered Date	2015/11/22

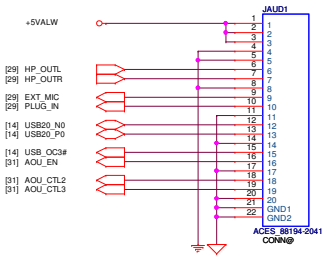
Compal Electronics, Inc.			
Title: USB 3.0 Conn			
Size: C	Document Number: LA-8127P		Rev: 1.0
Date: Tuesday, March 12, 2013		Sheet 34 of 51	

ON/OFF switch

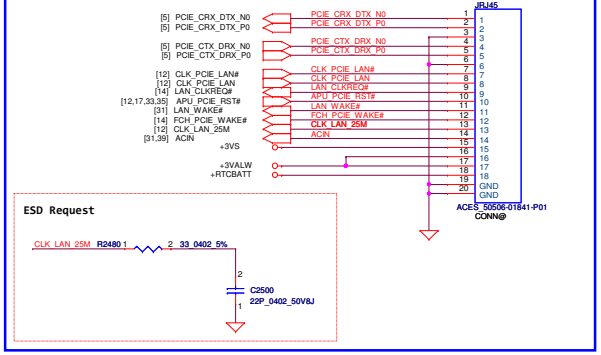


Power Button Board Conn

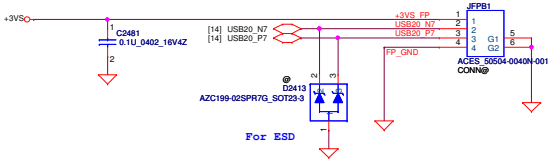
USB2.0/Audio Jack SB CONN



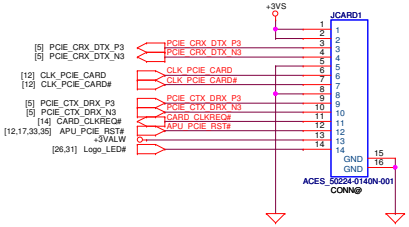
Lan Conn



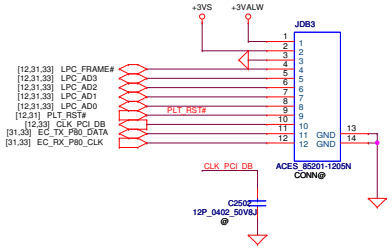
Finger Printer



Card Reader

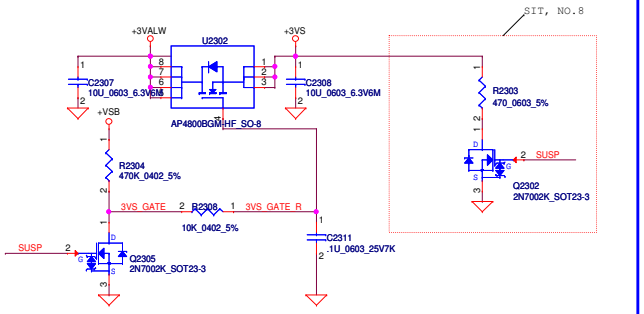


Debug Conn.

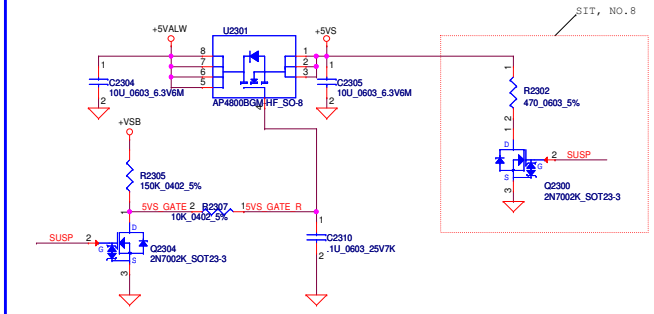


Compal Electronics, Inc.			
Title	Sub Board		
Size	Document Number		Rev
Custom	LA-8127P		1.0
Date:	Tuesday, March 12, 2013	Sheet	35 of 51

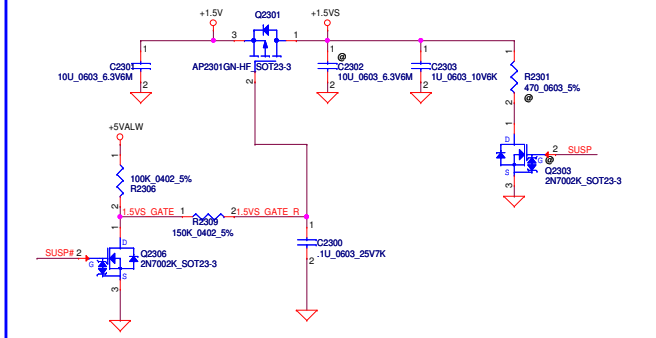
+3VALW TO +3VS



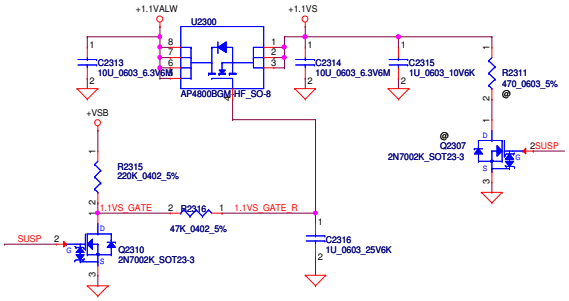
+5VALW TO +5VS



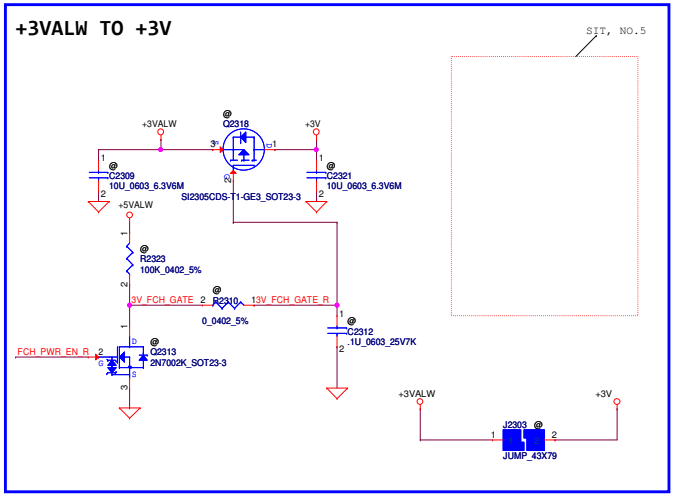
+1.5V to +1.5VS



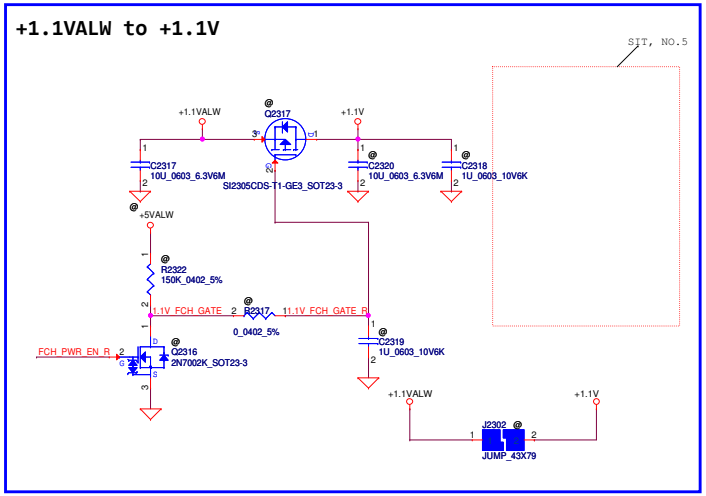
+1.1VALW to +1.1VS

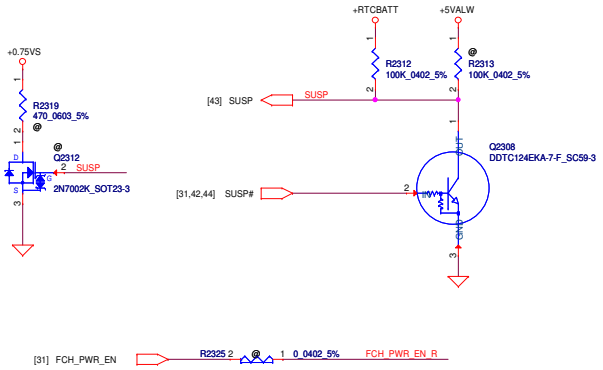


+3VALW TO +3V



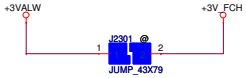
+1.1VALW to +1.1V





+3VALW TO +3V_FCH

Short J2301 for PCH VCCSUS3.3



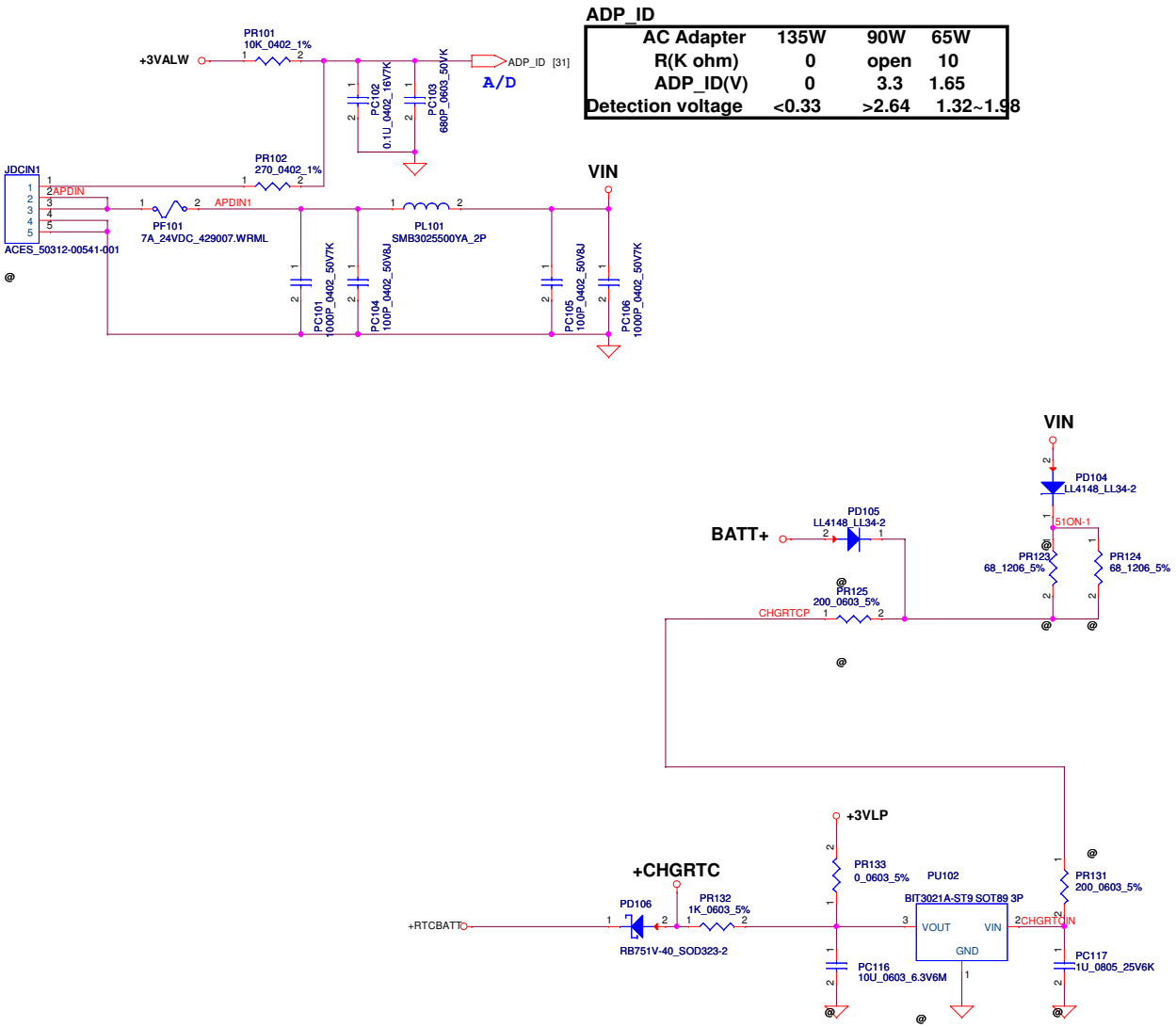
Security Classification	Compal Secret Data		
Issued Date	2012/11/22	Deciphered Date	2015/11/22

Compal Electronics, Inc.

Title: DC_V_TO_VS_INTERFACE

Size	Document Number	Rev
C	LA-8127P	1.0

Date: Tuesday, March 12, 2013 Sheet 36 of 51



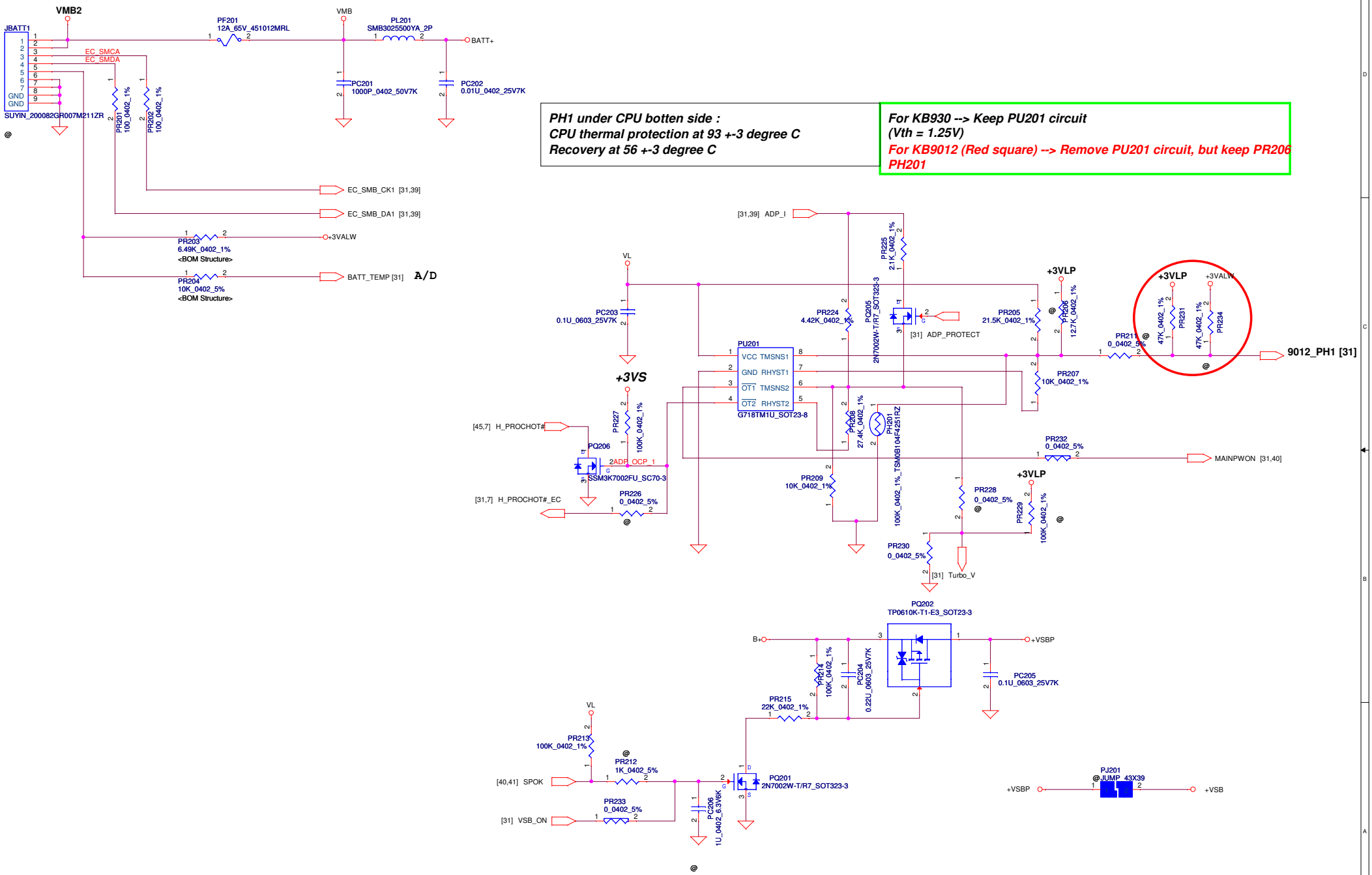
Security Classification	Compal Secret Data		
Issued Date	2011/04/18	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: PWR DCIN / Vin Detector /Pre-charge

Size: Custom | Document Number | Rev: 1.0

Date: Tuesday, March 12, 2013 | Sheet 37 of 51



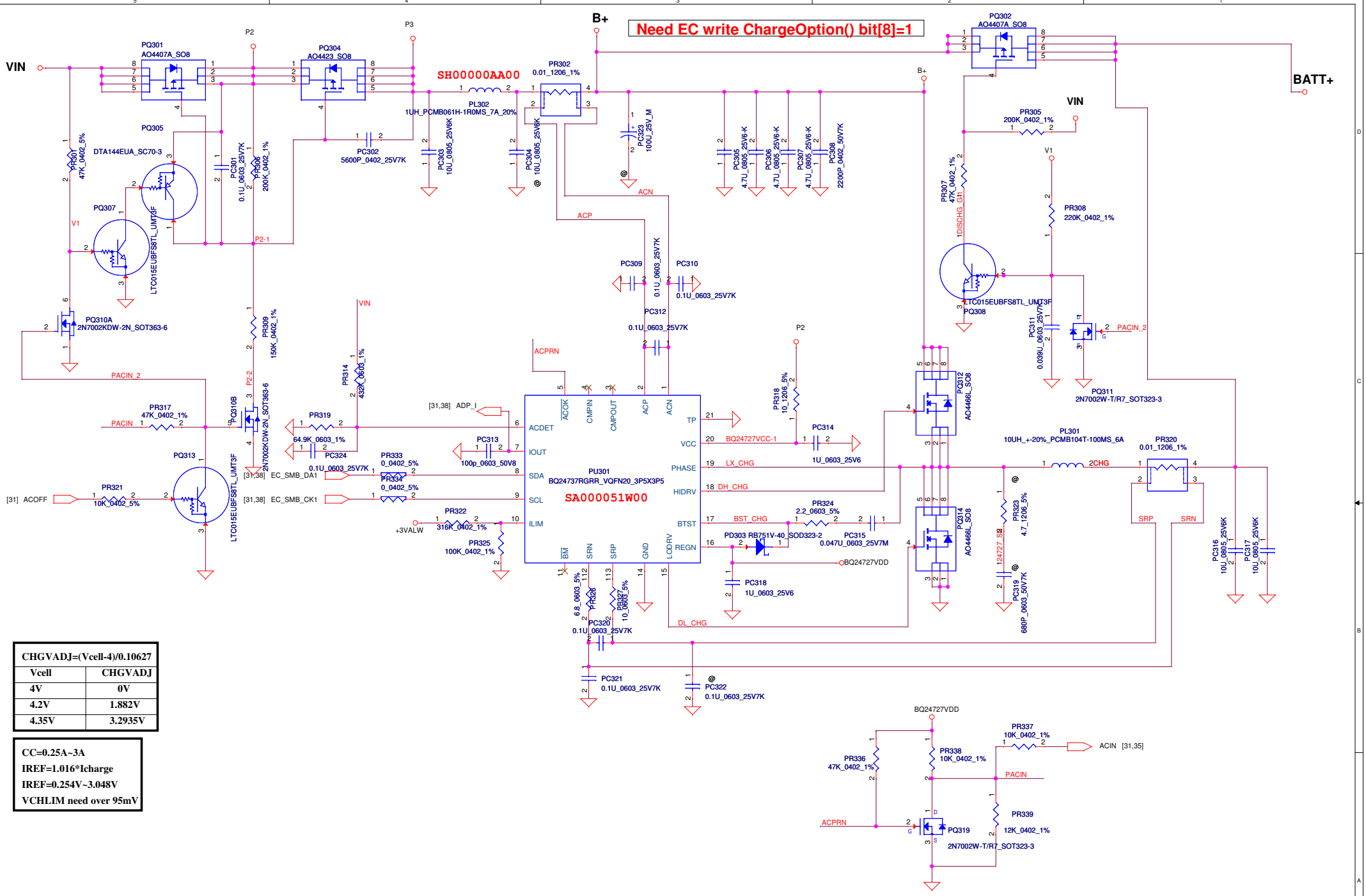
Security Classification	Compal Secret Data		
Issued Date	2011/04/18	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: PWR-BATTERY CONN/OTP

Size: Custom | Document Number | Rev: 1.0

Date: Tuesday, March 12, 2013 | Sheet 38 of 51



CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CC=0.25A~3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

Security Classification	Compal Secret Data		
Issued Date	2011/04/18	Deciphered Date	2015/07/08

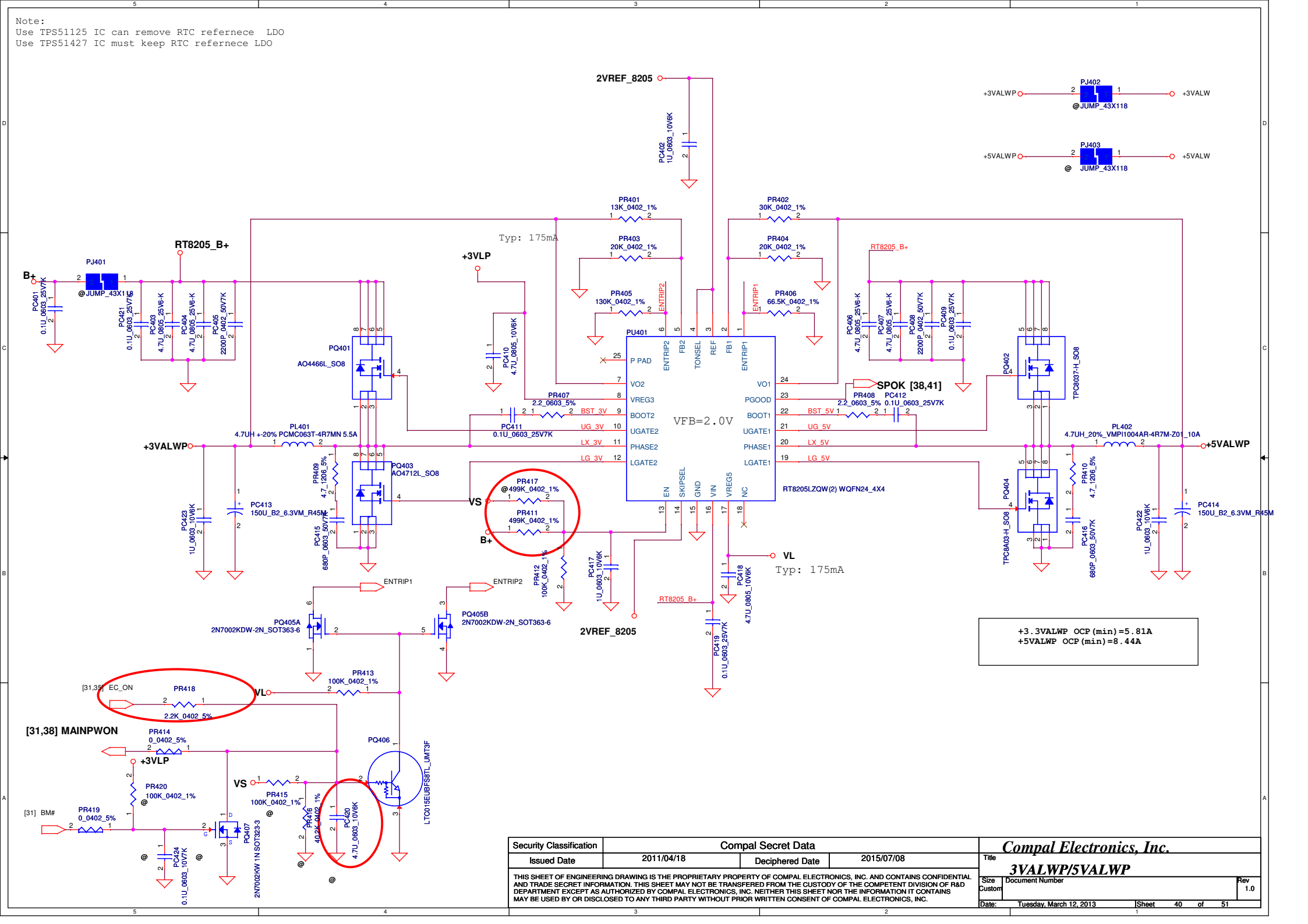
Compal Electronics, Inc.

Title: CHARGER

Size | Document Number | Rev 1.0

Date: Tuesday, March 12, 2013 | Sheet 39 of 51

Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO



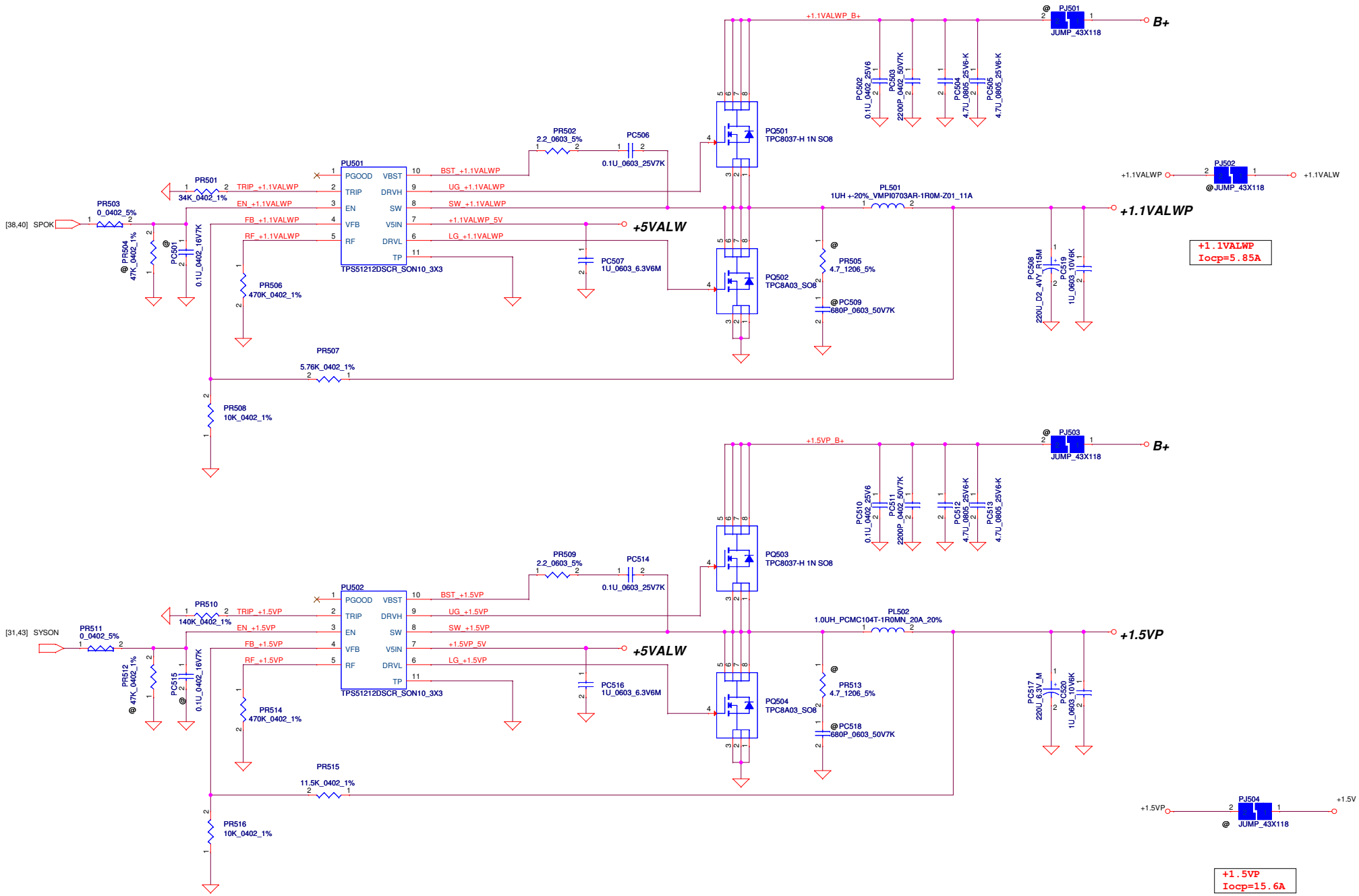
Security Classification	Compal Secret Data		
Issued Date	2011/04/18	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: 3VALWP/5VALWP

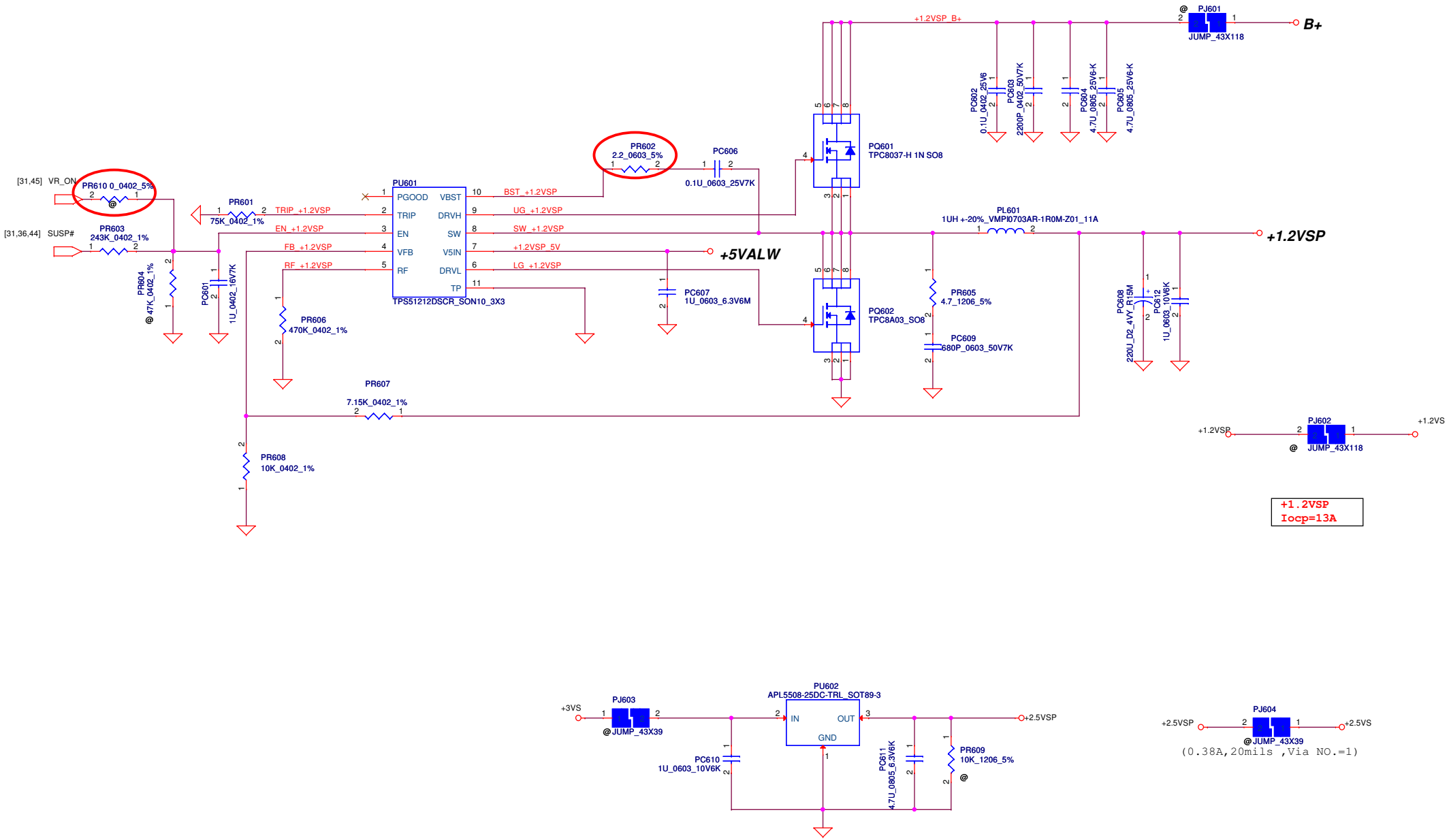
Size	Document Number	Rev
Custom		1.0

Date: Tuesday, March 12, 2013 Sheet 40 of 51



Security Classification	Compal Secret Data		
Issued Date	2011/04/18	Deciphered Date	

Compal Electronics, Inc.			
Title: +1.1VALWP/+1.5VP			
Size:	Document Number		Rev: 1.0
Date: Tuesday, March 12, 2013	Sheet 41 of 51		



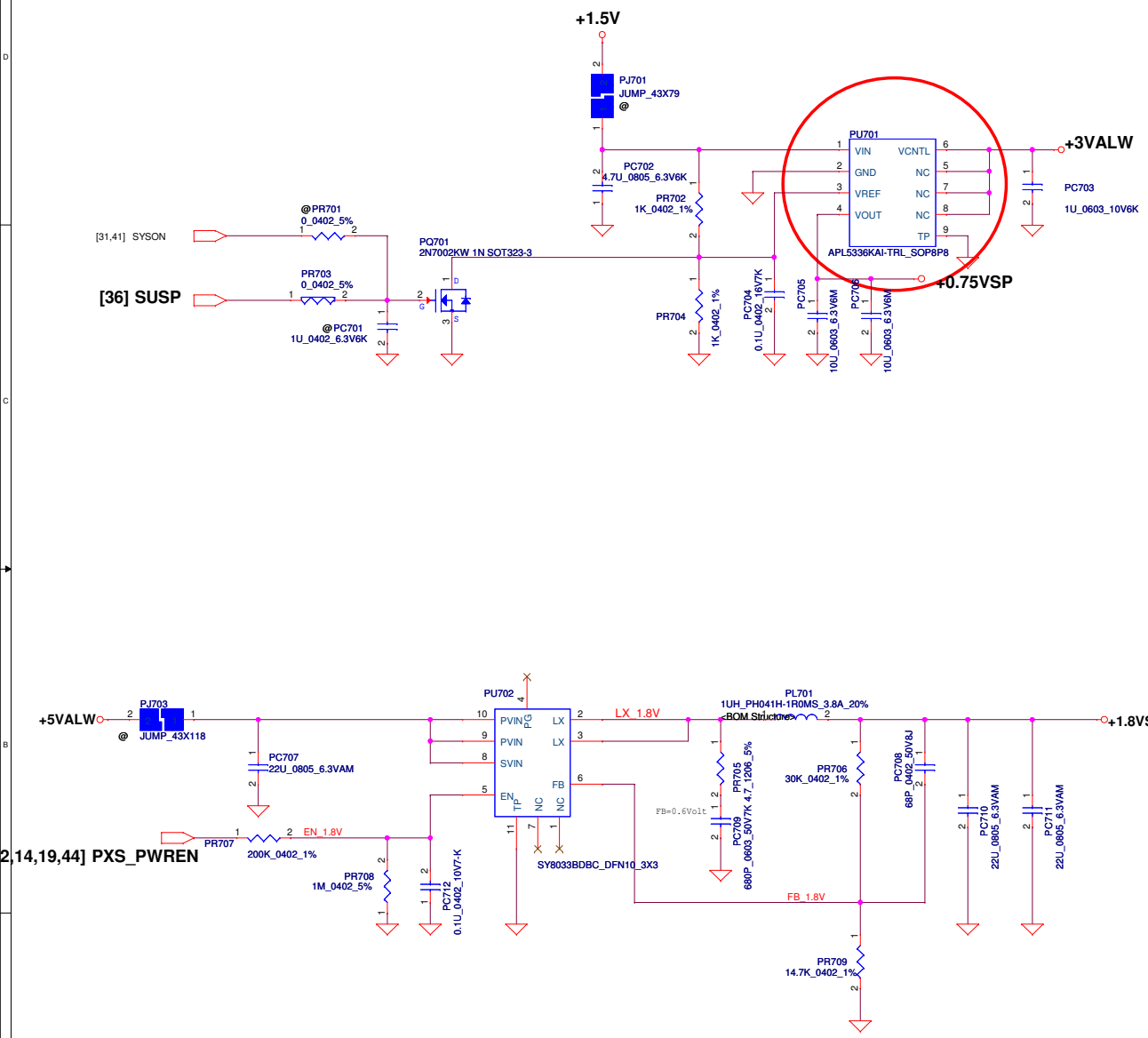
Security Classification	Compal Secret Data		
Issued Date	2011/04/18	Deciphered Date	

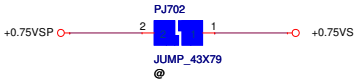
Compal Electronics, Inc.

Title: **+1.2VSP/+2.5VSP**

Size	Document Number	Rev
		1.0

Date: Tuesday, March 12, 2013 | Sheet 42 of 51





Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/04/18	Deciphered Date	Title: +0.75VP/+1.8VP

Size	Document Number		Rev 1.0
Date: Tuesday, March 12, 2013	Sheet 43 of 51		

GPIO21	GPIO29	GPIO30	GPIO20	GPIO15	
VID5	VID4	VID3	VID2	VID1	VDDC
0	1	1	1	1	1.125V
1	0	0	0	0	1.100V
1	0	0	0	1	1.075V
1	0	0	1	0	1.050V
1	0	0	1	1	1.025V
1	0	1	0	0	1.000V
1	0	1	0	1	0.975V
1	0	1	1	0	0.950V
1	0	1	1	1	0.925V
1	1	0	0	0	0.900V
1	1	0	0	1	0.875V
1	1	0	1	0	0.850V
1	1	0	1	1	0.825V
1	1	1	0	0	0.800V
1	1	1	0	1	0.775V

Default

Layout Note:
Place near Phase1 Choke

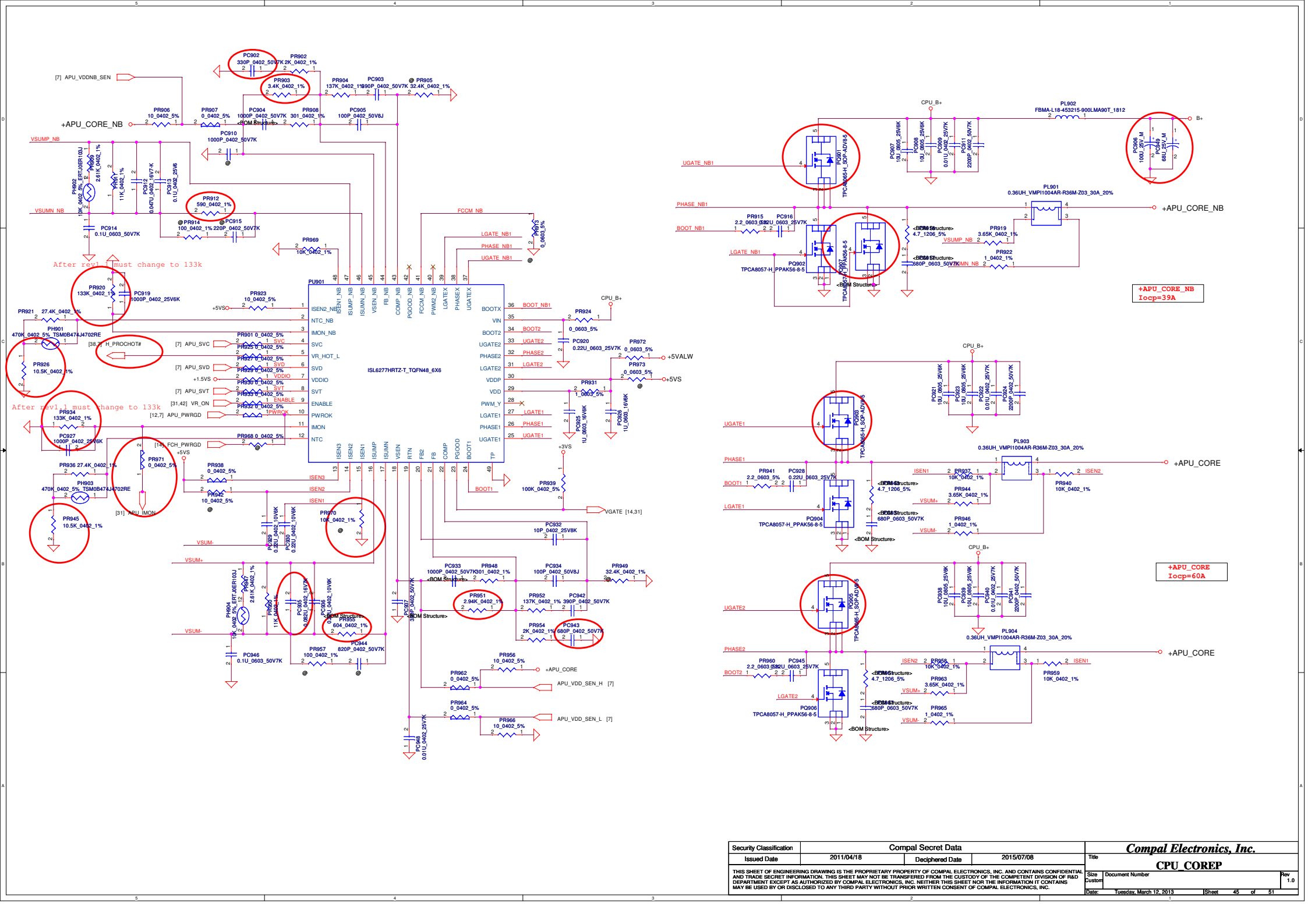
Security Classification	Compal Secret Data		
Issued Date	2012/07/03	Deciphered Date	2013/07/03

Compal Electronics, Inc.

Title: VGA_COREP

Size	Document Number	Rev
		1.0

Date: Tuesday, March 12, 2013 | Sheet 44 of 51



Security Classification	Compal Secret Data		
Issued Date	2011/04/18	Deciphered Date	2015/07/08

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Compal Electronics, Inc.

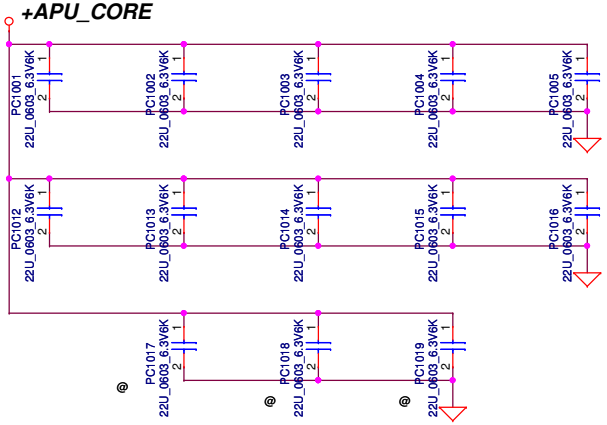
Title: **CPU_COREP**

Size	Document Number	Rev
Custom		1.0

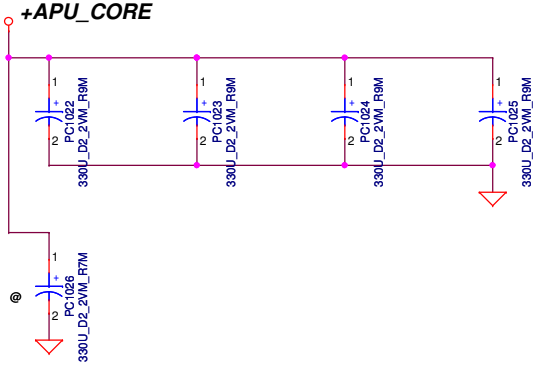
Date: Tuesday, March 12, 2013 Sheet 45 of 51

+CPU_CORE

+APU_CORE

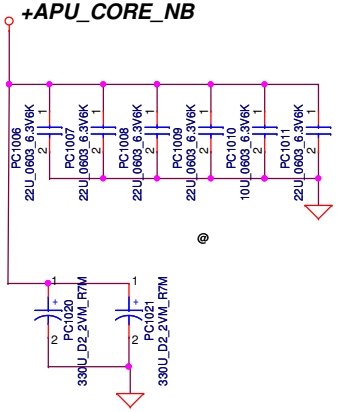


+APU_CORE



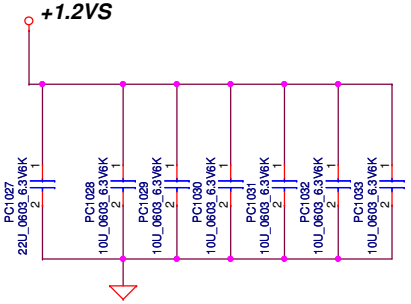
+CPU_CORE_NB

+APU_CORE_NB



+1.2VS

+1.2VS



+1.2VS

Security Classification	Compal Secret Data		
Issued Date	2011/04/18	Deciphered Date	

Compal Electronics, Inc.

Title: **PROCESSOR DECOUPLING**

Size	Document Number	Rev
A3		1.0

Date: Tuesday, March 12, 2013 | Sheet 46 of 51

Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	Base on EE's request for fine tune power sequence.	P44	Change PR866 from 2.49k to 130k.	2013.1.11	From 0.1 to 0.2
2	For fine tune OCP set up point of VGA core.	P44	Change PR860 from 604ohm to 866ohm.	2013.1.11	From 0.1 to 0.2
3	Base on EE's request for fine tune power sequence.	P44	Change PR861 from 47k to 91k.	2013.1.11	From 0.1 to 0.2
4	Base on must meet EUP spec, change power design.	P37	Remove PR110, PC108, PR114, PC109, PR109, PC107,PU101, PR111, PD101, PR138, PR116, PR112, PD105, PR125, PR128, PC114, PR129, PQ101, PD104, PR123, PR124, PC115, PR131, PC117, PR103, PR104, PR105, PD102, PQ102, PR106, PR107, PQ103, PQ104, PR108, PR118, PR121, PC113, PR127, PQ106, PQ105, PR120, PR115, PC110, PC112, PR126, PR119, PR122, PD103.	2013.1.11	From 0.2 to 0.3
5	Base on must meet EUP spec, change power design.	P39	RemovePQ315, PR328, PR329, PQ316, PD304, PD301, PD302, PQ303, PR303, PR304, PQ306, PQ309.	2013.1.11	From 0.2 to 0.3
6	Base on must meet EUP spec, change power design.	P39	Add PR336, PR338, PR337, PR339, PQ319.	2013.1.11	From 0.2 to 0.3
7	Base on must meet EUP spec, change power design.	P40	Remove PR417, PC420, PQ407, PR420, PC424. Add PR411. Change PR418 from 47K to 2.2K.	2013.1.11	From 0.2 to 0.3
8					
9					
10					
11					
12					
13					
14					
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16					
17					
18					
19					
20					

Compal Electronics, Inc.
Title: PIR (PWR)
Size: Custom | Document Number: C38-G series Chief River Schematic | Rev: 1.0
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Phase	Date	No.	BOM	Sch	Layout	Description
SDV/FVT	2012/11/22	No.1	V	V	V	Page 5, Delete for Sun Pro M2 C17,C18,C19,C20,C21,C22,C23,C24,C25,C26,C27,C28,C29,C30,C31,C32 Delete PCIE_CRX_GTX_P8~15 PCIE_CTX_C_GRX_P8~15 PCIE_CTX_GRX_P8~15 PCIE_CRX_GTX_N8~15 PCIE_CTX_C_GRX_N8~15 PCIE_CTX_GRX_N8~15
SDV/FVT	2012/11/22	No.2	V	V	V	Page 17, Delete for Sun Pro M2 C1400,C1417,C1418,C1419,C1420,C1421,C1422,C1423,C1424,C1425,C1426,C1427,C1428,C1429,C1430,C1431 Delet PCIE_CRX_C_GTX_P8~15 PCIE_CRX_C_GTX_N8~15
SDV/FVT	2012/11/22	No.3	V	V	V	Page 17 ,U1401 change Part Number from SA000047H50 to SA00006BA30 for Sun Pro M2
SDV/FVT	2012/11/22	No.4	V	V	V	Page 24, Delete for Sun Pro M2 no Channel B C1621,C1622,C1623,C1624,C1625,C1626,C1627,C1628,C1629,C1630,C1631,C1632,C1633,C1634,C1635,R1462,R1463 C1636,C1637,C1638,C1639,C1640,C1641,C1642,C1643,C1644,C1645,C1646,C1647,C1648,C1649,C1650,R1464,R1465 C1651,C1652,C1653,C1654,C1655,C1656,C1657,C1658,C1659,C1660,C1661,C1662,C1663,C1664,C1665,C1569 C1666,C1667,R1504,R1504,R1505,R1505,R1506,R1507,R1508,R1509,R1510,R1510,R1511,R1511,R1512,C1570 R1513,R1514,R1515,R1516,R1517,R1518,R1519,R1520,R1521,R1522,R1523,R1524,R1525,R1526,R1527,U1409,U1410,U1411,U1412
SDV/FVT	2012/11/22	No.5		V	V	Page 19, Reserved T1406,T1407 for Sun Pro M2
SDV/FVT	2012/11/22	No.6	V	V	V	Page 18, Reserved D1401 for Sun Pro M2 PX5.5
SDV/FVT	2012/11/22	No.7	V	V	V	Page 19, Delete PX4.0 and PX5.0 schematic C1459,C1460,C1461,C1462,C1463,D1400,Q1401,Q1402,Q1403A,Q1403B,Q1404,Q1405,Q1406,R1401,R1438,R1439,,R1440, R1442,R1460,R1461,U1402,U1403
SDV/FVT	2012/11/22	No.8	V	V	V	Page 20, Delete DGPU Display Power not need reserved C1472,C1473,C1474,C1475,C1477,C1478,C1479,C1480,C1481,C1482,C1483,C1484,C1487,C1488
SDV/FVT	2012/11/22	No.9	V	V	V	Page 20, L1405 change Part Number from SM010009U00 to SM01000AX00 for Sun Pro M2 Spec Suggetion 120 to 220 ohm
SDV/FVT	2012/11/22	No.10	V	V	V	Page 20, Delete R1457,R1458 ,Because the Sun Pro M2 AW28,AW18 are NC.
SDV/FVT	2012/11/22	No.11	V	V	V	Page 20, Delete Thames&Seymour reserved R1407,R1408,R1409,R1410,R1411,R1412,R1413,R1414,R1415,R1416,R1417,R1466,R1467,R1468,R1469,R1471
SDV/FVT	2013/1/10	No.12	X	V	V	Page 12 U2 change Part Number from SA000066K10 to SA000066K60
SDV/FVT	2013/1/10	No.13		V	V	Page 31, for Power Eulot 6 modfiy Delete net FSTCHG,BATT_LEN#
SDV/FVT	2013/1/11	No.14	X	V	V	Page 18, for fine tune VGA Power saving Stuff C1441
SDV/FVT	2013/1/11	No.15	X	V	V	Page 19, for fine tune VGA Power Sequence R1445 change value from 20K to 470K R1446 change value from 20K to 10K

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SIT	2013/1/10	No.1	V	V	V	Page 35, for Power Eulot 6 modfiy Un-Stuff @ Q2408,R2463
SIT	2013/1/10	No.2	V	V	V	Page 33, for Touch Pad Module requirment Stuff R2470
SIT	2013/2/1	No.3	V	V	V	Page 07, for APU_SID and APU_SIC voltage smothly Stuff C69
SIT	2013/2/1	No.4	V	V	V	Page 26, for Logo LED brightness change Resistor Valve from 4.99K to 1.6K
SIT	2013/2/20	No.5		V	V	Page 36, for delete Discharge circuit ,remove R2324,Q2314,R2321,Q2309
SIT	2013/3/05	No.6		V	V	Page 33, for Factory issue ,remove JBT1
SIT	2013/3/12	No.7	V	V	V	Page 25, for cost down ,not need reserved for EC ,non-stuff Q2107,R2177,R2178
SIT	2013/3/12	No.8	V	V	V	Page 36, for customer request , Stuff R2302,R2303,Q2300,Q2302

Security Classification	Compal Secret Data		
Issued Date	2012/11/22	Deciphered Date	2015/11/22

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