

Compal Confidential

G470/G570 DIS+UMA+Muxless M/B Schematics Document

Intel Sandy Bridge Processor with DDRIII + Cougar Point PCH
ATI Robson/PX3.0,PX4.0

2010-10-22

LA-6751P / LA-6753P

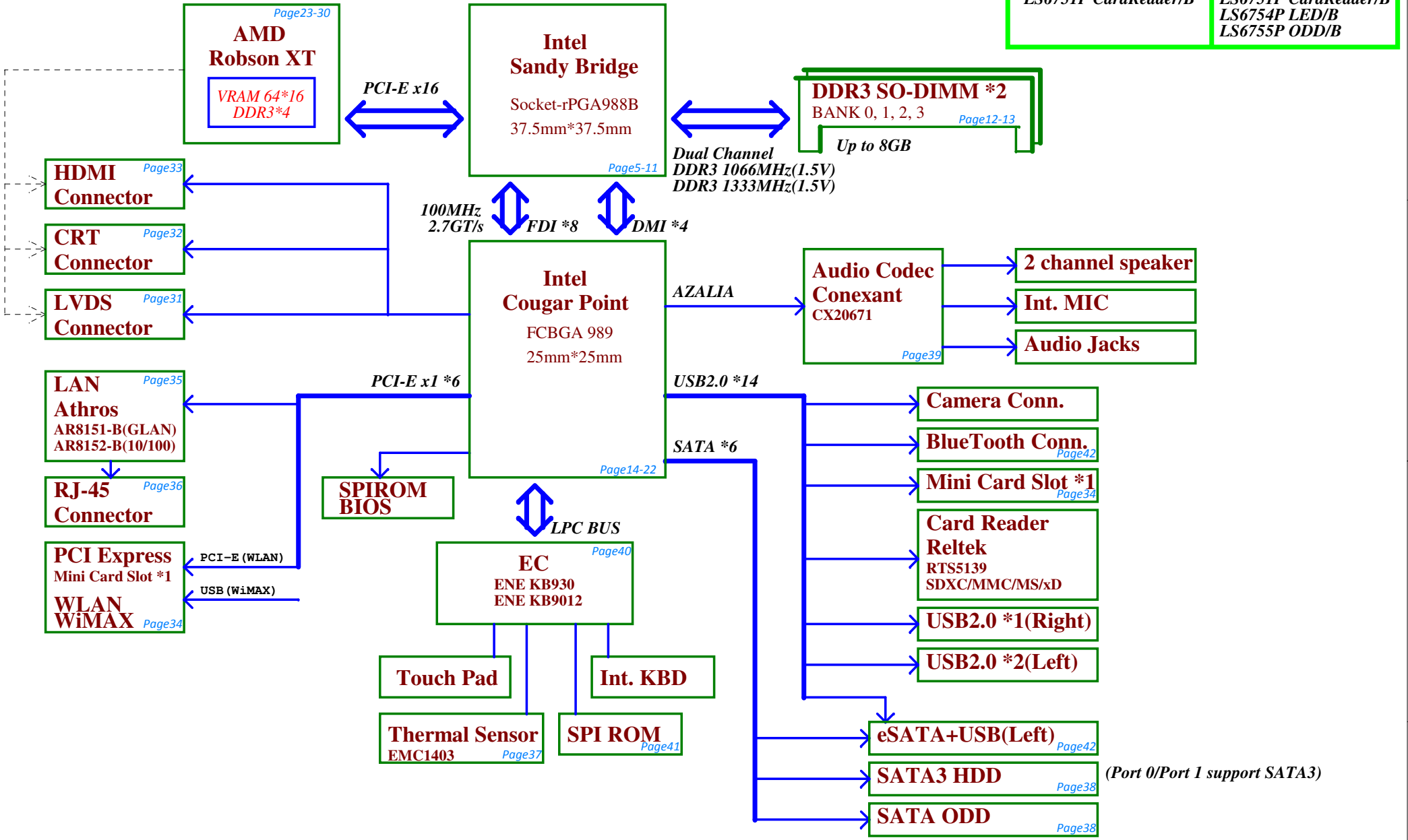
REV: 0.3

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For 14"(Page 4x)
LS6753P PWR/B
LS6751P CardReader/B

For 15"(Page 4x+1)
LS6753P PWR/B
LS6751P CardReader/B
LS6754P LED/B
LS6755P ODD/B



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Voltage Rails				
power plane	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +VCCP +CPU_CORE +VGA_CORE +GFX_CORE +1.8VS +0.75VS +1.05VS
State				
S0	○	○	○	○
S3	○	○	○	✗
S5 S4/AC	○	○	✗	✗
S5 S4/ Battery only	○	✗	✗	✗
S5 S4/AC & Battery don't exist	✗	✗	✗	✗

EC SM Bus1 address			EC SM Bus2 address		
Device	Address		Device	Address	
Smart Battery	0001 011Xb		Thermal Sensor EMC1403-2	1001_101xb	
			Thermal Sensor EMC1402-1	100_1100b	

PCH SM Bus address	
Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

SMBUS Control Table								
	SOURCE	VGA	BATT	KE930	SODIMM	WLAN WWAN	Thermal Sensor	PCH
SMB_EC_CK1	KB930	✗	✓	✗	✗	✗	✗	✗
SMB_EC_DA1	+3VALW		+3VALW					
SMB_EC_CK2	KB930	✗	✗	✗	✗	✗	✗	✓
SMB_EC_DA2	+3VALW							+3VS
SMBCLK	PCH	✗	✗	✗	✓	✓	✗	✗
SMBDATA	+3VALW				+3VS	+3VS		
SML0CLK	PCH	✗	✗	✗	✗	✗	✗	✗
SML0DATA	+3VALW							
SML1CLK	PCH	✓	✗	✓	✗	✗	✓	✗
SML1DATA	+3VALW	+3VS		+3VS			+3VS	

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%				
Ra/Rc/Re	100K +/- 5%				
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max	
0	0	0 V	0 V	0 V	EVT
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	DVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	PVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	MP
4	56K +/- 5%	1.036 V	1.185 V	1.264 V	
5	100K +/- 5%	1.453 V	1.650 V	1.759 V	
6	200K +/- 5%	1.935 V	2.200 V	2.341 V	
7	NC	2.500 V	3.300 V	3.300 V	

USB Port Table

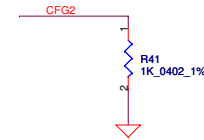
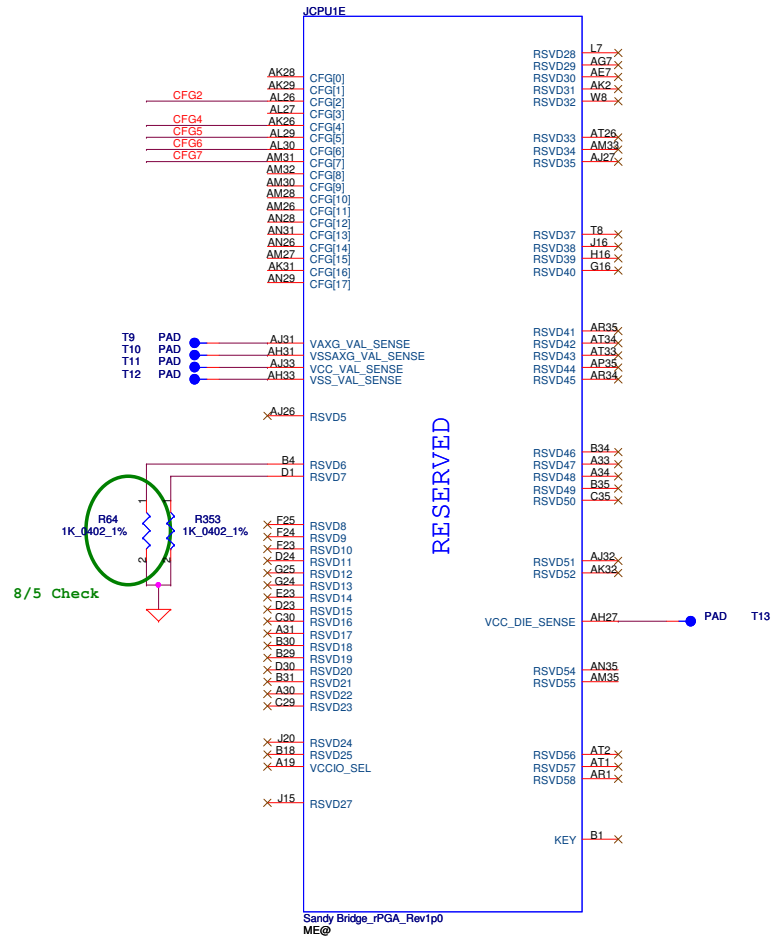
USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB/B (Right Side)
		1	USB Port (Left Side)
		2	USB Port (Left Side)
	UHCI1	3	USB Port (Left Side)
		4	
	UHCI2	5	Camera
		6	
EHCI2	UHCI3	7	
		8	Mini Card(WLAN)
	UHCI4	9	
		10	
	UHCI5	11	Card Reader
		12	
	UHCI6	13	Blue Tooth

BOM Structure Table

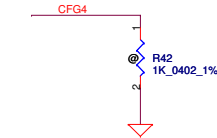
BTO Item	BOM Structure
UMA and PX bus	PX@
Discrete Only	DIS@
PX3.0 only, not for BACO	PX3@
BACO	BACO@
COMMON HDMI	HDMI@
UMA HDMI	UMA_HDMI@
Discrete HDMI	VGA_HDMI@
eSATA	ESATA@
Blue Tooth	BT@
Connector	ME@
45 LEVEL	45@
10/100 LAN	8152@
GIGA LAN	GIGA@
Cameara	CMOS@
Unpop	@

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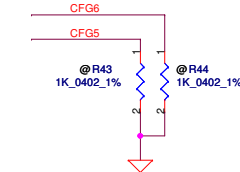
CFG Straps for Processor



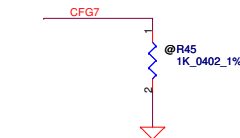
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0: Lane Reversed



Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



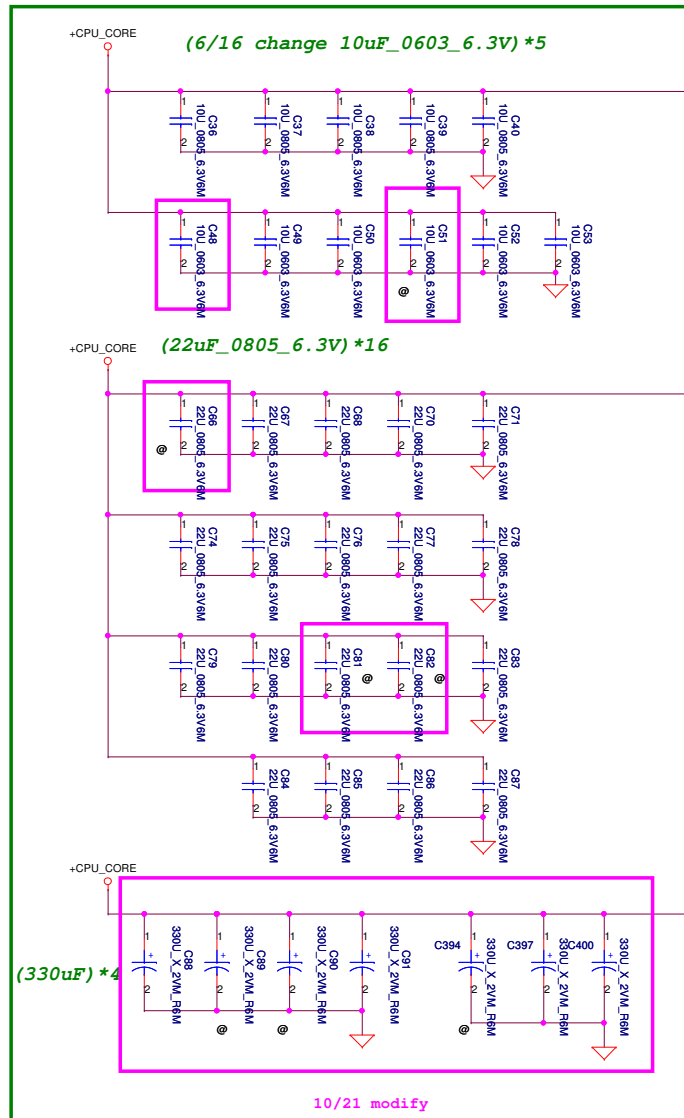
PCIe Port Bifurcation Straps	
CFG[6:5]	* 11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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QC=94A
DC=53A

JCPU1F

AG35 VCC1
AG34 VCC2
AG33 VCC3
AG32 VCC4
AG31 VCC5
AG30 VCC6
AG29 VCC7
AG28 VCC8
AG27 VCC9
AG26 VCC10
AF35 VCC11
AF34 VCC12
AF33 VCC13
AF32 VCC14
AF31 VCC15
AF30 VCC16
AF29 VCC17
AF28 VCC18
AF27 VCC19
AF26 VCC20
AD35 VCC21
AD34 VCC22
AD33 VCC23
AD32 VCC24
AD31 VCC25
AD30 VCC26
AD29 VCC27
AD28 VCC28
AD27 VCC29
AD26 VCC30
AC35 VCC31
AC34 VCC32
AC33 VCC33
AC32 VCC34
AC31 VCC35
AC30 VCC36
AC29 VCC37
AC28 VCC38
AC27 VCC39
AC26 VCC40
AA35 VCC41
AA34 VCC42
AA33 VCC43
AA32 VCC44
AA31 VCC45
AA30 VCC46
AA29 VCC47
AA28 VCC48
AA27 VCC49
Y35 VCC50
Y34 VCC51
Y33 VCC52
Y32 VCC53
Y31 VCC54
Y30 VCC55
Y29 VCC56
Y28 VCC57
Y27 VCC58
Y26 VCC59
Y25 VCC60
Y24 VCC61
Y23 VCC62
Y22 VCC63
Y21 VCC64
Y20 VCC65
Y19 VCC66
Y18 VCC67
Y17 VCC68
Y16 VCC69
Y15 VCC70
Y14 VCC71
Y13 VCC72
Y12 VCC73
Y11 VCC74
Y10 VCC75
Y9 VCC76
Y8 VCC77
Y7 VCC78
Y6 VCC79
Y5 VCC80
Y4 VCC81
Y3 VCC82
Y2 VCC83
Y1 VCC84
Y0 VCC85
V35 VCC86
V34 VCC87
V33 VCC88
V32 VCC89
V31 VCC90
V30 VCC91
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V23 VCC98
V22 VCC99
V21 VCC100

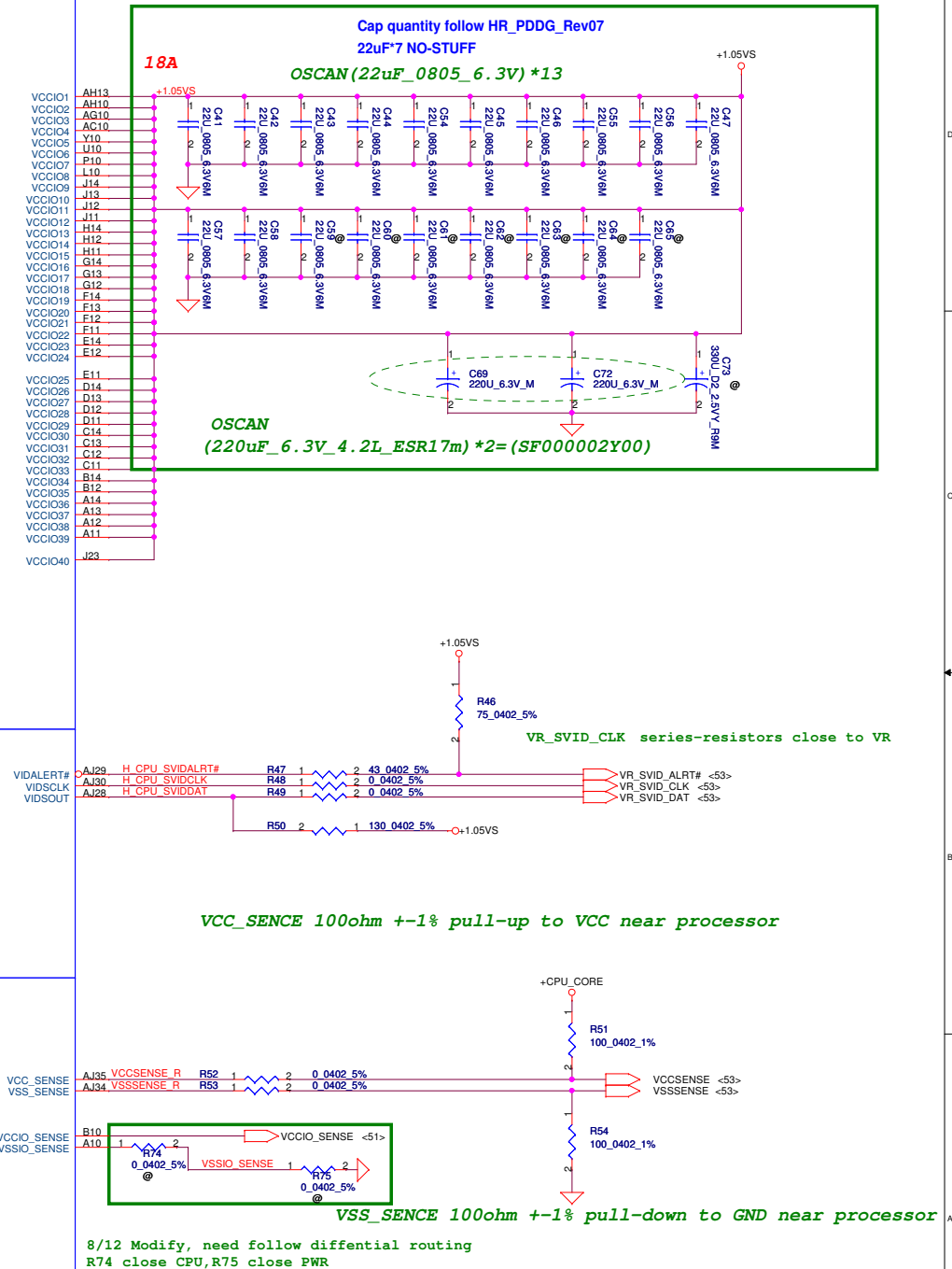
POWER

PEG AND DDR

CORE SUPPLY

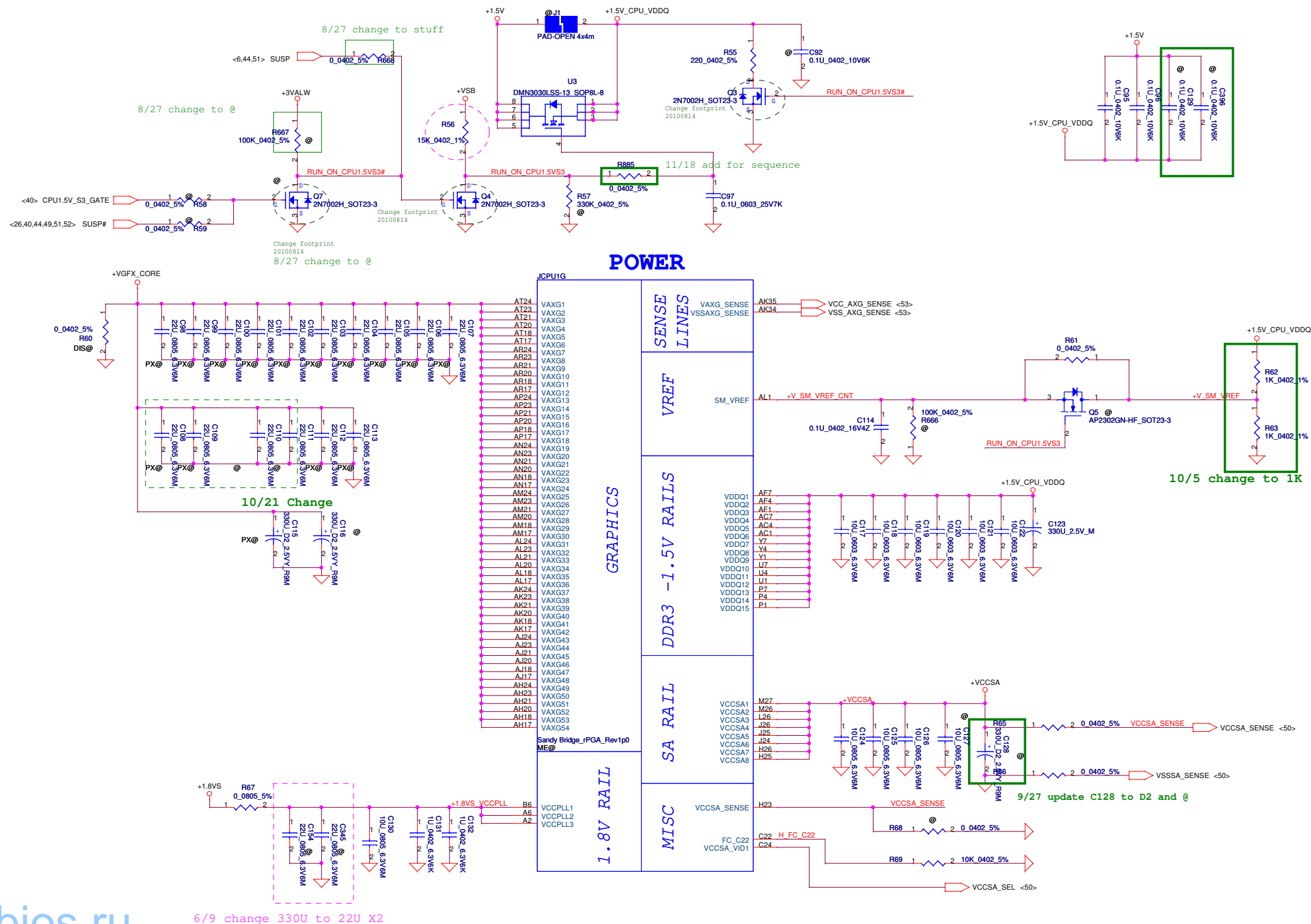
SVID

SENSE LINES

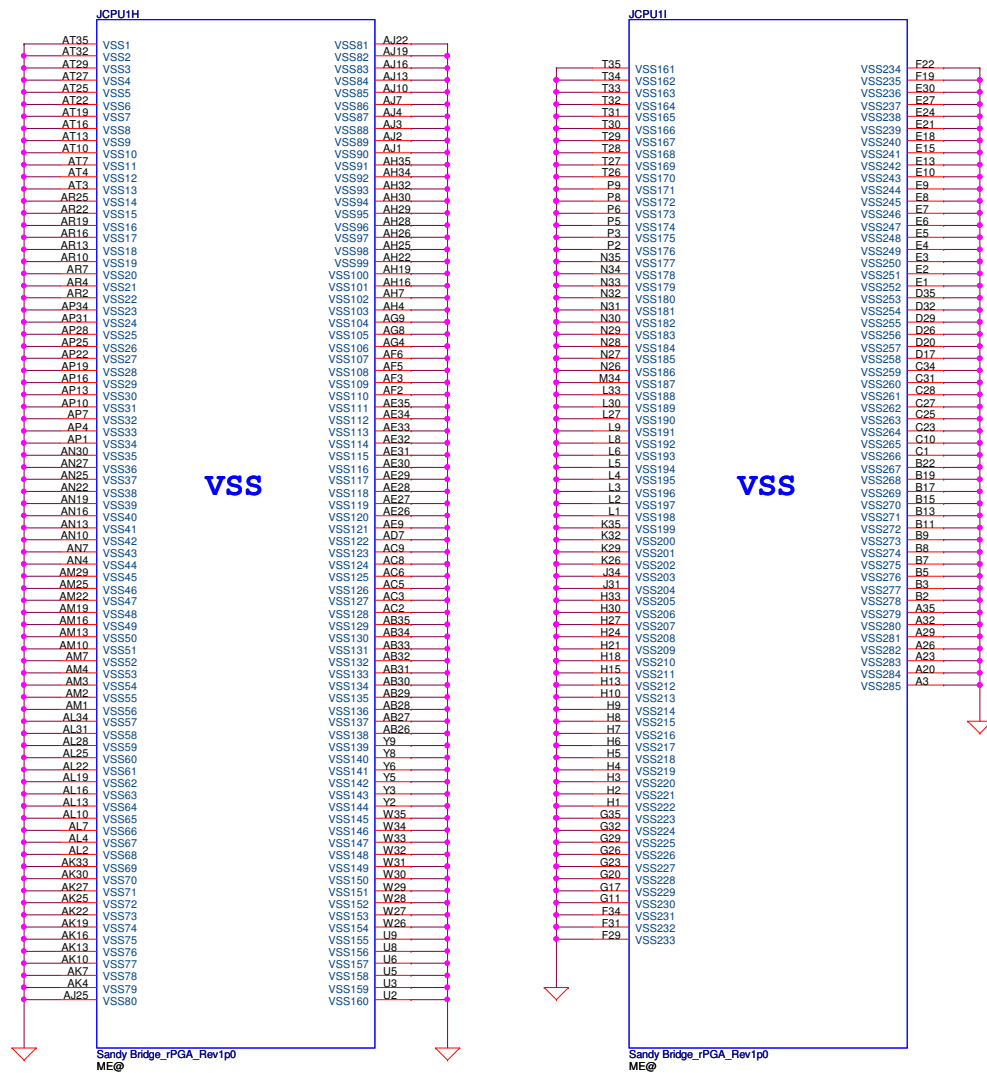


Sandy Bridge_rPGA Rev1n1
ME@

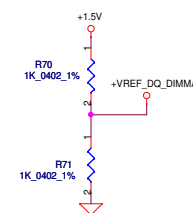
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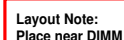


Layout Note:
Place near DIMM



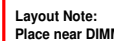
Layout Note:
Place near DIMM

(0.1uF 402 10V) *4

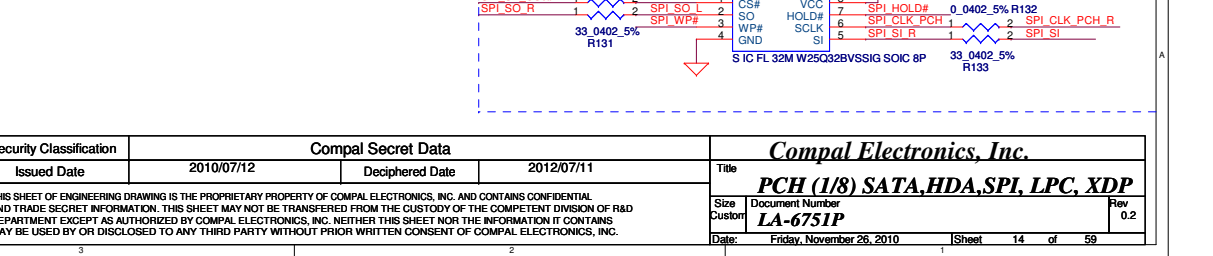
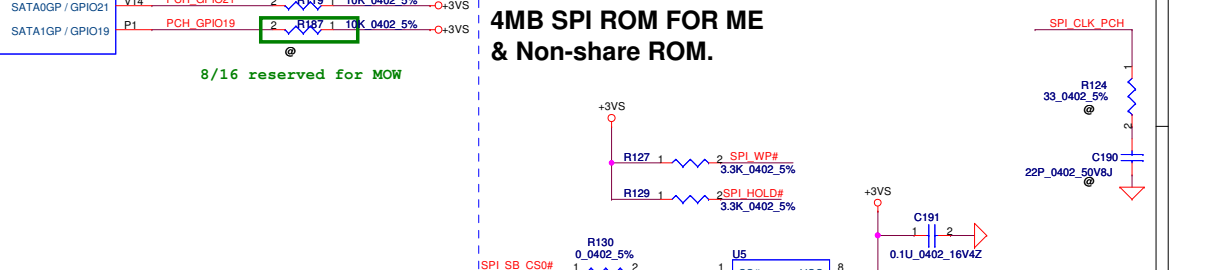
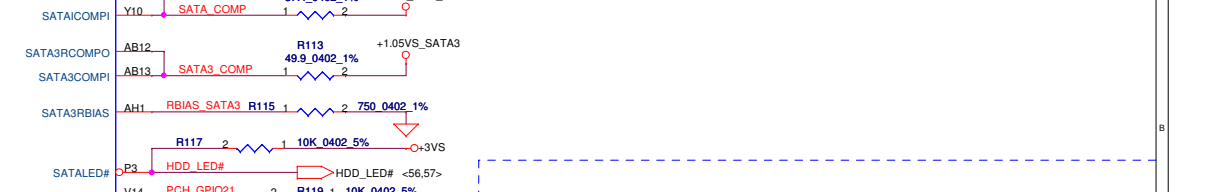
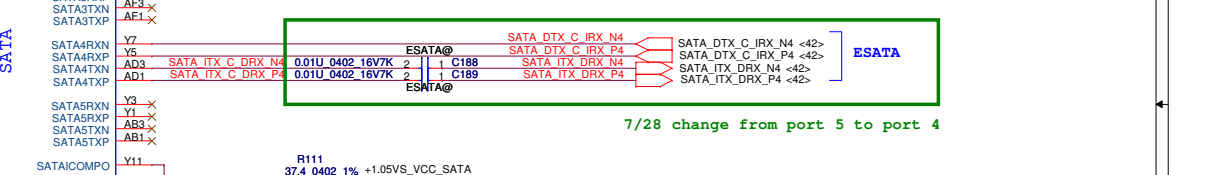
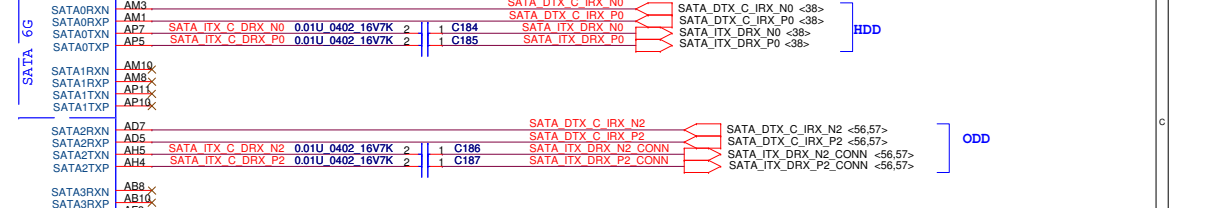
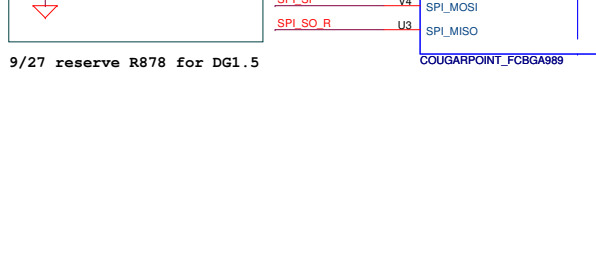
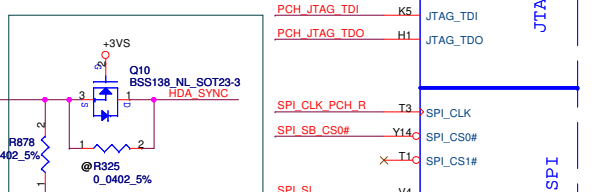
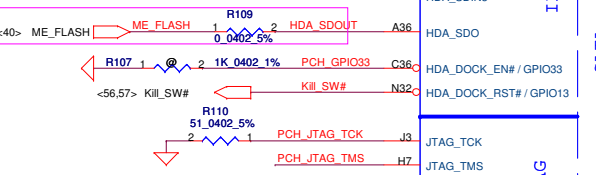
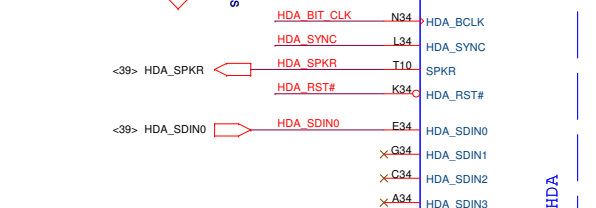
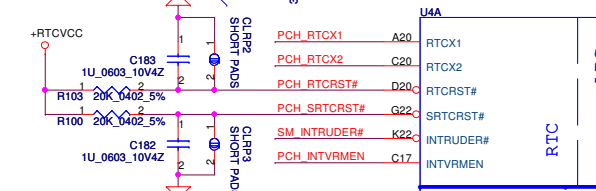
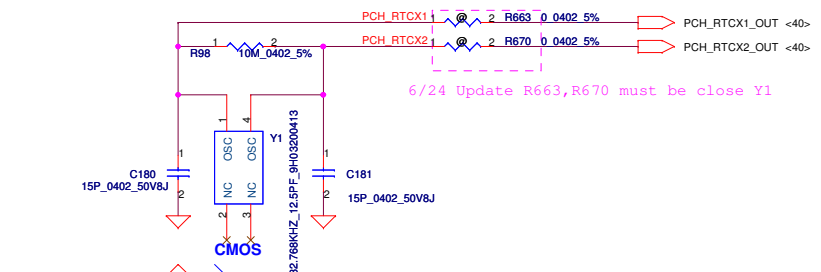
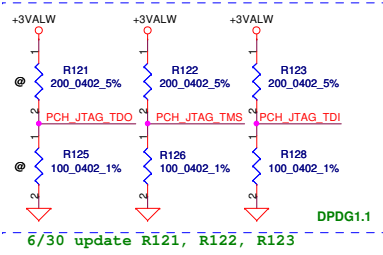
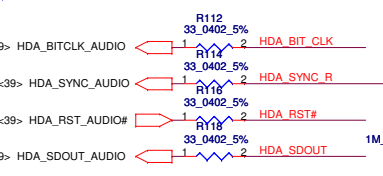
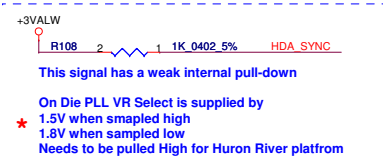
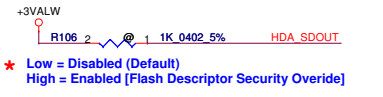
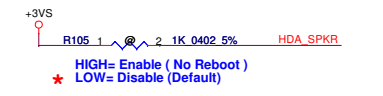
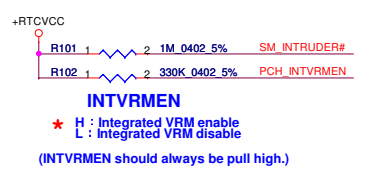
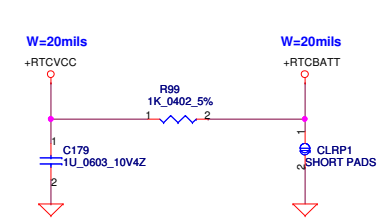


VTT(0.75V) =
3*0805 10uf 4*0402 1uf

7/28 Update connect GND directly

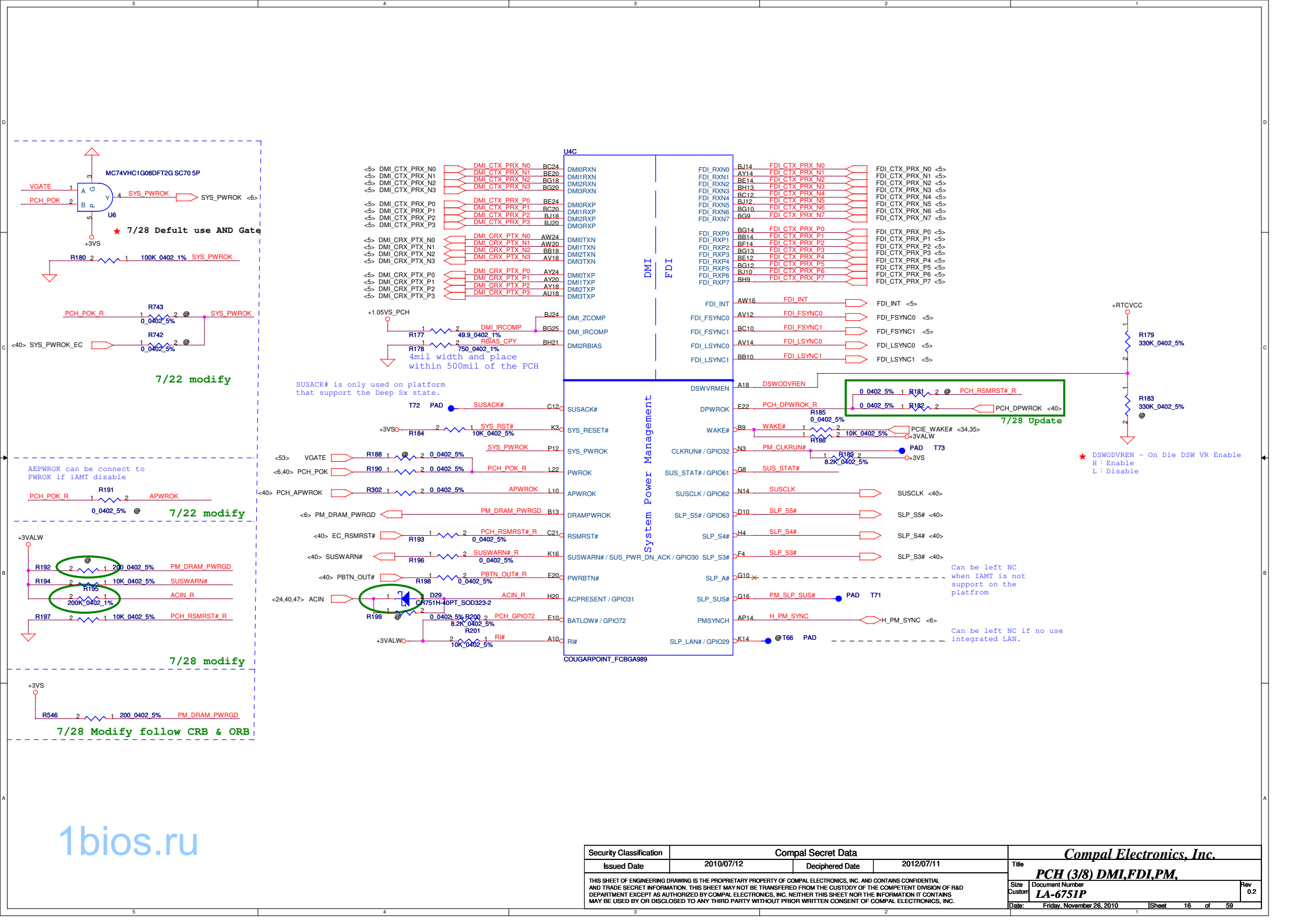


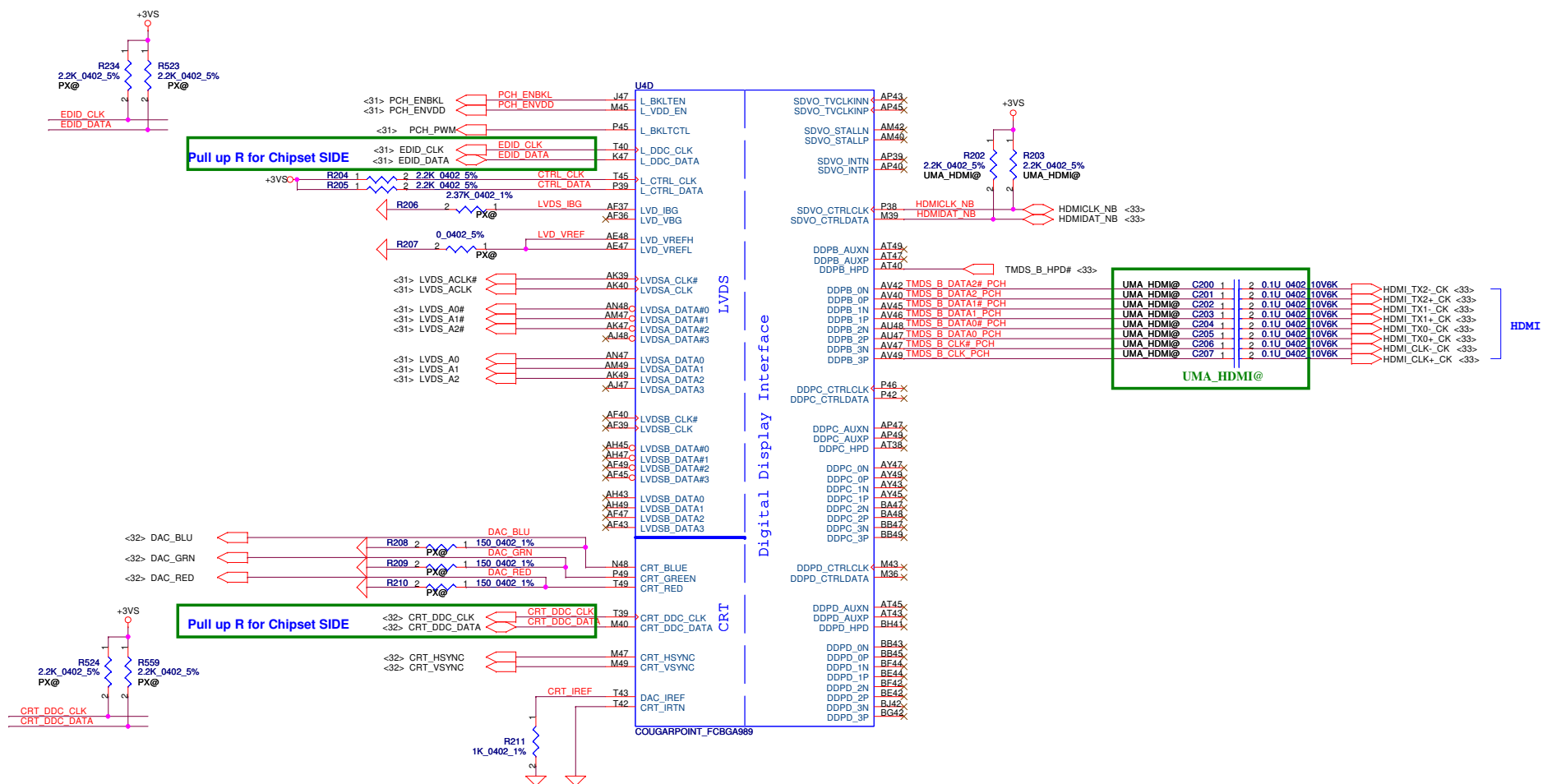
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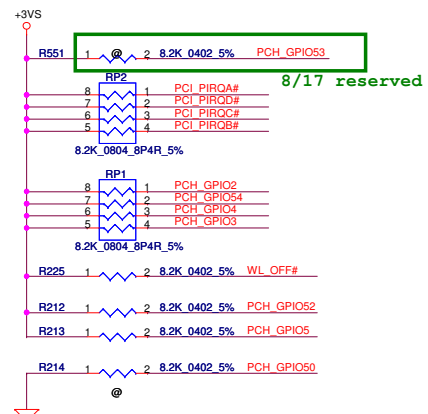






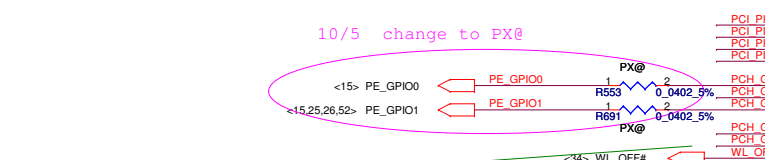
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				PCH (4/9) LVDS,CRT,DP,HDMI			
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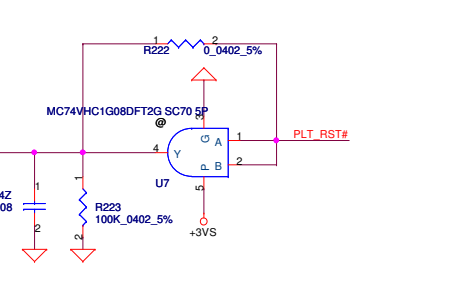
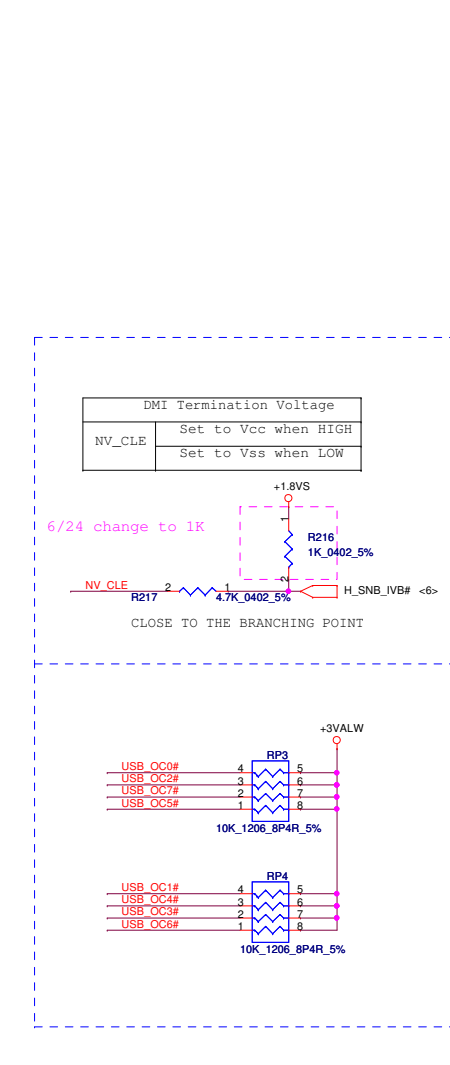
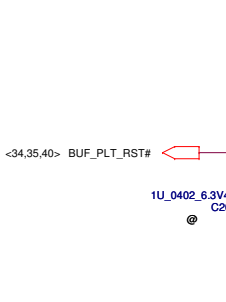
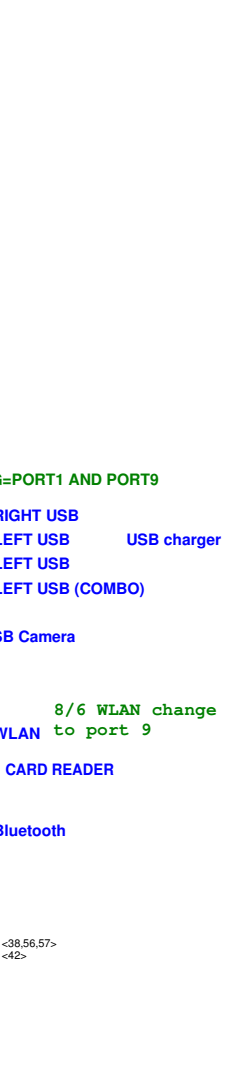
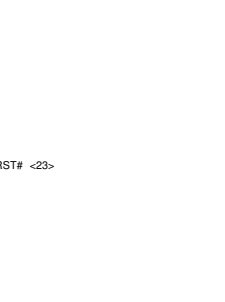
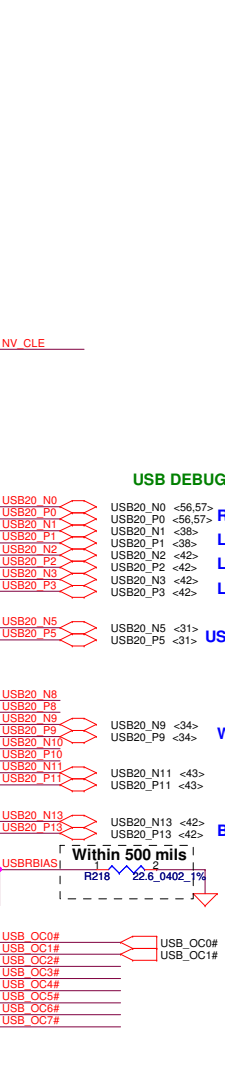
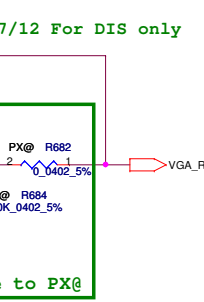
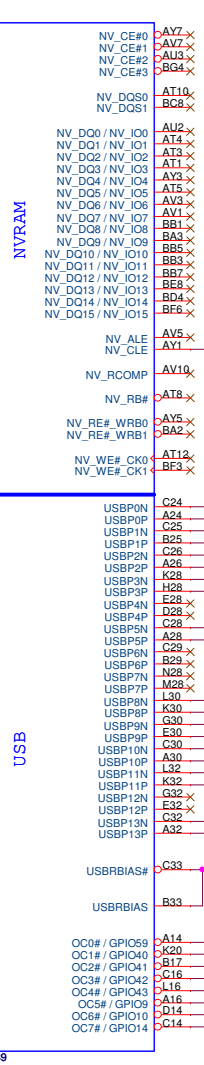
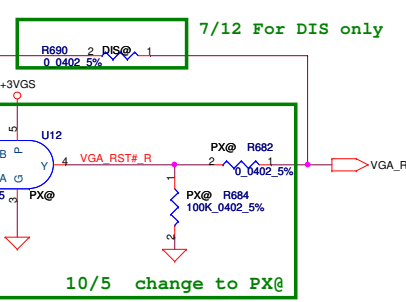
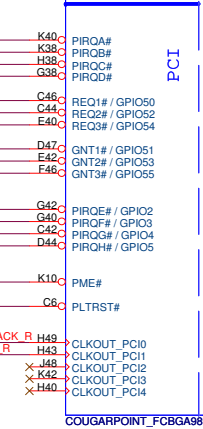
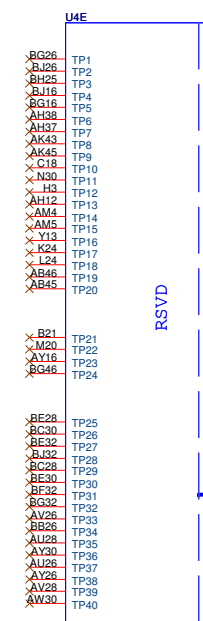
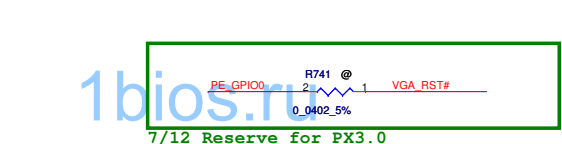
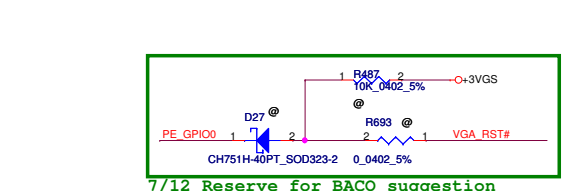
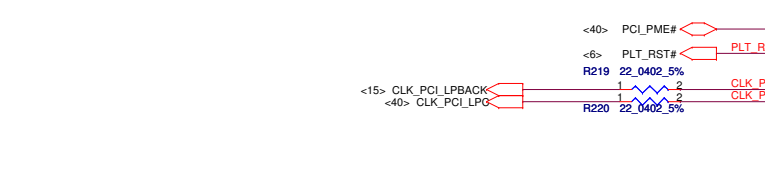


Boot BIOS Strap bit1 BBS1		
Bit11	Bit10	Destination
0	1	Reserved
1	0	Reserved
1	1	★ SPI (Default)
0	0	LPC

Al6 swap override Strap/Top-Block Swap Override jumper	
Low=Al6 swap override/Top-Block Swap Override enabled	High=Default ★



GPI053=This Signal has a weak internal pull-up.
NOTE: The internal pull-up is disabled after PLTRST# deasserts.



Security Classification		Compal Secret Data	
Issued Date	2010/07/12	Deciphered Date	2012/07/11
Title		Compal Electronics, Inc.	
Size		PCH (5/9) PCI, USB	
Custom		LA-6751P	
Date		Friday, November 26, 2010	
Sheet		18 of 59	

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ICC_EN#
Integrated Clock Chip Enable

H ; Disable
★ L ; Enable

7/22 update to reserve only

R235 1 2 1K 0402 5% EC_SMI#
Weak internal pull-high

GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up
★ H : On-Die voltage regulator enable
★ L : On-Die PLL Voltage Regulator disable

R240 1 2 1K 0402 5% PCH_GPIO28

PCH_GPIO27 (Have internal Pull-High)
★ High: VCCVRM VR Enable
Low: VCCVRM VR Disable

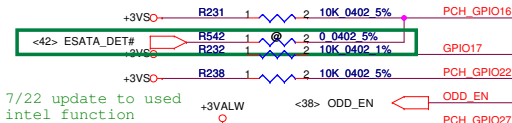
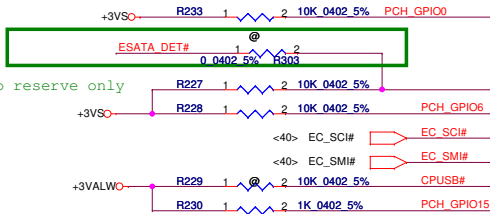
R245 1 2 1K 0402 5% PCH_GPIO27

+3VSO R250 1 2 1K 0402 5% PCH_GPIO36

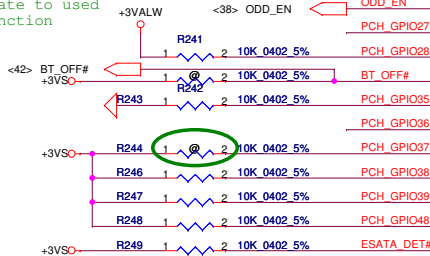
8/5 update to pull down

R881 1 2 1K 0402 5% PCH_GPIO37

10/8 update to pull down for checklist Rev1.2



7/22 update to used intel function



+3VSO R251 1 2 1K 0402 5% PCH_GPIO57

- PAD T19 @ A4 VSS_NCTF_1
- PAD T21 @ A44 VSS_NCTF_2
- PAD T23 @ A45 VSS_NCTF_3
- PAD T25 @ A46 VSS_NCTF_4
- PAD T27 @ A5 VSS_NCTF_5
- PAD T29 @ A6 VSS_NCTF_6
- PAD T31 @ B3 VSS_NCTF_7
- PAD T33 @ B47 VSS_NCTF_8
- PAD T35 @ BD1 VSS_NCTF_9
- PAD T37 @ BD49 VSS_NCTF_10
- PAD T39 @ BE1 VSS_NCTF_11
- PAD T41 @ BE49 VSS_NCTF_12
- PAD T43 @ BF1 VSS_NCTF_13
- PAD T45 @ BF49 VSS_NCTF_14

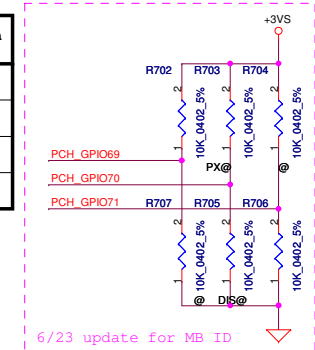
U4F

- BMBUSY# / GPIO0
- TACH1 / GPIO1
- TACH2 / GPIO6
- TACH3 / GPIO7
- TACH7 / GPIO71
- GPIO8
- LAN_PHY_PWR_CTRL / GPIO12
- GPIO15
- SATA4GP / GPIO16
- TACH0 / GPIO17
- SCLK / GPIO22
- GPIO24 / MEM_LED
- GPIO27
- STP_PC# / GPIO34
- GPIO35
- SATA2GP / GPIO36
- SATA3GP / GPIO37
- SLOAD / GPIO38
- SDATAOUT0 / GPIO39
- SDATAOUT1 / GPIO48
- SATA5GP / GPIO49
- GPIO57

GPIO
CPU/MISC
NCTF

- TACH4 / GPIO68
- TACH5 / GPIO69
- TACH6 / GPIO70
- TACH7 / GPIO71
- P4
- AU16 PCH_PECI_R
- RCIN#
- PROCPWRGD
- THRMTRIP#
- INIT3_3V#
- NC_1
- NC_2
- NC_3
- NC_4
- NC_5
- VSS_NCTF_15
- VSS_NCTF_16
- VSS_NCTF_17
- VSS_NCTF_18
- VSS_NCTF_19
- VSS_NCTF_20
- VSS_NCTF_21
- VSS_NCTF_22
- VSS_NCTF_23
- VSS_NCTF_24
- VSS_NCTF_25
- VSS_NCTF_26
- VSS_NCTF_27
- VSS_NCTF_28
- VSS_NCTF_29
- VSS_NCTF_30
- VSS_NCTF_31
- VSS_NCTF_32

PCH_GPIO69	PCH_GPIO70	PCH_GPIO71	Function
0	0	0	UMA
1	0	0	DIS
0	1	0	PX3.0
1	1	0	PX4.0 *



6/23 update for MB ID

PCH_GPIO68 R224 1 2 1K 0402 5%
KB_RST# R226 1 2 1K 0402 5%

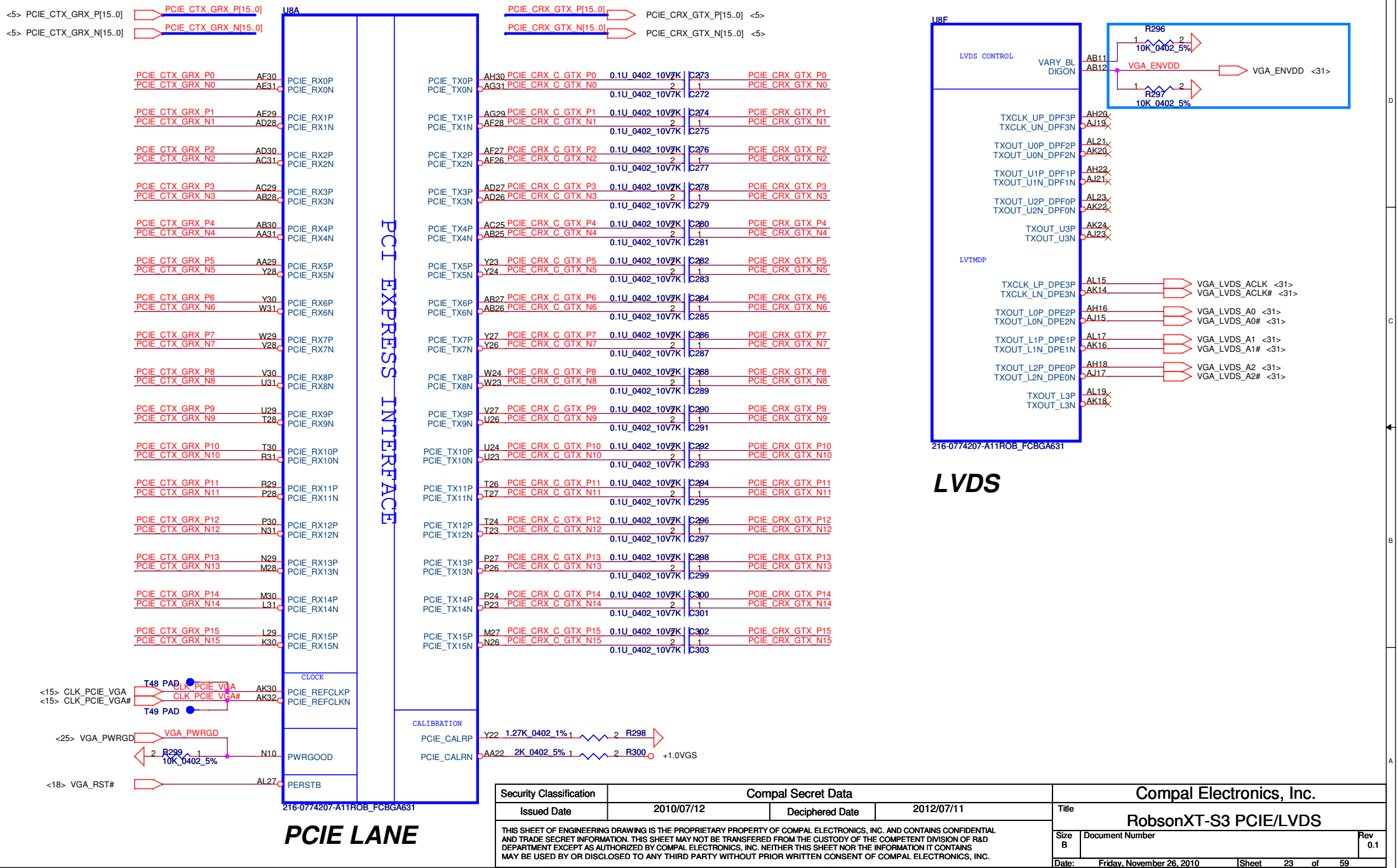
INIT3_3V
This signal has weak internal PU, can't pull low
Intel schematic reviee recommand.

1bios.ru

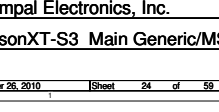
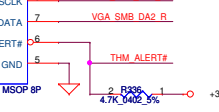
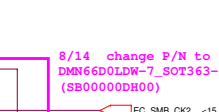
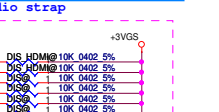
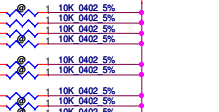
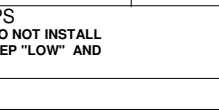
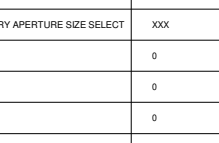
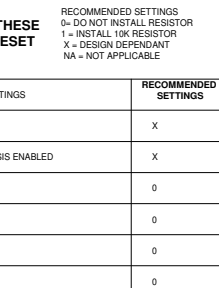
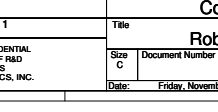
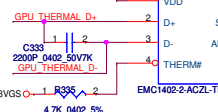
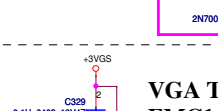
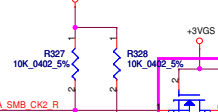
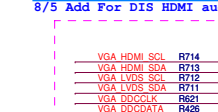
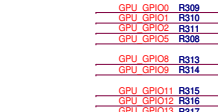
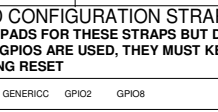
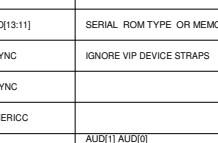
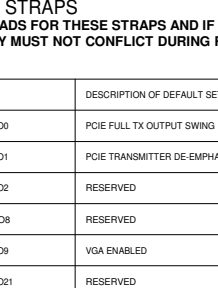
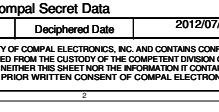
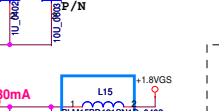
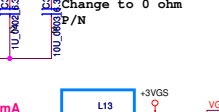
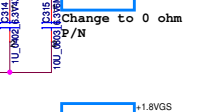
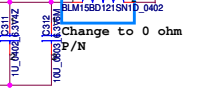
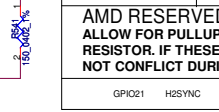
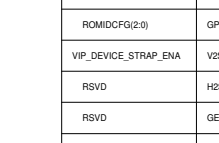
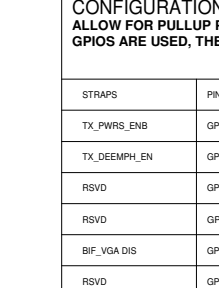
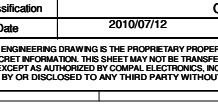
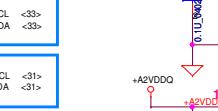
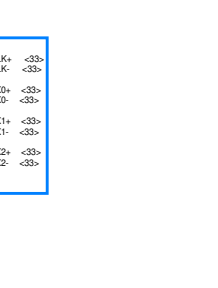
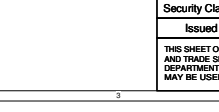
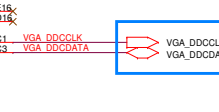
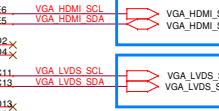
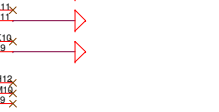
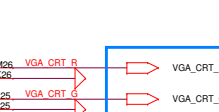
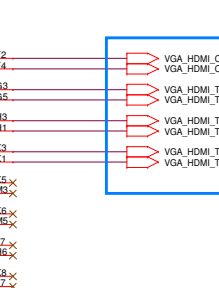
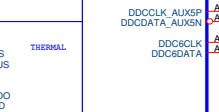
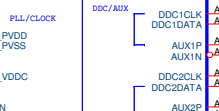
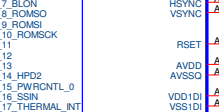
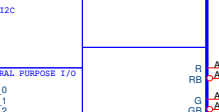
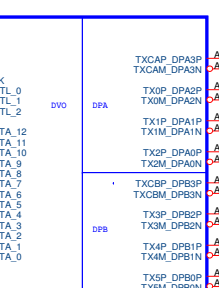
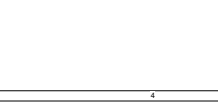
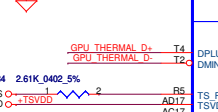
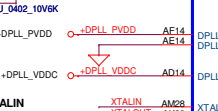
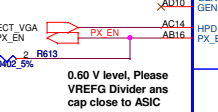
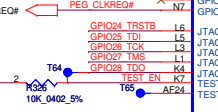
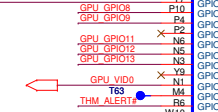
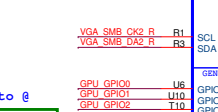
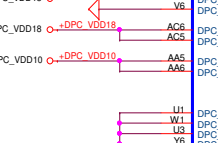
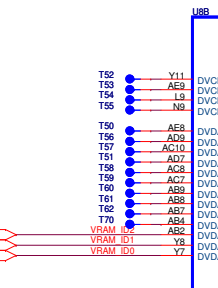
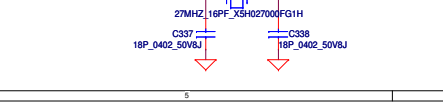
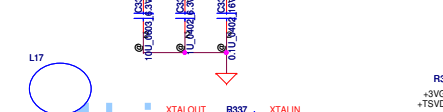
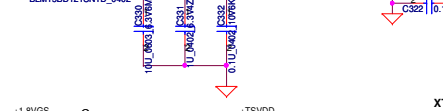
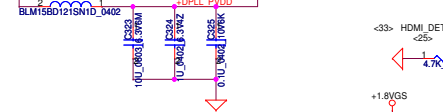
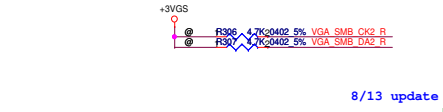
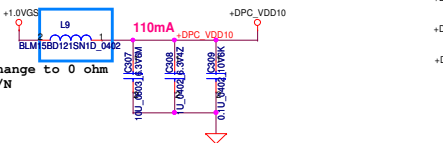
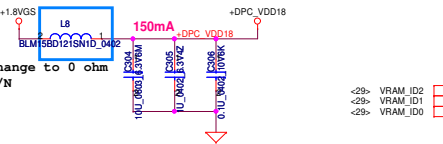
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2010/07/12	Deciphered Date	2012/07/11	PCH (6/9) GPIO, CPU, MISC	
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				Date: Friday, November 26, 2010	Sheet 19 of 59



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/07/12	Deciphered Date	2012/07/11	Title	PCH (9/9) VSS
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				Date: Friday, November 26, 2010	Rev 0.2
				Sheet 22 of 59	



TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for desktop)



CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

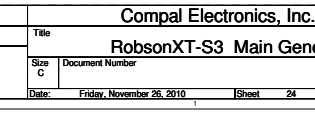
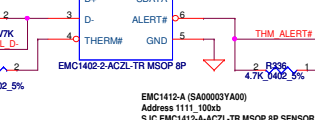
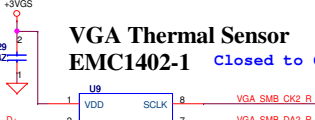
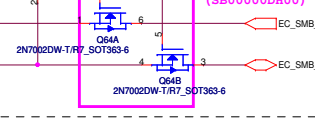
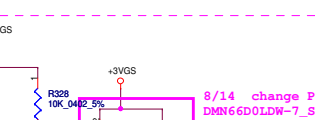
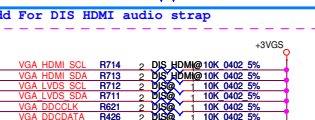
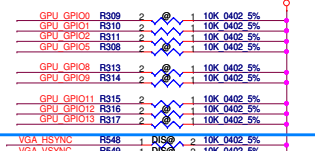
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	POIE FULL TX OUTPUT SWING	X
TX_DEEMPH_EN	GPIO1	POIE TRANSMITTER DE-EMPHASIS ENABLED	X
RSVD	GPIO2	RESERVED	0
RSVD	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	X
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	XXX
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD	H2SYNC		0
RSVD	GENERICC		0
AUD[0]	HSYNC	AUD[0] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	11
AUD[1]	VSNC		

AMD RESERVED CONFIGURATION STRAPS

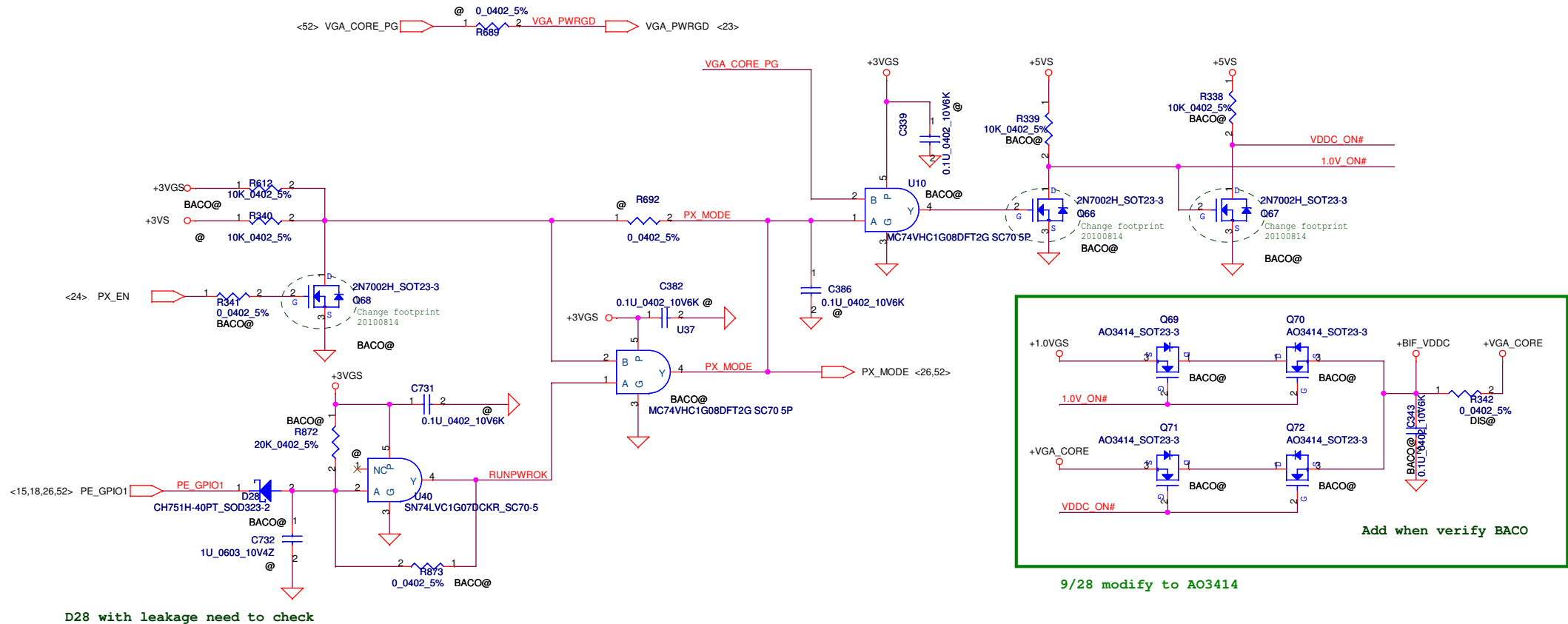
ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
GPIO21	H2SYNC		0
GPIO21	GENERICC		0
GPIO21	GPIO2		0
GPIO21	GPIO8		0

STRAPS

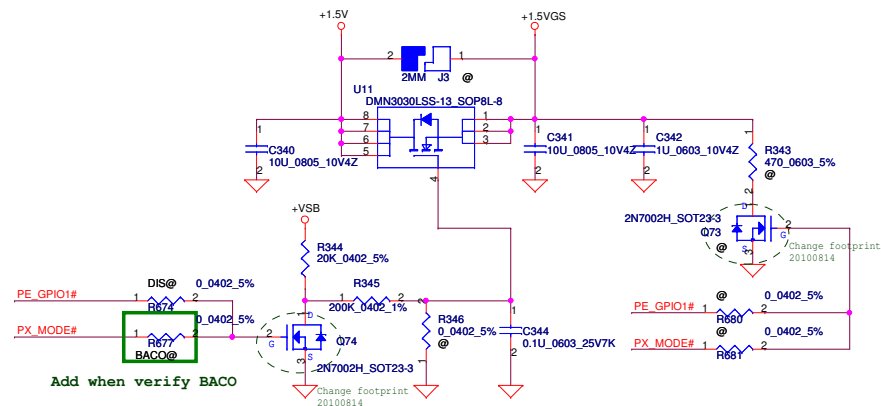


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Size	C	Document Number		Rev 0.2
Date:	Friday, November 26, 2010	ISheet	24	of 59



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Size B		Document Number		Rev 0.1	
Date:		Friday, November 26, 2010		Sheet 25 of 59	
LA-6751P					

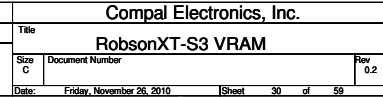
+VGA_PCIE TO +1.0VGS



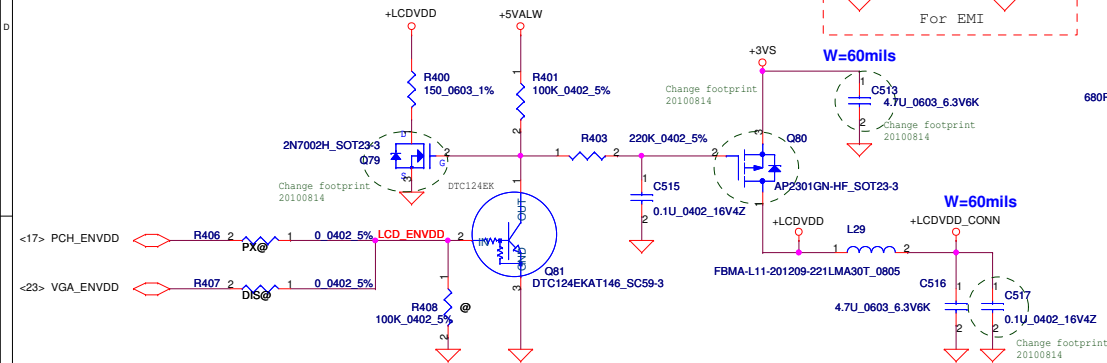
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Issued Date	2010/07/12	Deciphered Date	2012/07/11	Title		
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				Size	Document Number	Rev.
				Custom	LA-6751P	0.
Date:	Friday, November 26, 2010		Sheet	26	of	58



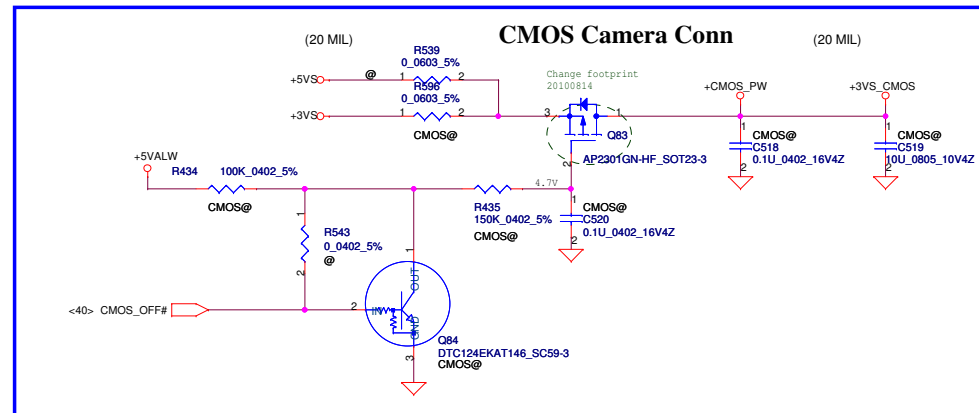
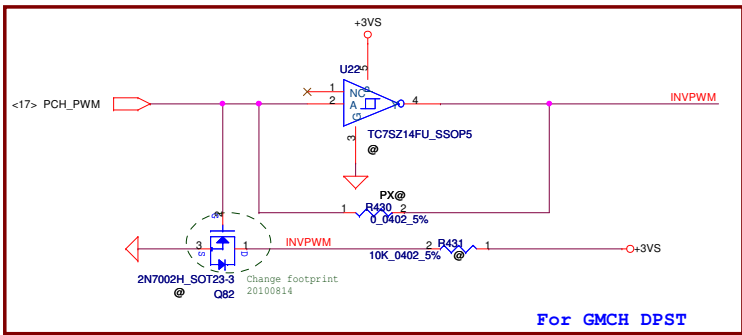
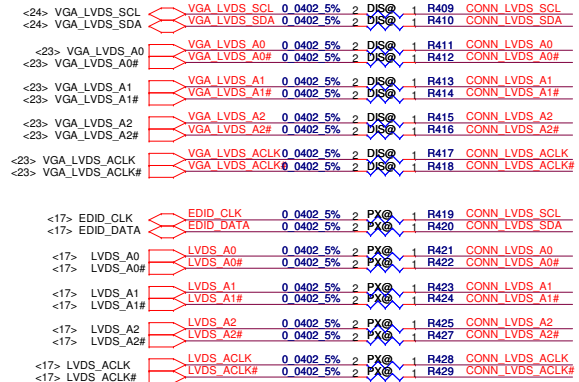
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LCD POWER CIRCUIT

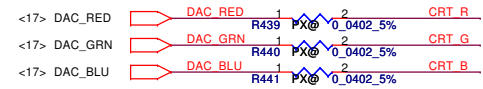


Pull high at chipset/VGA side

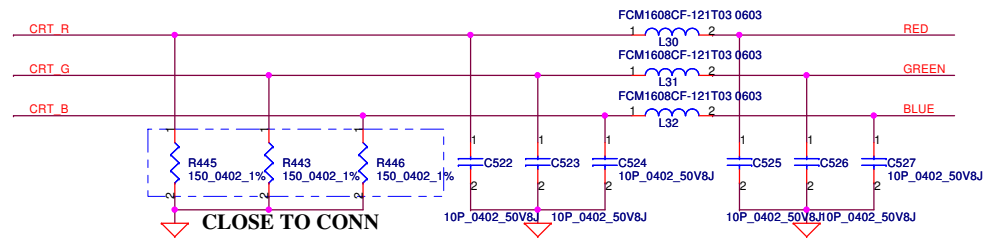
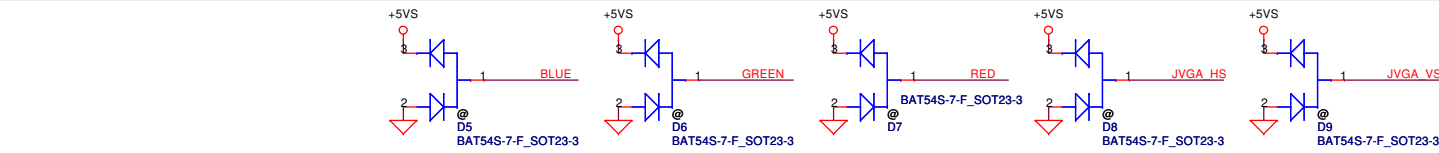
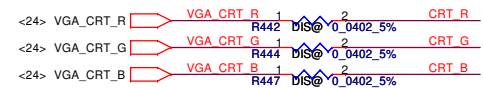


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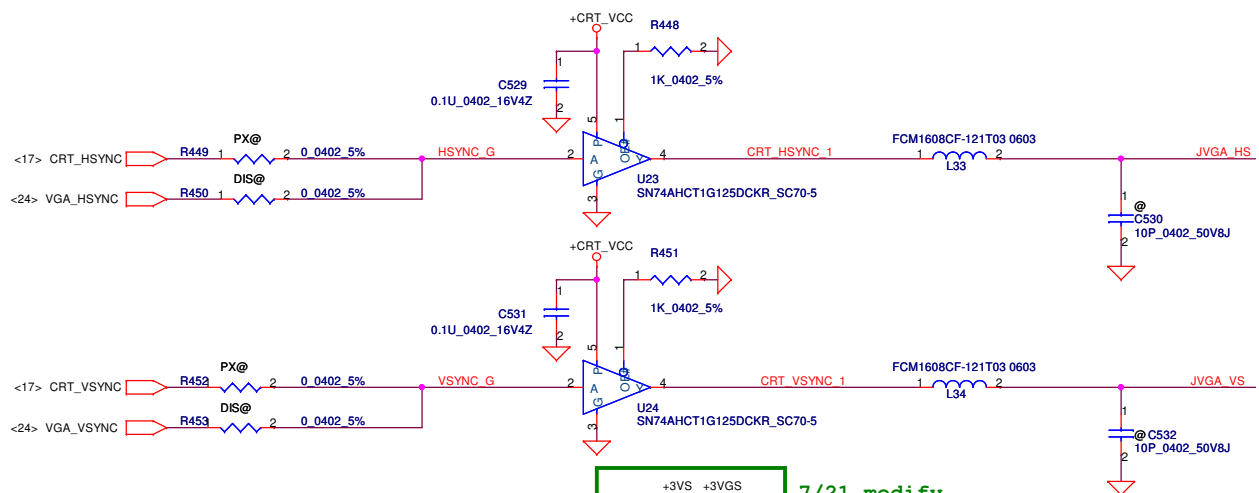
UMA only



DIS only

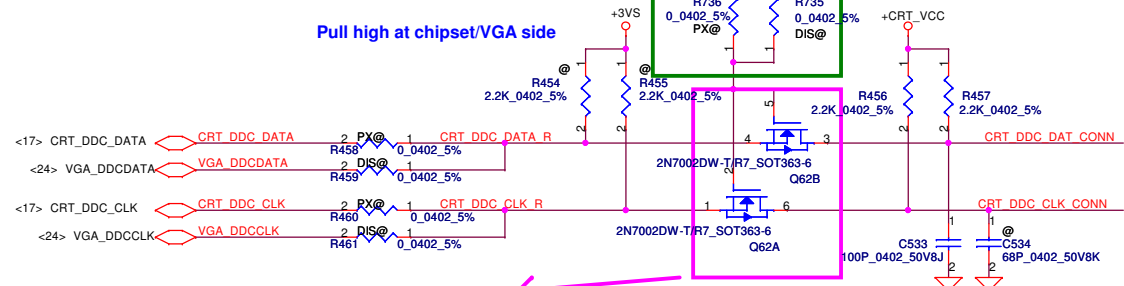


CLOSE TO CONN



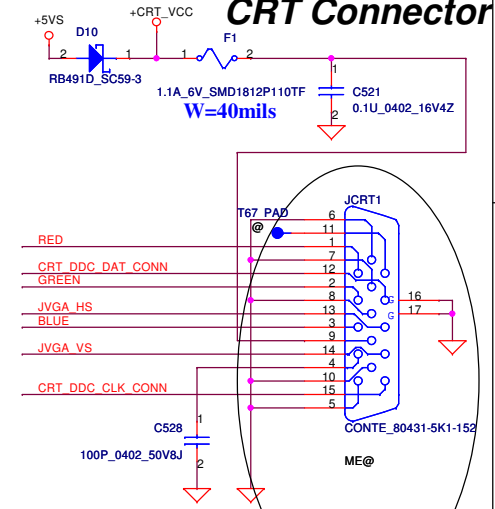
7/21 modify

Pull high at chipset/VGA side



8/14 change P/N to
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(SB00000DH00)

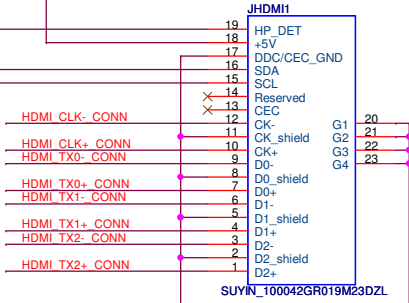
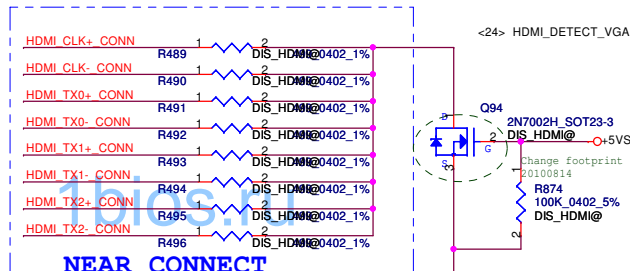
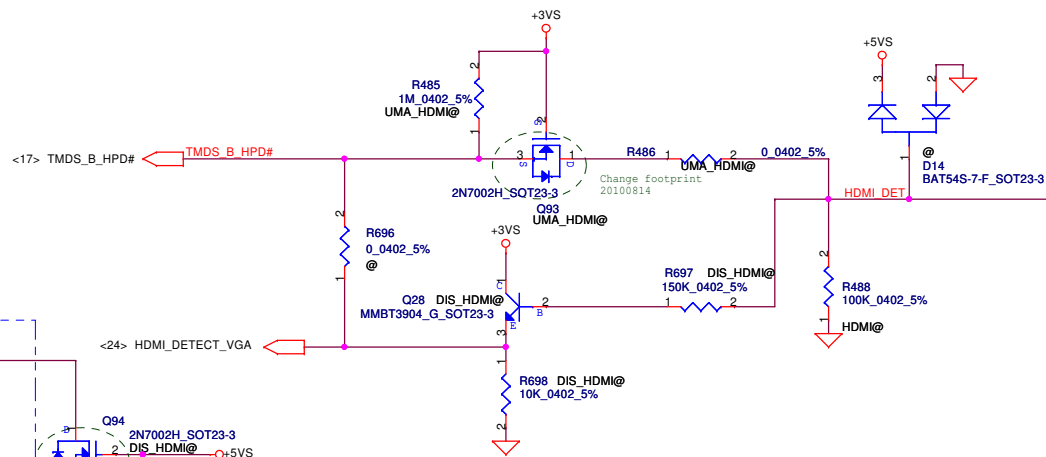
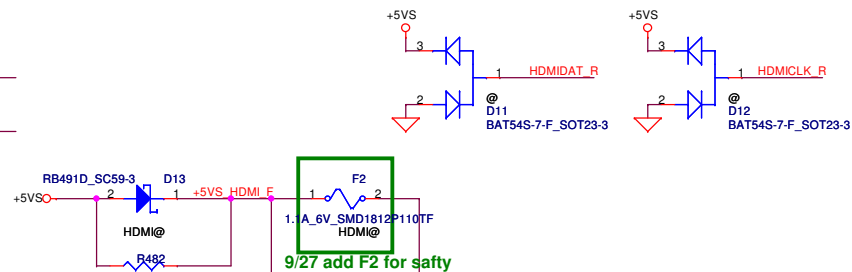
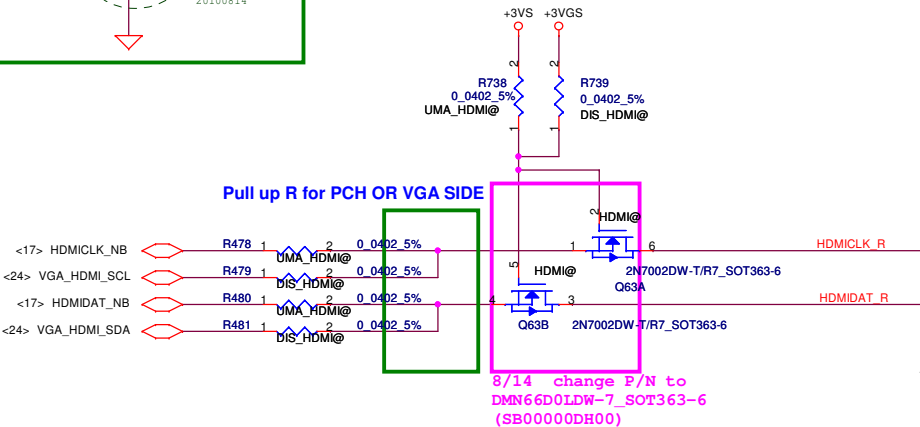
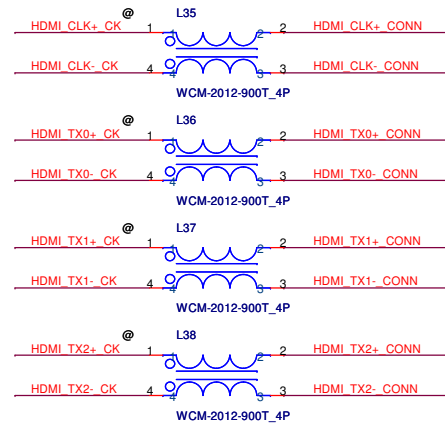
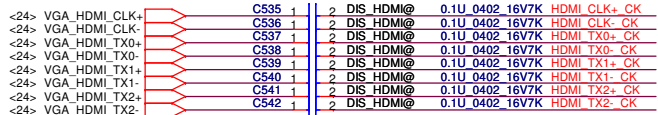
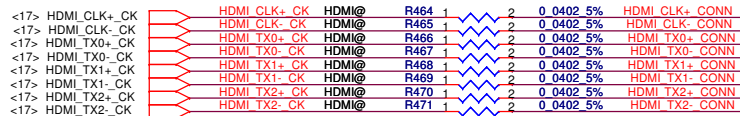
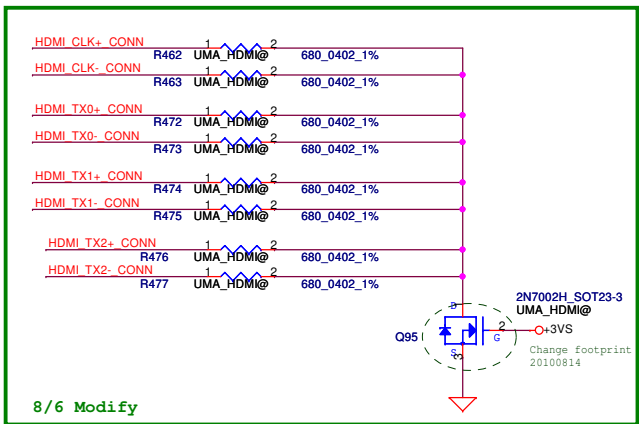
CRT Connector



Check CRT footprint 7/20_OTIS

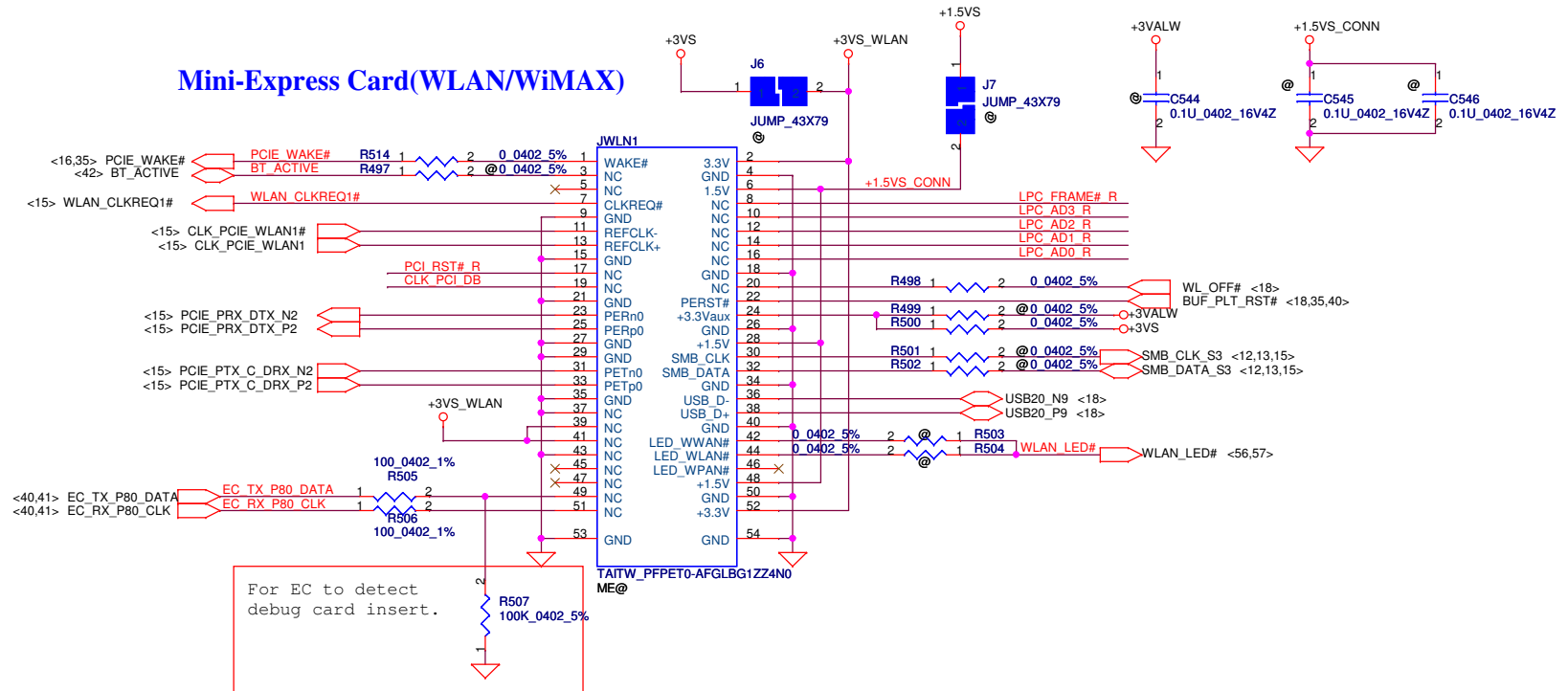
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Size	Custom	Document Number	LA-6751P		Rev 0.2
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				Custom	LA-6751P
				Date	Friday, November 26, 2010
				Sheet	33 of 59
				Rev	0.2

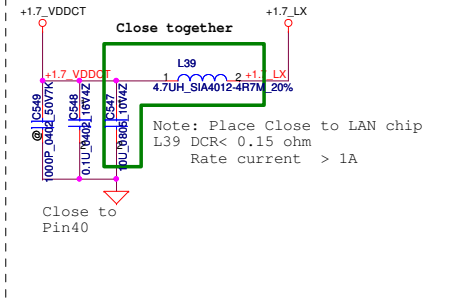
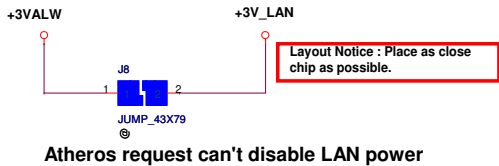
Mini-Express Card for WLAN/WiMAX(Half)



Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.

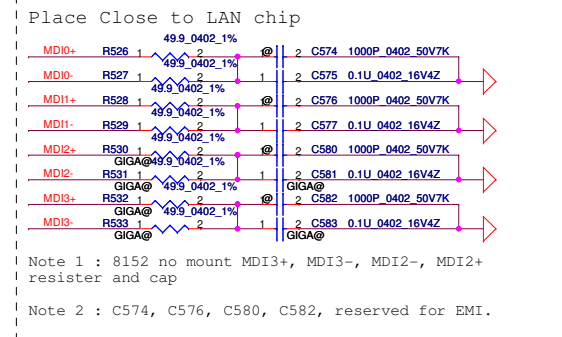
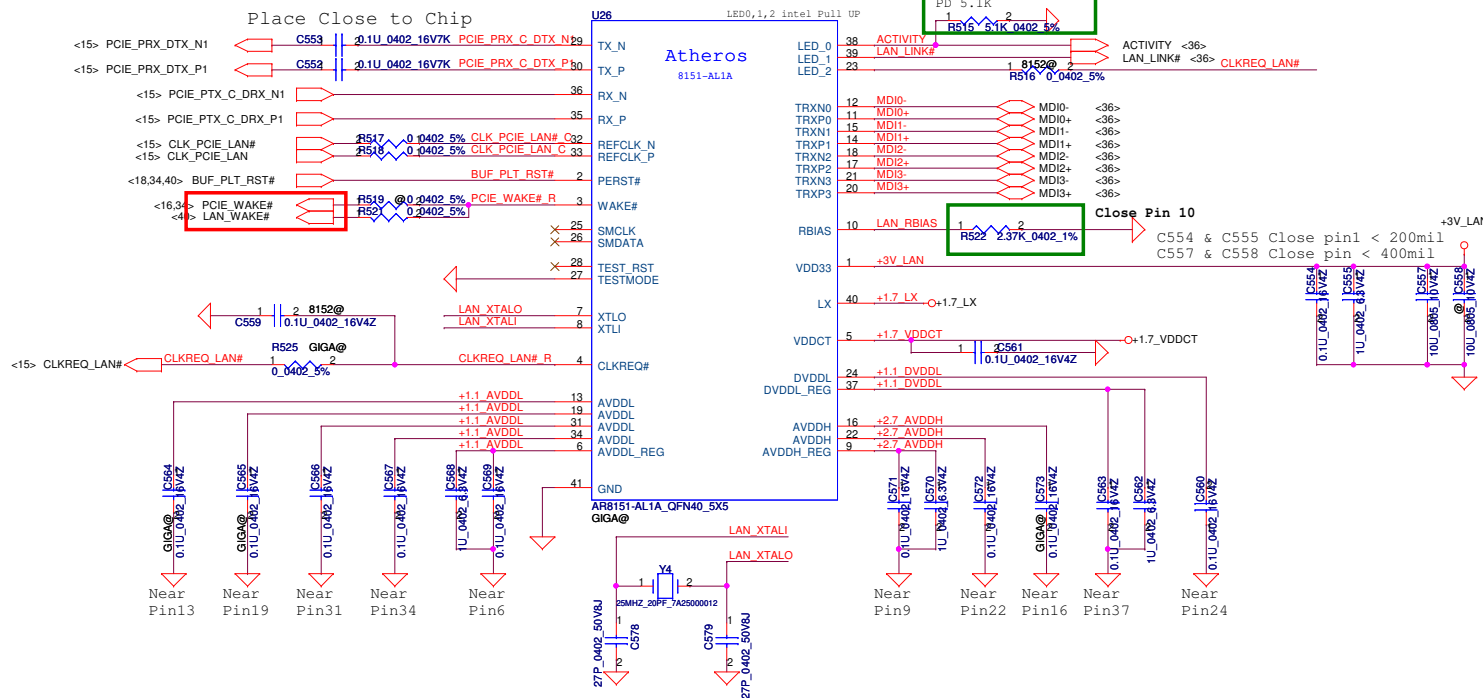
LPC_FRAME#_R	R508	1	2	0.0402 5%	LPC_FRAME#	LPC_FRAME# <14,40>
LPC_AD3_R	R509	1	2	0.0402 5%	LPC_AD3	LPC_AD3 <14,40>
LPC_AD2_R	R510	1	2	0.0402 5%	LPC_AD2	LPC_AD2 <14,40>
LPC_AD1_R	R511	1	2	0.0402 5%	LPC_AD1	LPC_AD1 <14,40>
LPC_AD0_R	R512	1	2	0.0402 5%	LPC_AD0	LPC_AD0 <14,40>
PCI_RST#_R	R513	1	2	0.0402 5%	PCI_RST#	PCI_RST# <14,40>
CLK_PCI_DB					CLK_PCI_DB	CLK_PCI_DB <15>

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				Size	Document Number
				LA-6751P	
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Pin	Description	Chip Default
LED0	H:Over Clock Enable L:Over Clock Disable *	H
LED2	H:SWR Switch mode regulator Select * AR8151 Pin23=LED2. AR8152, Pin23 is CLKREQ	--

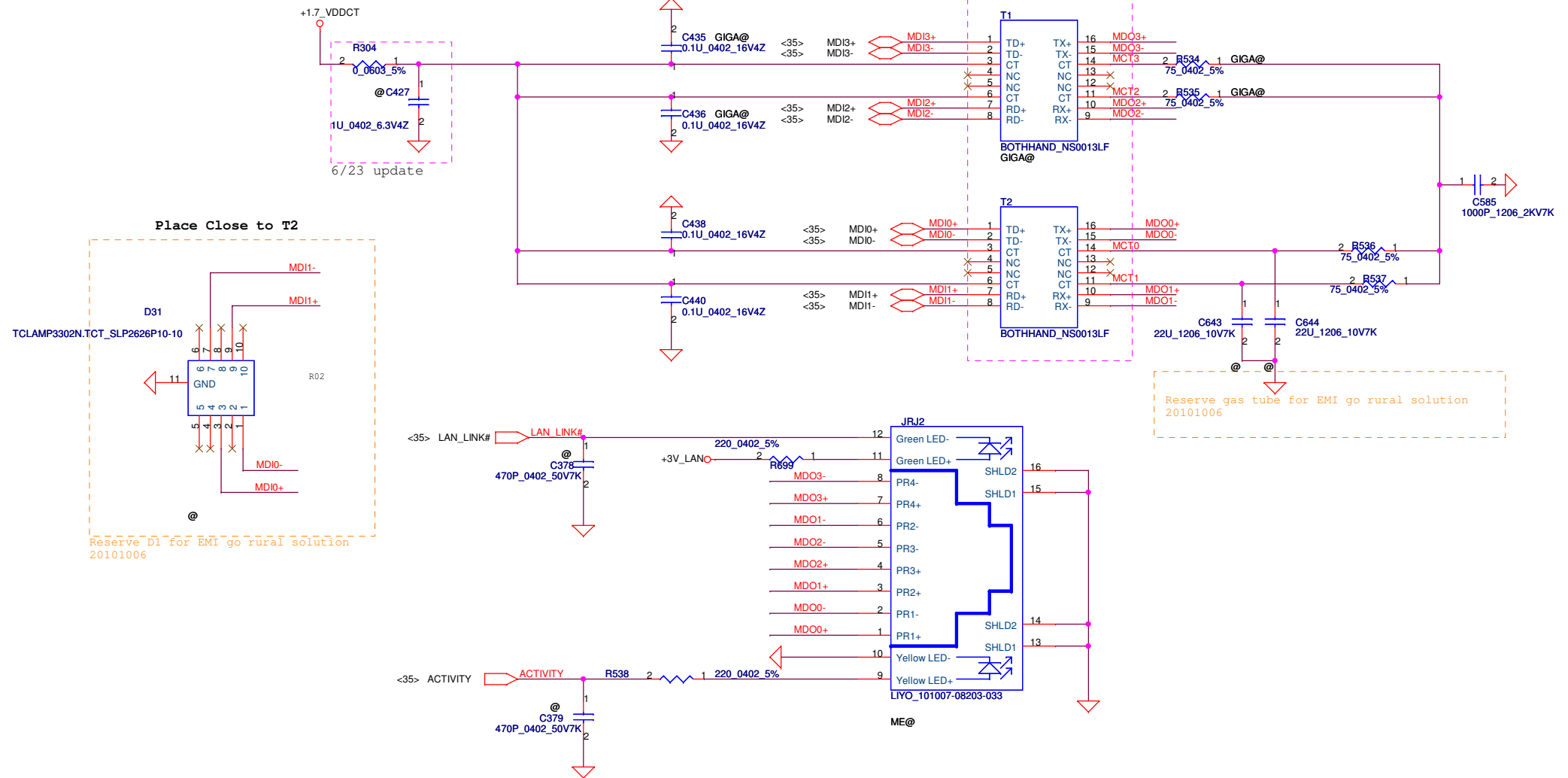
U26 8152@
S IC AR8152-AL1E QFN 40P E-LAN CTRL



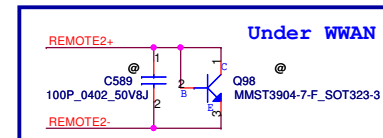
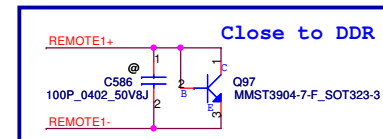
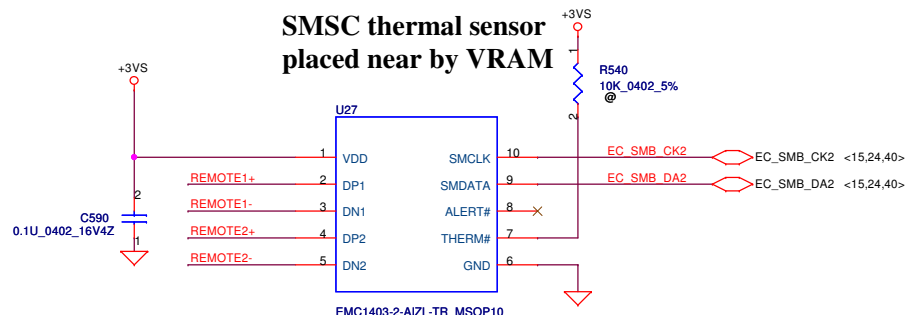
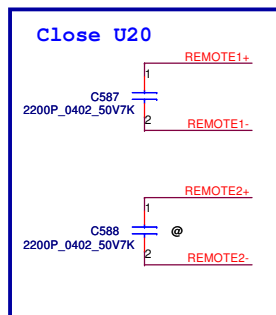
	Pin4	Configure		Pin23	Configure
AR8152	VDDCT_REG	R525	C559 *	CLKREQn	*
AR8151	CLKREQn	*		LED [2]	

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				Document Number	LA-6751P
				Date: Friday, November 26, 2010	Sheet 35 of 59

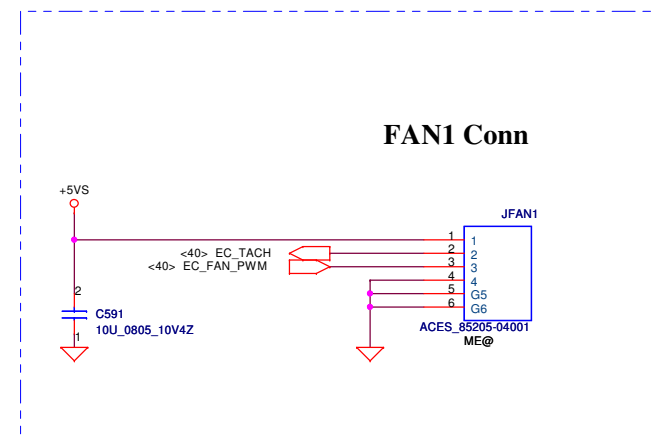
8/23 Change T1,T2 P/N to SP050006E00



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				Size	Document Number
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REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"



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				Date: Friday, November 26, 2010	Rev 0.2
				Sheet 37 of 59	LA-6751P

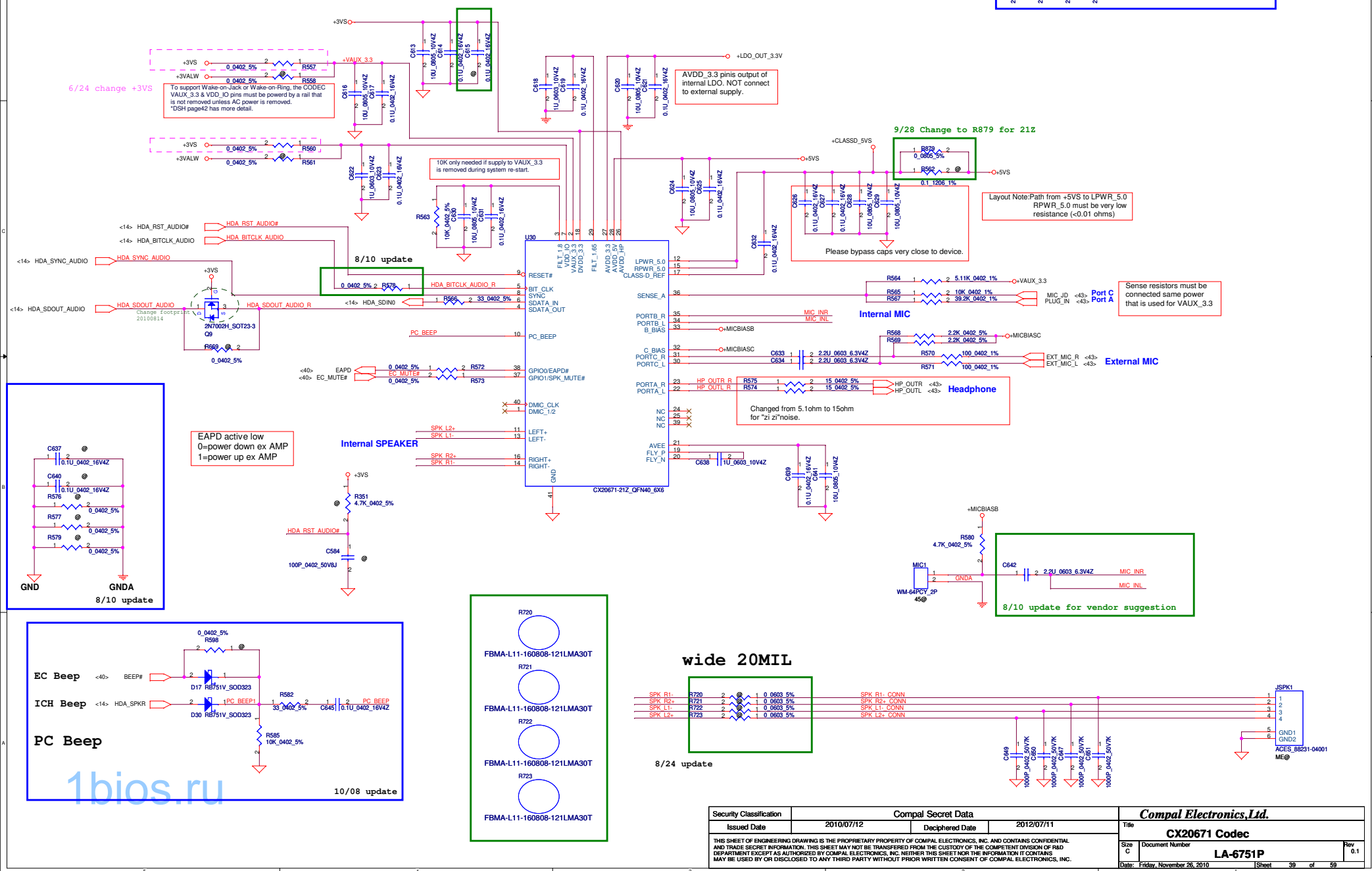
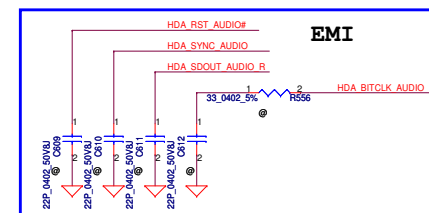
W=80mils



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CX20671
High Definition Audio Codec SoC
With Integrated Class-D Stereo
Amplifier.
An integrated 5 V to 3.3 V Low-dropout
voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout
voltage regulator (LDO).

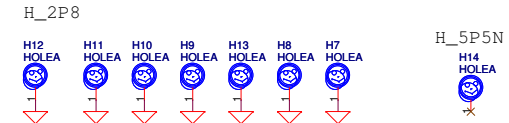
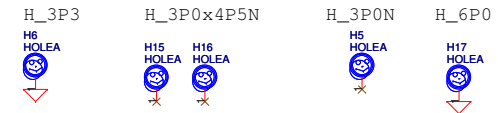
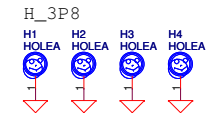
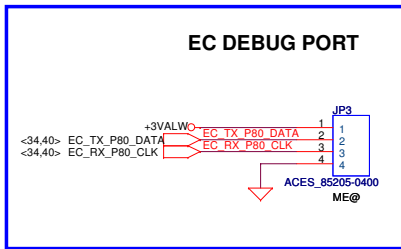
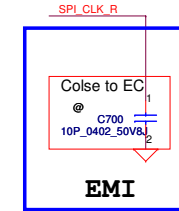
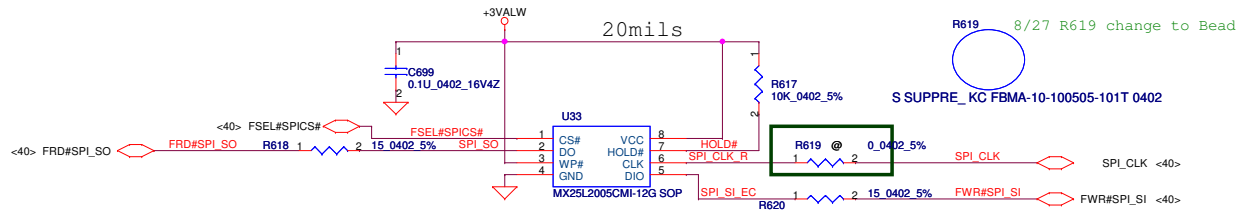
9/27 Update U30 P/N to SA00003K410



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				LA-6751P
Date: Friday, November 26, 2010				Rev 0.1
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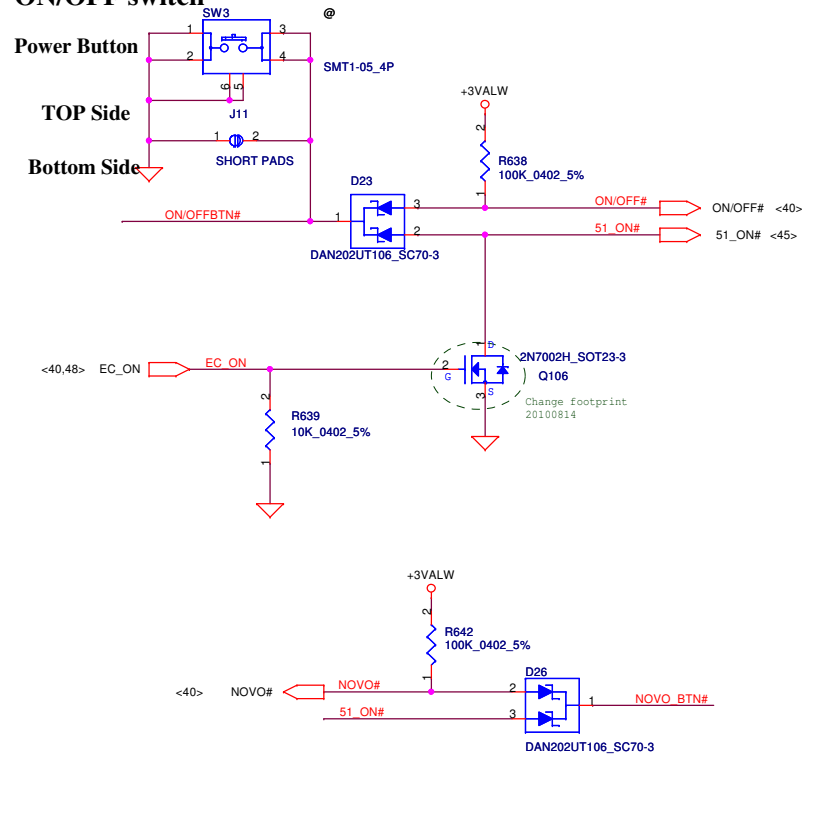


**FOR EC 128KB SPI ROM
(150mil PACKAGE)
SA00003FL10
SA00003JD00**

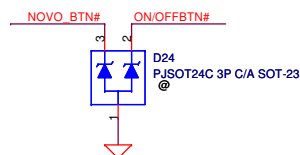
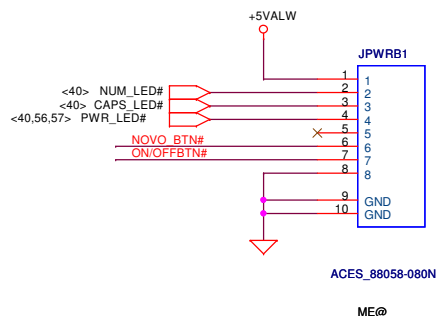


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						Size B	Document Number			Rev 0.2	
						LA-6751P					
						Date:	Friday, November 26, 2010	Sheet	41	of	59

ON/OFF switch



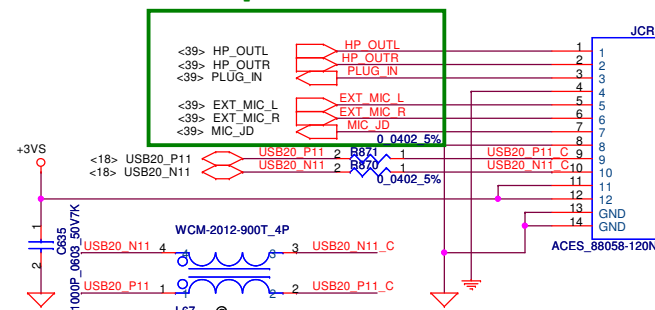
Power Bottom Board Conn. 8pin



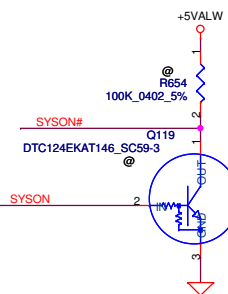
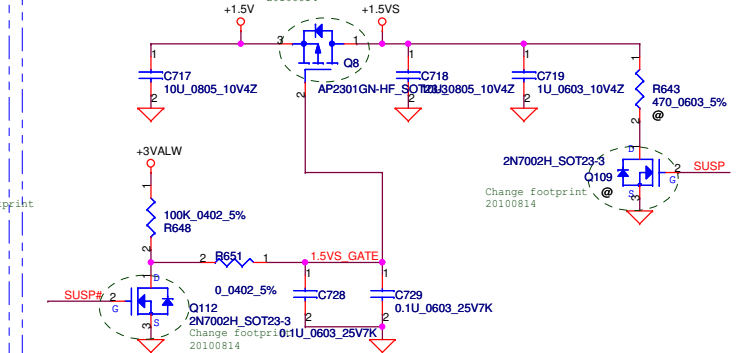
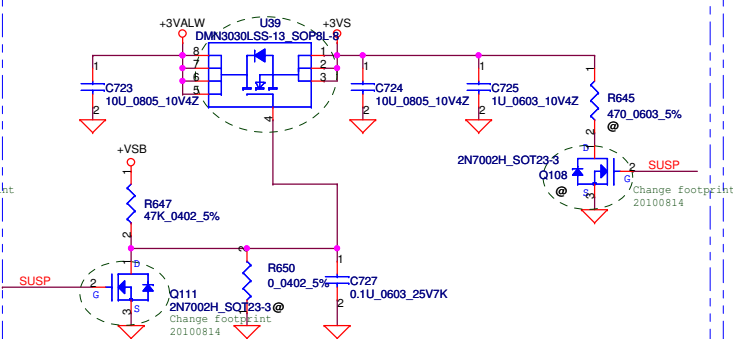
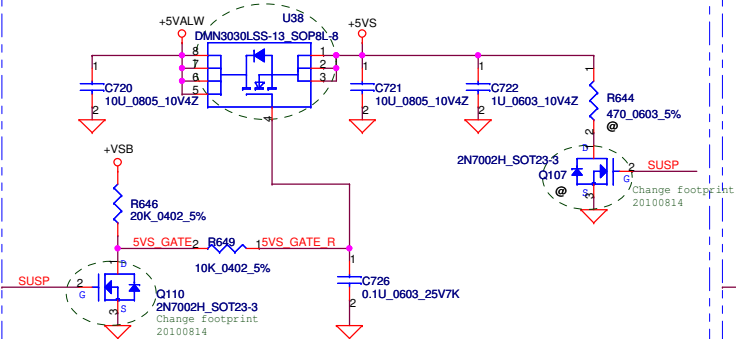
EMI REQUEST 1ST = SCA00000E00
2ST = SCA00000R00

Card Reader/Audio Jack SB CONN

8/5 modify

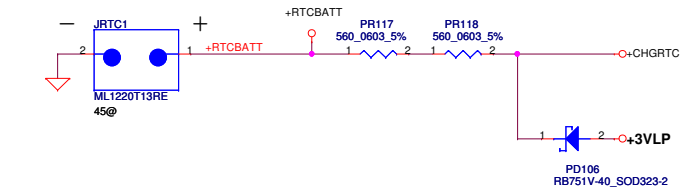
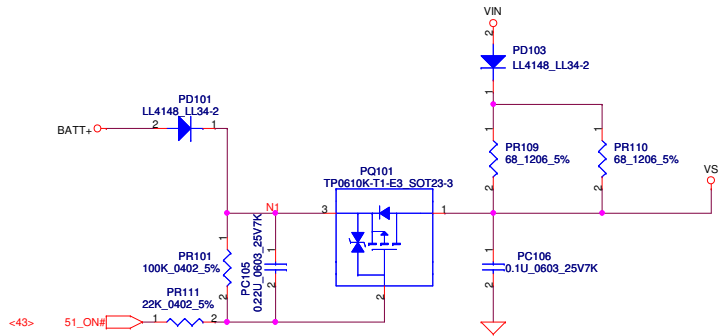
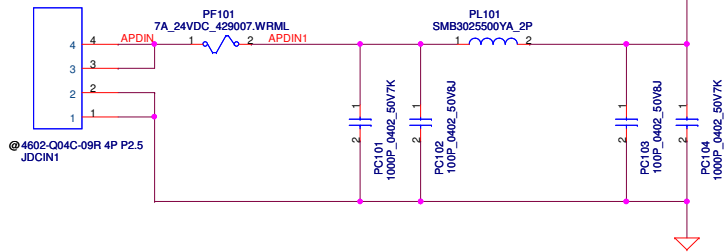


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Size Custom	Document Number			Rev 0.2
Date: Friday, November 26, 2010	Sheet 43 of 59			LA-6751P

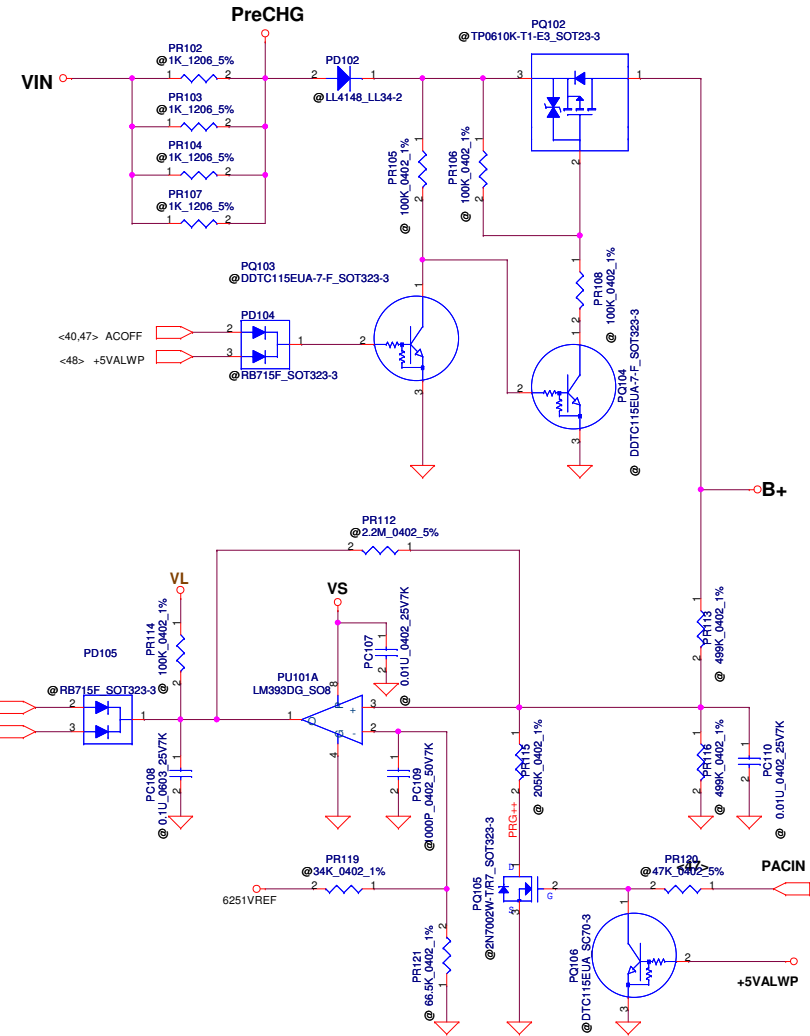


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				Date Friday, November 26, 2010	Rev 0.2
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DC030006J00



Precharge detector
15.97V/14.84V FOR
ADAPTOR



ACIN

Precharge detector			
Min.	typ.	Max.	
L-->H	14.991V	15.381V	15.782V
H-->L	13.860V	14.247V	14.621V

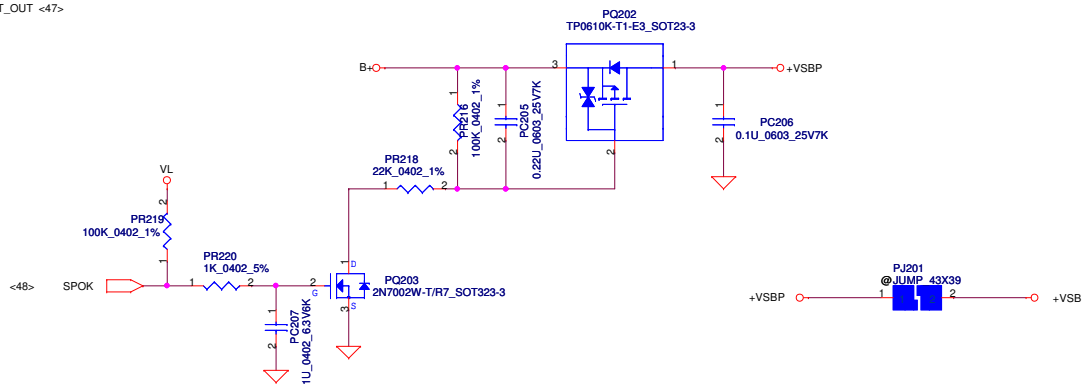
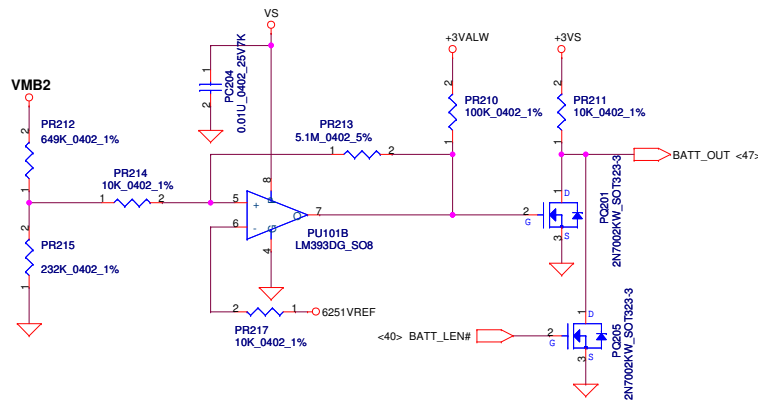
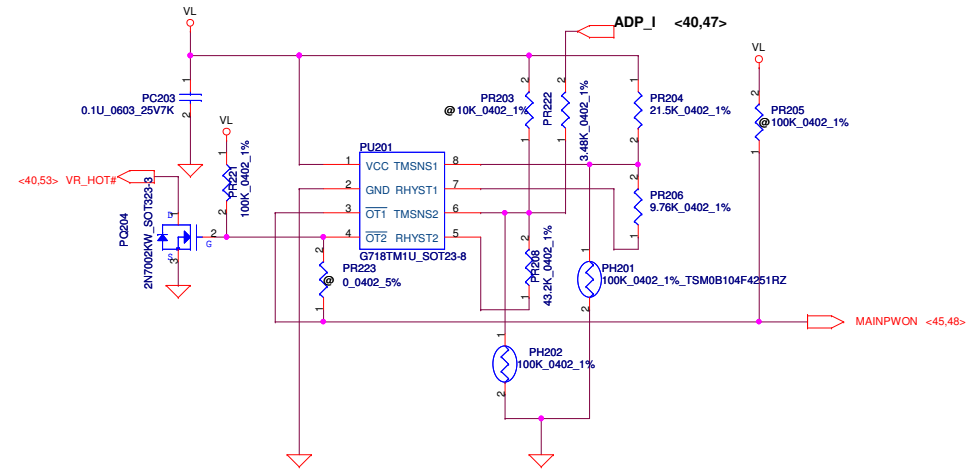
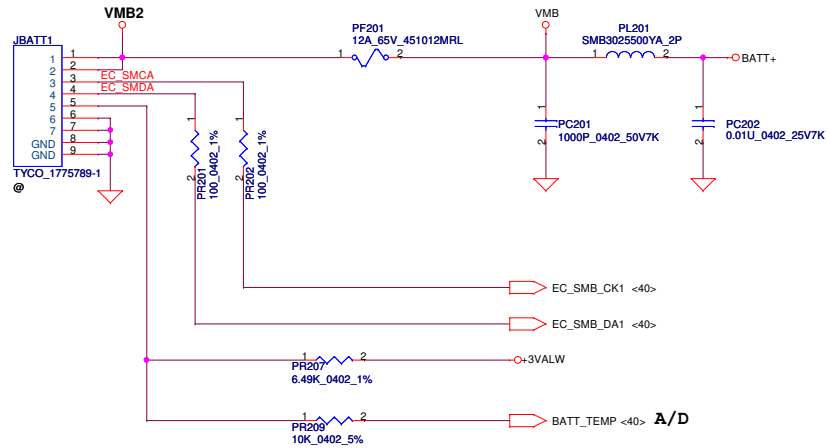
BATT ONLY

Precharge detector			
Min.	typ.	Max.	
L-->H	7.196V	7.349V	7.505V
H-->L	6.138V	6.214V	6.056V

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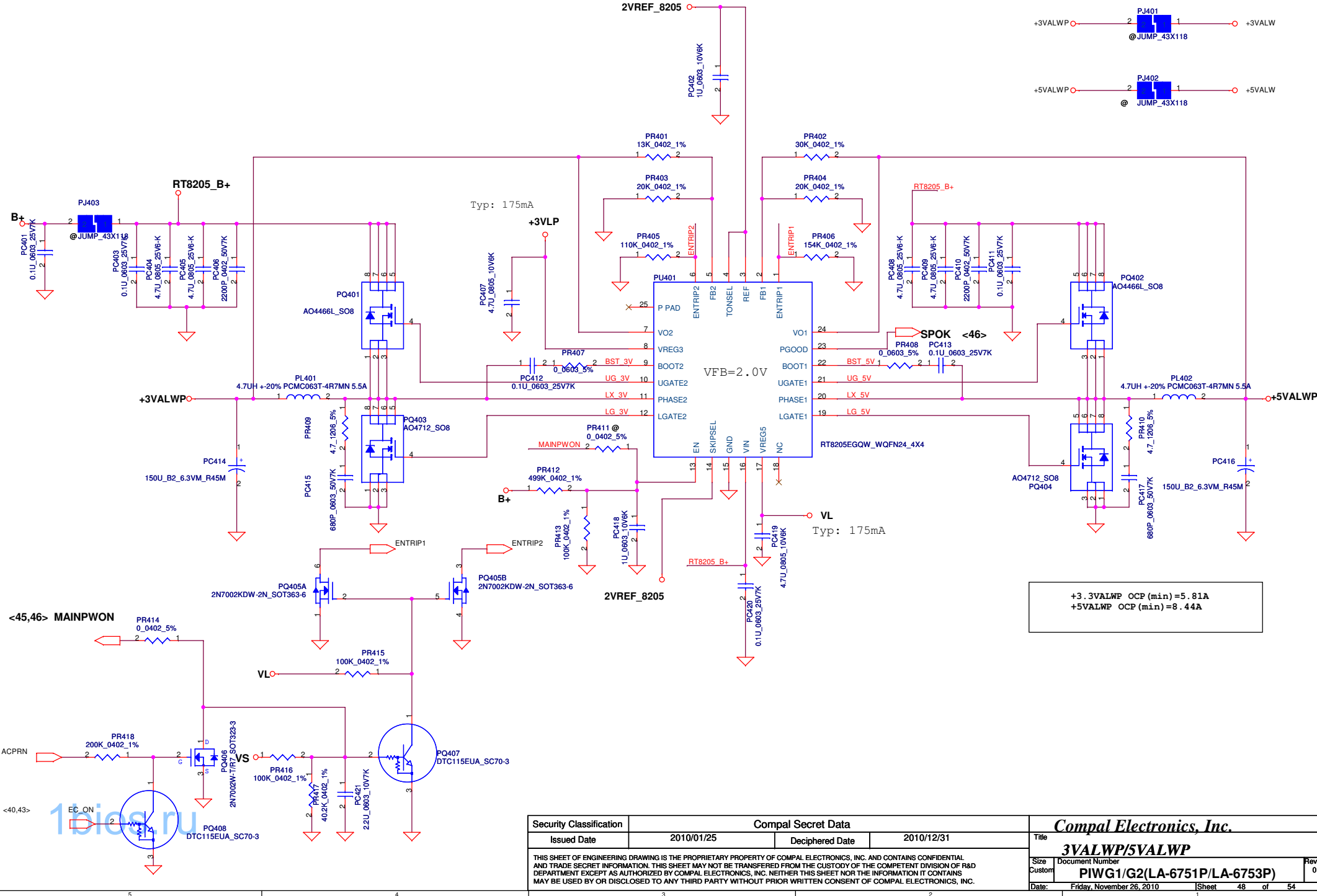
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2010/01/25				Title			
Deciphered Date				2010/12/31				PWR DCIN / Vin Detector /Pre-charge			
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				PIWG1/G2(LA-6751P/LA-6753P)				Rev			
				Date: Friday, November 26, 2010				Sheet 45 of 54			

PH201 under CPU bottom side :
 CPU thermal protection at 92 degree C
 Recovery at 56 degree C

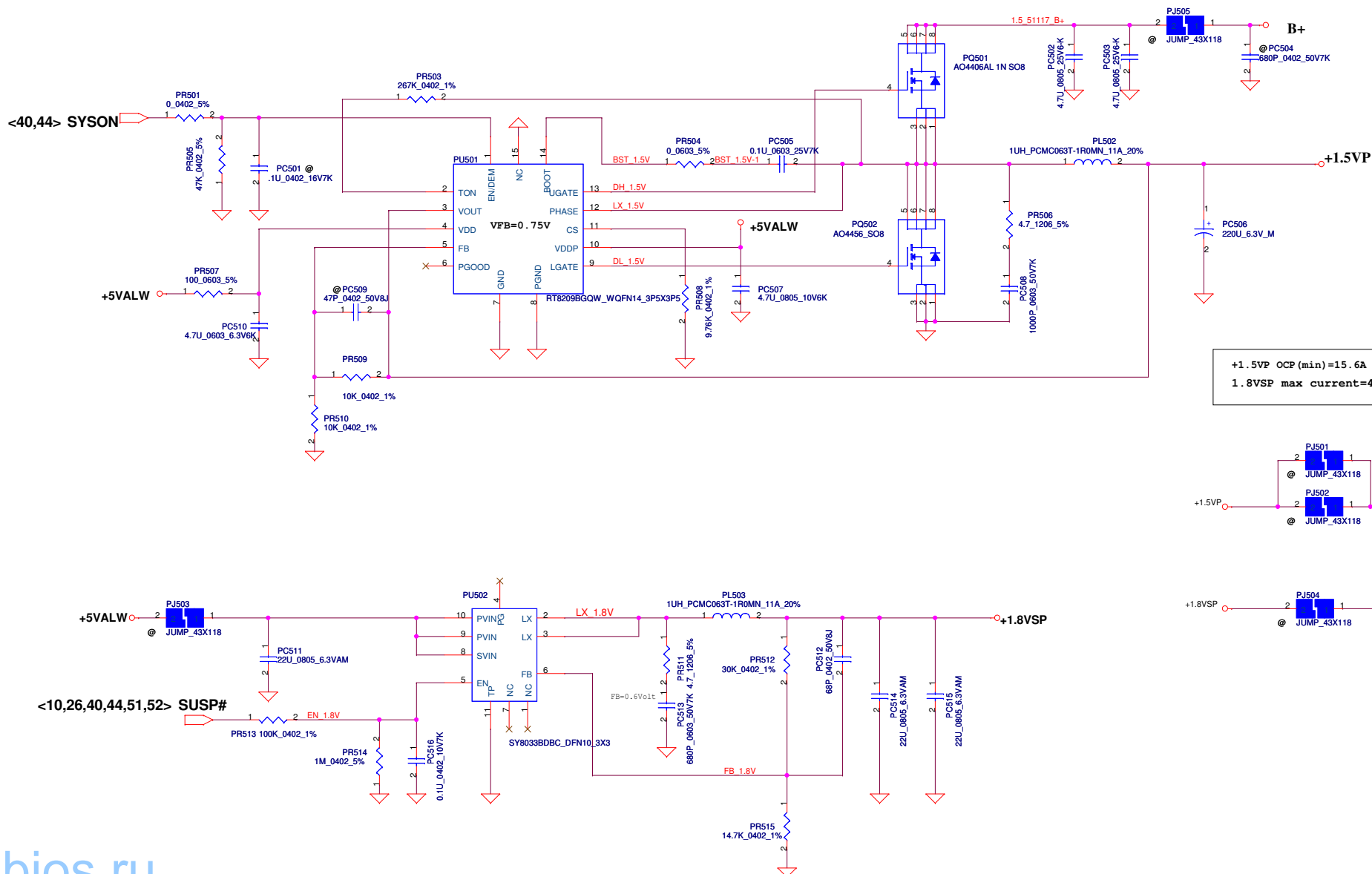


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Size	Custom	Document Number	PIWG1/G2(LA-6751P/LA-6753P)	Rev	0.1
Date:	Friday, November 26, 2010	Sheet	46	of	54

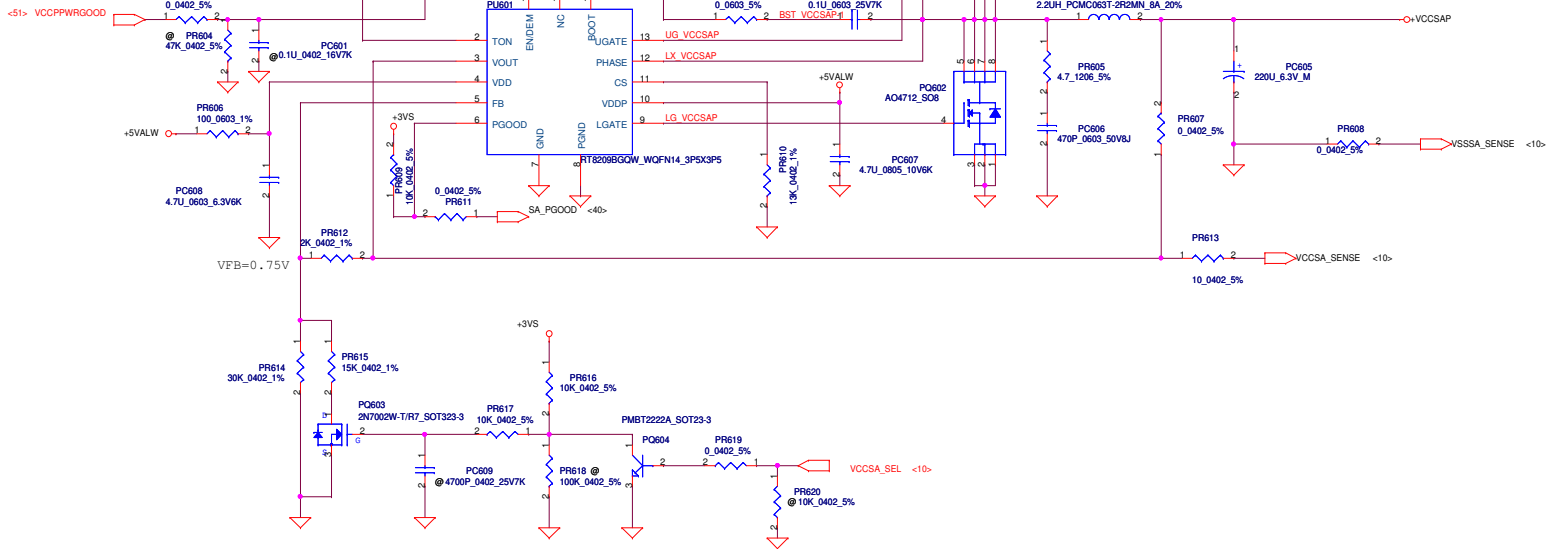
Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO



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				Document Number	Rev 0.1
				Date:	Friday, November 26, 2010
				Sheet	49 of 54



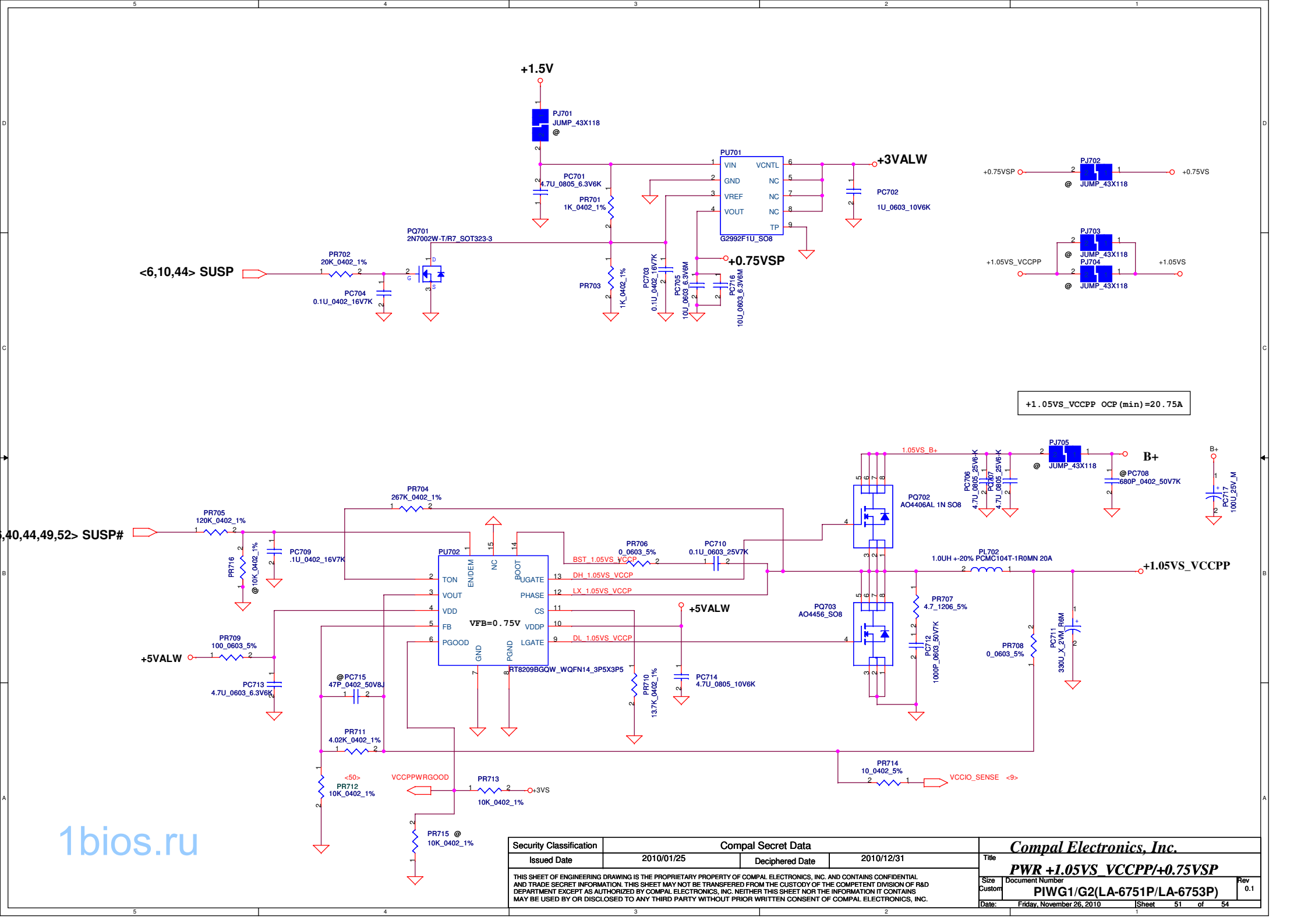
+VCCSAP OCP (min)=6.28A

+VCCSAP OCP (min)=6.28A

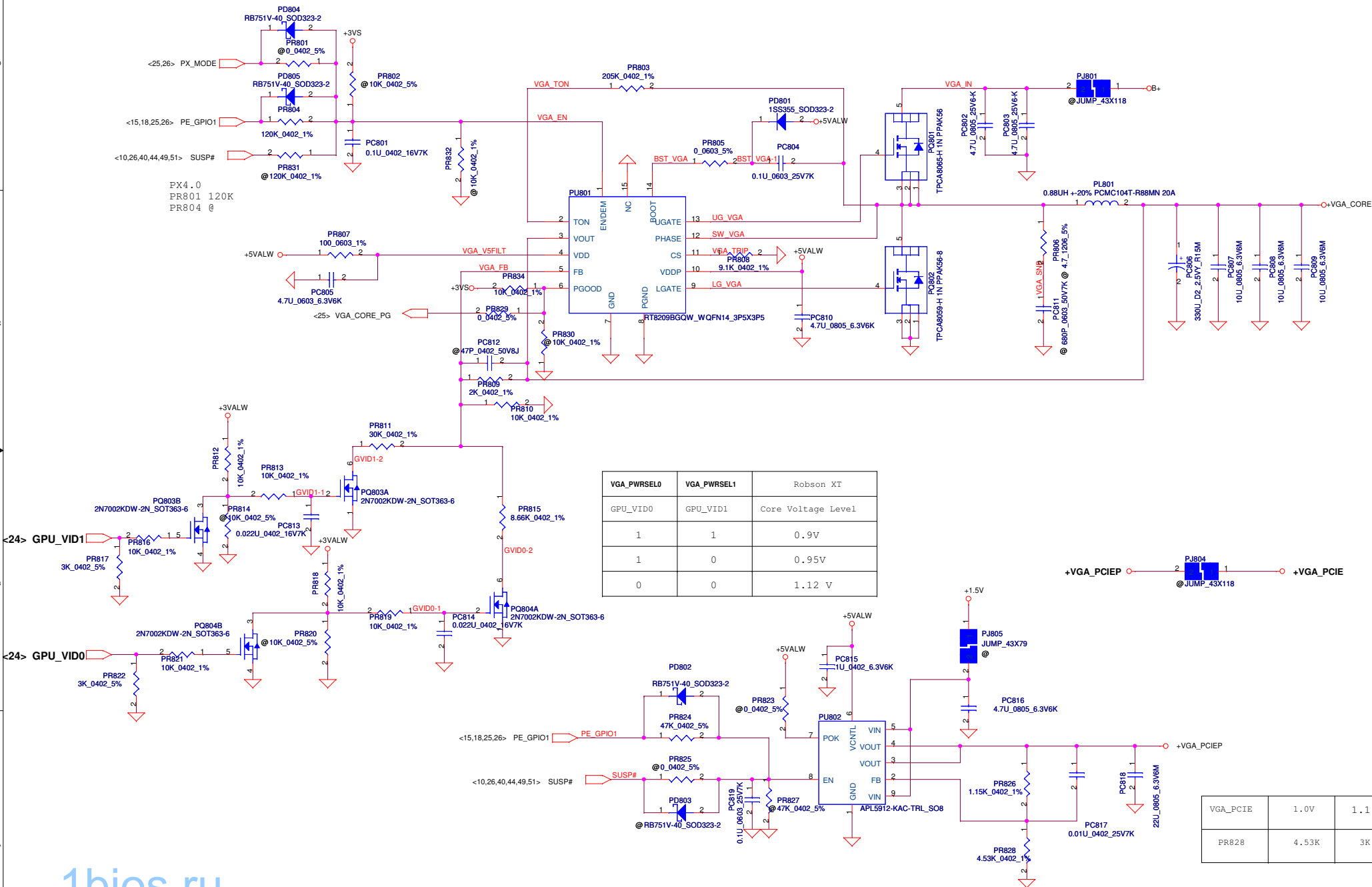
VID[0]	VID[1]	VCCSA Vout	Require on 2011/ 2012	Required
0	0	0.9 V	Yes/Yes	Yes/Yes
0	1	0.8 V	Yes/Yes	Yes/Yes
1	1	0.725V	No/Yes	No/Yes
1	1	0.675V	No/Yes	No/Yes

Note:Use VCCSA_SEL to switch High & Low Level for VID[1]
(ie. VCCSA_SEL) due to the VID[0] is don't care for this setting.

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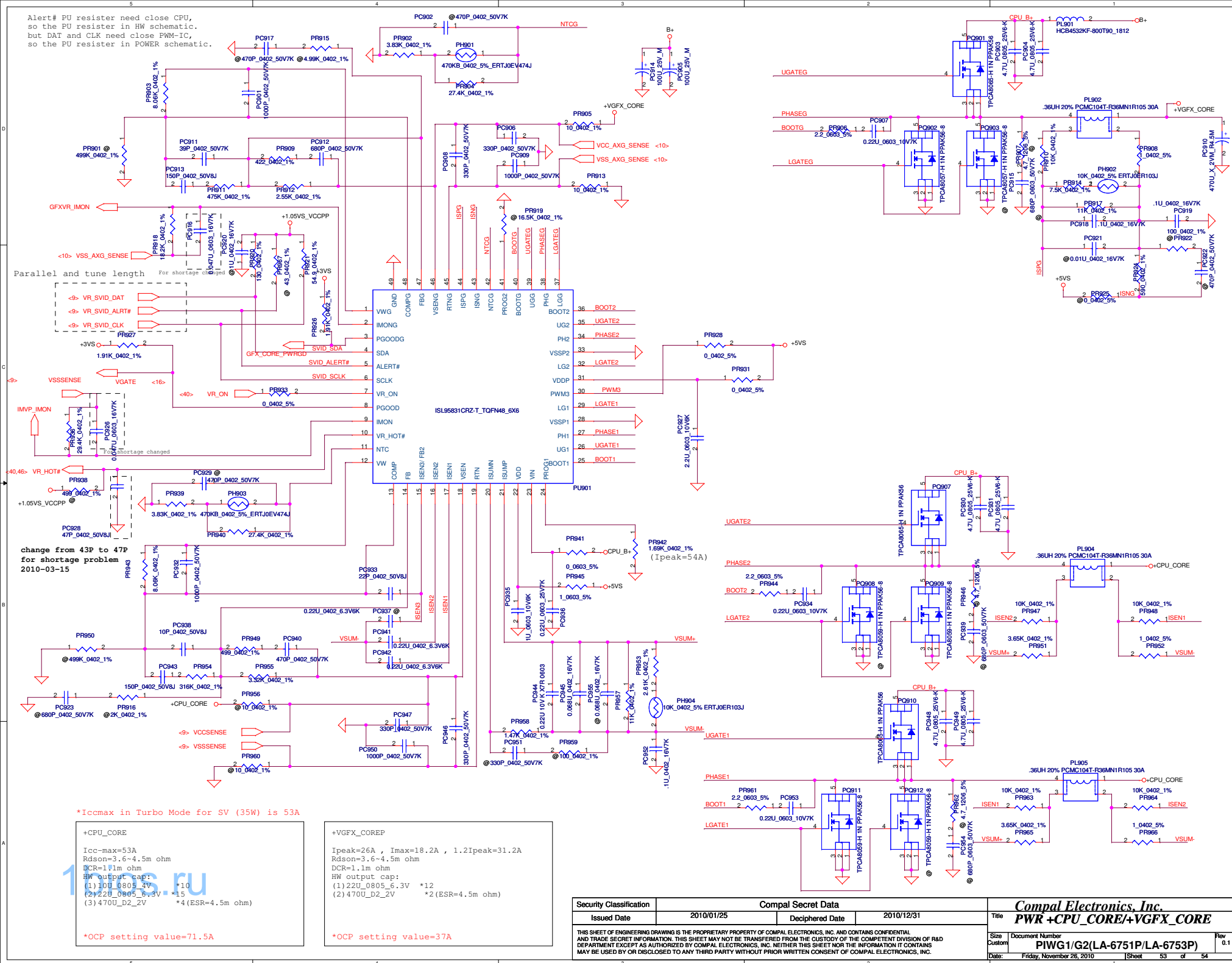


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Alert# PU resister need close CPU,
so the PU resister in HW schematic.
but DAT and CLK need close PWM-IC,
so the PU resister in POWER schematic.



Security Classification	Compal Secret Data			<i>Compal Electronics, Inc.</i> PWR +CPU_CORE/+VGFX_CORE		
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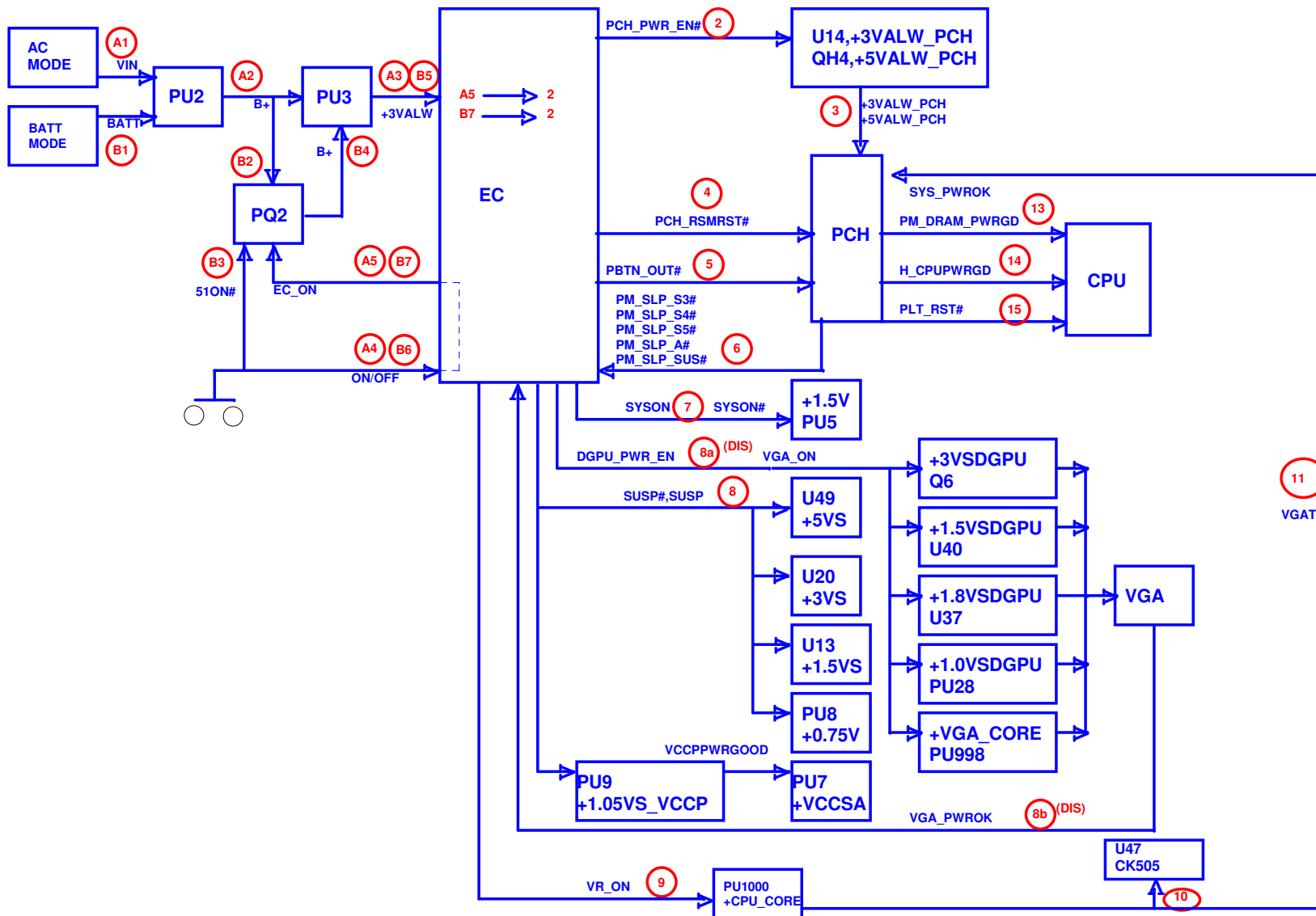
Version change list (P.I.R. List)

Page 1 of 1
for PWR

Item	Reason for change	PG#	Modify List	Date	Phase
1	To reduce charger ripple	47	Add PC323	2010.08.15	DVT
2	HW request for power sequence	51	Change +VGA_PCIE enable signal from PX_MODE to PE_GPIO1 PR804:120K PR831,PR801,PR825 UN-POP PR824:47K PC819:0.2uF	2010.08.15	DVT
3	Change Vboot setting	52	Change PR942 as 4.32K	2010.08.15	DVT
4	Change OCP setting	52	Change PR958 as 1.47K	2010.08.15	DVT
5	Add PC955 for loadline adjust	52	Add PC955	2010.08.15	DVT
6	Reserve pull low resistor	51	Add PR718,PR832	2010.09.29	PVT
7	Remove jump	51	Remove PJ802,PJ803	2010.09.29	PVT
8	Adapter protect circuit	46	Pop PR222,PR208,PH202,PR221,PQ204 Un-Pop PR223,PR203	2010.09.29	PVT
9	EMI Request	47	Remove PJ301 Add PL302 and reserve PC324	2010.09.29	PVT
10					
11					
12					
13					
14					
15					
16					
17					

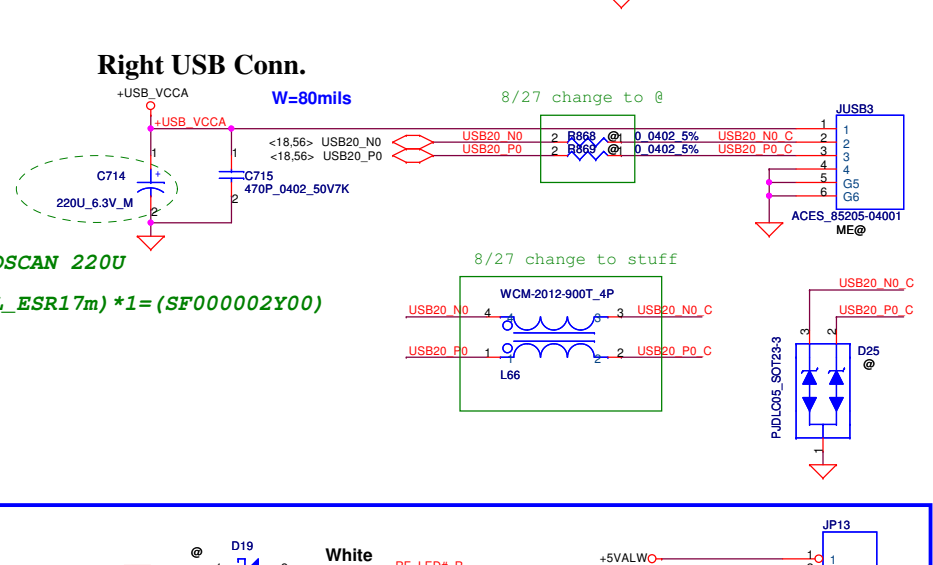
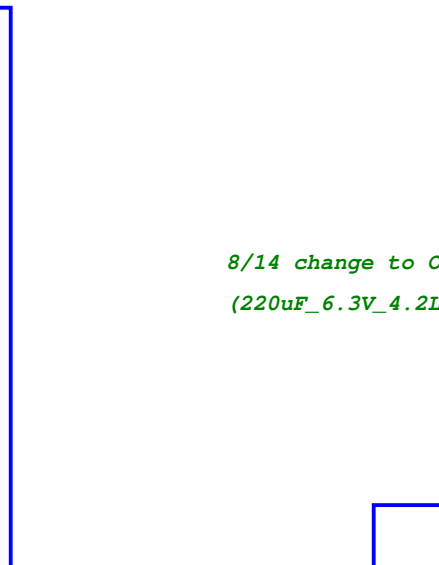
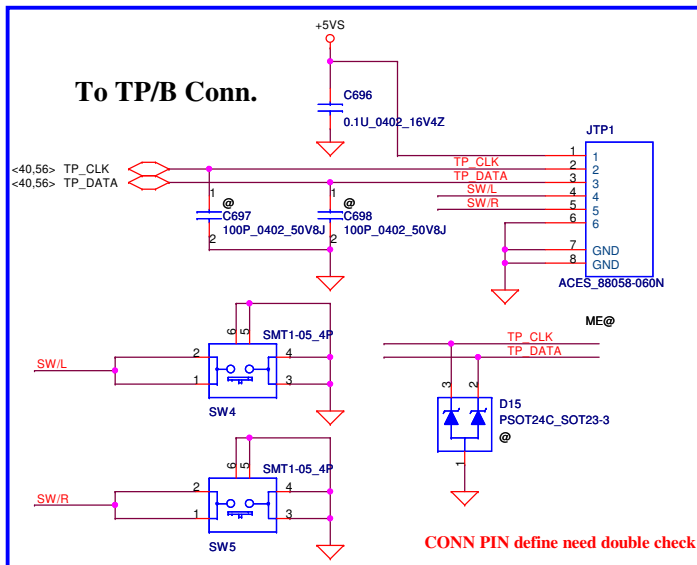
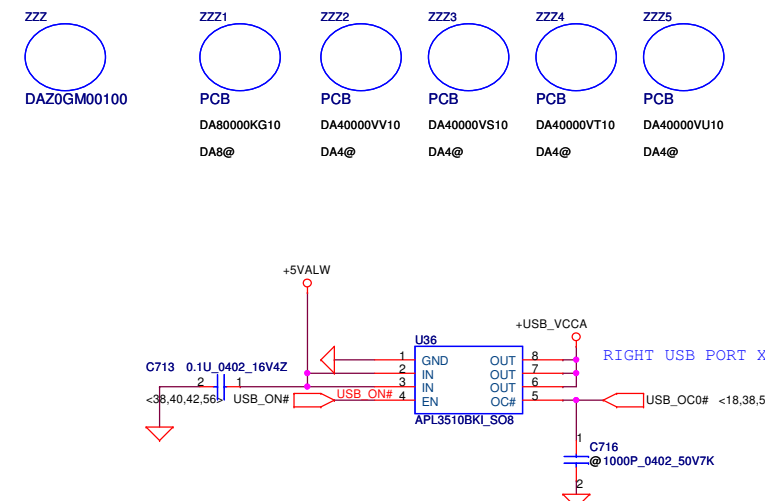
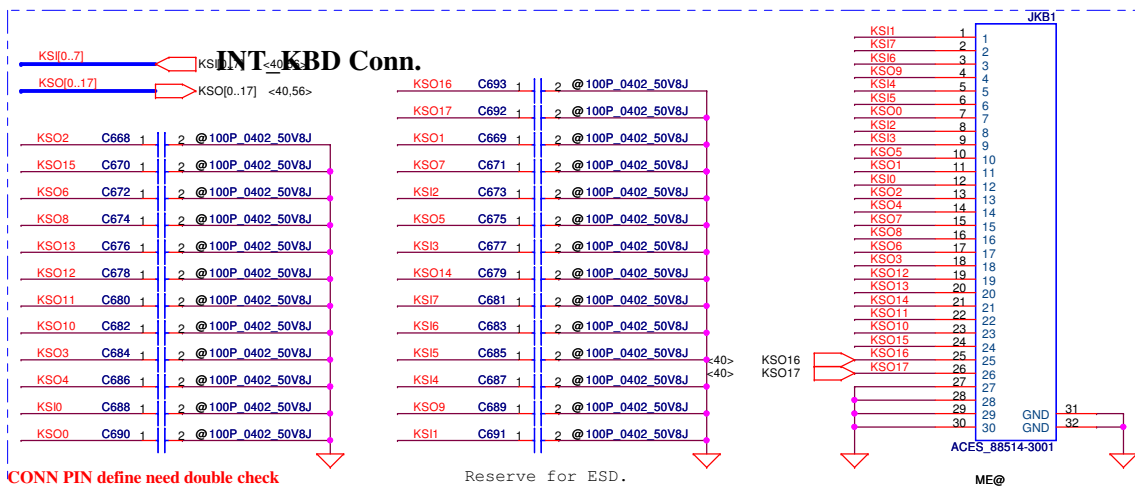
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				PIWG1/G2	
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PHASE	PAGE	Modification list	PURPOSE
0.2	P33	Del RQ51 ~ Q54 Add Q95	For DIS HDMI
0.2	P39	Del J10, C637,C640,R576,R577,R579 change to @ , L40~L43 change to R720~R723 Del C643, R578 , MIC_INR connect MIC_INL , Add R578	For Vendor suggestion and EMI Del C653, R578 connect MIC_INR/L for vendor suggestion , Add R578 for EMI
0.2	P20	Add L75 , R264 , C917, R259 C226 change to @	For intel PDDG update
0.2	P20	Change JCR1 pin define , MIC change with HP	For correct ID
0.2	P9	Add C394, C397 ,C400 ,Add R75	For CPU_CORE power reserved at Bottom side, Add R75 for reserved at cpu side and pwr side
0.2	P26	Add R688 change to 20k, R345 change to 200k , R350 change to 330k , Q65 stuff	For VGA power sequence
0.2	P42	Change C706 P/N to SF000001500	Change to H=6 OSCAN
0.2	P10	Change CI28 to @	For Reserved
0.2	P26	Change D3 change to @	For VGA leakage
0.2	P25	Change BiF_VDDC control pin net name	For correct behavior
0.2	P56	Update JODDI symbol	For ME update drawing
0.2	P16	D29 change to @	For AC detect issue
0.2	P24	R548,R549 change to DIS@	For AC detect issue
0.2	P10	CI28 change to stuff	For test on DVT
0.2	P44	Del Q118, R657	For not need
0.2	P57	Change I5" C714 to OSCAN	For ME Space ok
0.2		Change R513, R516 ,R667 P/N and from 0805 to 0603	For common part
0.2		Change C633, C634 , C642	For common part
0.2		Change D3, D29 P/N and symbol	For common part
0.2		Change U3,U11,U13,U14,U38,U39 P/N and symbol	For common part
0.2		Change U3,U11,U13,U14,U38,U39 P/N and symbol	For common part
0.2		Change Q8,Q65,Q80,Q83,Q99,Q104 P/N and symbol	For common part
0.2		Change Q1,Q37,Q93 P/N and symbol	For common part
0.2		Change Q94, Q95 P/N and symbol	For common part
0.2		Change Q3,Q4,Q7,Q9,Q66,Q67,Q68,Q73,Q74,Q75,Q76,Q77,Q78, Q79,Q82,Q85,Q86,Q87,Q102,Q106,Q107,Q108,Q109,Q110,Q111,Q112,Q113,Q114,Q115,Q116 P/N and symbol	For common part
0.2	P43	Change C635 part and change to @	For EMI
0.2	P18	Reserved R551	Reserved
0.2	P9	Change C53,C85,C86,C87 ,C394,C397,C400 to stuff and change C48,C80,C81,C82,C89,C90,C91 to @	For CPU_CORE
0.2	P10	Change C110,C111,C112,C113 to stuff	For VGFX_CORE
0.2	P56	Change LED1/LED3/LED4 P/N to SC50000A300	Change P/N
0.2	P36	Change T1,T2 P/N to SP050003N00	For test pass part
0.2	P40	Change R611,R740,C93 to stuff and change Y5,C347,C367 to @ Change R695 to 18K, Q37 change to @, R747 change to stuff,	For SUS_CLK R695 for Board ID, Q37, R747 for VR_HOT
0.2	P41	Change U33 P/N to SA00003FL10	For BIOS ROM
0.2		Change C509,C511,C635 to stuff	For EMI request
0.2	P56	Change I4" C714 P/N to SGA00002N80	For Sourcer request
0.2	P39	Change R720,R721,R722,R723 P/N to SM01000BZ00(Bead), and Change C647,C649,C650,C651 to Stuff	For EMI request
0.2	P19	Change R303 to Stuff, and change R542 to @	For BIOS ESATA detect function
0.2	P56	Change U32 P/N to SA000031C00	For common part
0.2	P36	Change T1,T2 P/N to SP050006E00	For correct part
0.2	P10	R688 change to stuff , R687 ,Q7 change to @	For S3 power reduction
0.2		Change R660,R661,R862,R863,R864,R865,R868,R869 to @ , change L63,L64,L65,L66 to stuff , change R619 to Bead (SM01000DI00)	For EMI
0.2	P20	Change L75 symbol	For common part

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				LA-6751P	
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PHASE	PAGE	Modification list	PURPOSE
0.3	P10	Update Q5 symbol	For update symbol
0.3	P33	Add F2	For safty request
0.3	P39	Update U30 P/N to SA00003K410 and Add R879	For Audio update to 21Z
0.3	P10	Change C128 to D2 size and e	Change size for M/E issue
0.3	P14	Add reserve R878	For Intel DG 1.5
0.3	P37	C592 change P/N to SF000001500 (H=6)	For ME Z high ok
0.3	P25	Update Q69-Q72 to A03414 ,D28 R873 change to BACO@ , U40 change to @	For PX4.0
0.3	P28	Add reserve C94	For reserve VGA_CORE
0.3	P29	R369 P/N change to SD034100A80	For GP part
0.3	P18	R553,R691,R684,R682,U12 change to PX@	For PX 4.0
0.3	P6	Reserved R880 to SYS_PWROK	Follow ORB
0.3	P10	R62,R63 change to 1K	Follow CRB
0.3	P19	R303 change to @, Change M/B ID to PX4.0	For ESATA and PX4.0
0.3	P25	Q69-Q72 change to BACO @	For PX4.0
0.3	P26	R719 change to stuff, R744 change to @ , R677 change to BACO@	For PX4.0
0.3	P33	R483,R484 change connect to +5V_HDMI_F	For Add F2
0.3	P37	Change U27 P/N to SA000046C00	For Fintek
0.3	P40	Change R594 pull high to +5VALW	For leakage issue
0.3	P19	R881 change to Dstuff, R244 change to @	For intel MRC Rev0.9
0.3	P14	R878 change to stuff	For intel DG 1.5
0.3	P31	Del R432	For non-used part
0.3	P36	Reserved D31 , C643 , C644	For reserved EMI parts
0.3	P37	Del R581	For non-used part
0.3	P38	Del R550	For non-used part
0.3	P38	Change C592 P/N to SF000002Y00	For M/E Z high limlt
0.3	P39	Del R584, R586 , R587	For non-used part
0.3	P40	Change R600, R604 to 2.2K Change R695 to 8.2k	Change R600, R604 for Battery SMBus, R695 for Board ID
0.3	P42	Del R583	For non-used part
0.3	P6	Reserved R882 connect to PCH_PWROK	Reserved for intel
0.3	P56	R765 change to 300 ohm	For LED
0.3	P25	R324, R744 , R674 change DIS@	For DIS only sku