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Model Name : EA/EG50_CX (Z5WE1)

File Name : LA-9535P

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EA/EG50_CX (Z5WE1) M/B Schematics Document

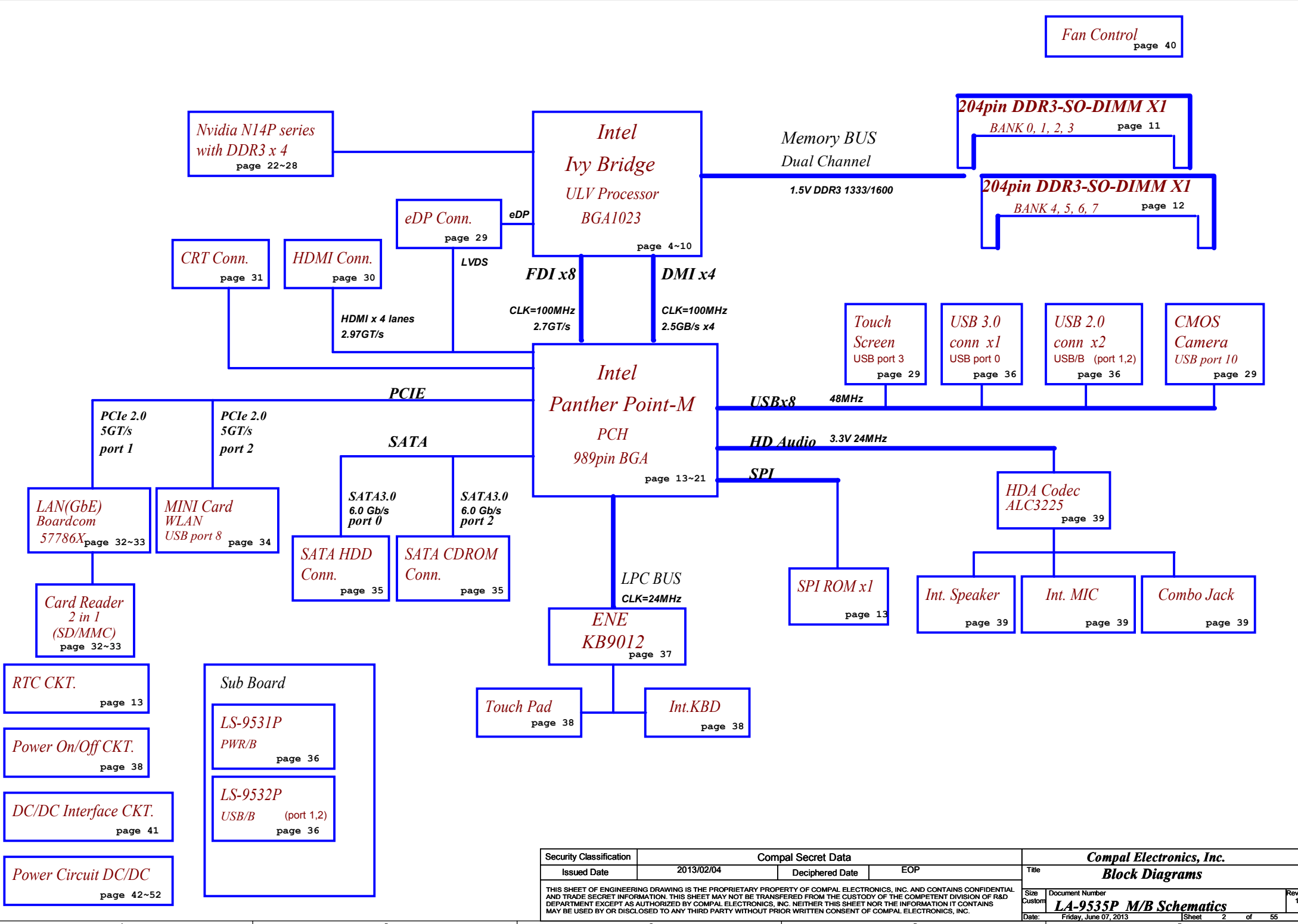
Intel Ivy Bridge ULV Processor + Panther Point PCH

Nvidia N14M-GE & N14P-GV2

2013-06-07

REV:1.0

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Fan Control
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Nvidia N14P series
with DDR3 x 4
page 22~28

Intel
Ivy Bridge
ULV Processor
BGA1023
page 4~10

Memory BUS
Dual Channel

204pin DDR3-SO-DIMM X1
BANK 0, 1, 2, 3
page 11

204pin DDR3-SO-DIMM X1
BANK 4, 5, 6, 7
page 12

1.5V DDR3 1333/1600

CRT Conn.
page 31

HDMI Conn.
page 30

eDP Conn.
page 29

HDMI x 4 lanes
2.97GT/s

LVDS

FDI x8

CLK=100MHz
2.7GT/s

DMI x4

CLK=100MHz
2.5GB/s x4

Intel
Panther Point-M
PCH
989pin BGA
page 13~21

Touch
Screen
USB port 3
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conn x1
USB port 0
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USB 2.0
conn x2
USB/B (port 1,2)
page 36

CMOS
Camera
USB port 10
page 29

PCIE

PCIe 2.0
5GT/s
port 1

PCIe 2.0
5GT/s
port 2

SATA

SATA3.0
6.0 Gb/s
port 0

SATA3.0
6.0 Gb/s
port 2

LAN(GbE)
Boardcom
57786X
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MINI Card
WLAN
USB port 8
page 34

Card Reader
2 in 1
(SD/MMC)
page 32~33

SATA HDD
Conn.
page 35

SATA CDROM
Conn.
page 35

USBx8
48MHz

HD Audio
3.3V 24MHz

SPI

HDA Codec
ALC3225
page 39

LPC BUS
CLK=24MHz

ENE
KB9012
page 37

SPI ROM x1
page 13

Int. Speaker
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Int. MIC
page 39

Combo Jack
page 39

RTC CKT.
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Power On/Off CKT.
page 38

DC/DC Interface CKT.
page 41

Power Circuit DC/DC
page 42~52

Sub Board

LS-9531P
PWR/B
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LS-9532P
USB/B (port 1,2)
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Touch Pad
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Int.KBD
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+0.75VS	+0.675VSP to +0.675VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VSDGPU	+1.0VSDGPU switched power rail for GPU	ON	OFF	OFF
+0.95VSDGPU	+0.95VSDGPUP to +0.95VSDGPU switched power rail for CPU	ON	OFF	OFF
+1.5V	+1.35VP to +1.35V power rail for DDRIML	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.5VSDGPU	+1.5VSDGPUP to +1.5VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.8VS	+3VS to 1.8V switched power rail to CPU	ON	OFF	OFF
+1.8VSDGPU	+1.8VS to +1.8VSDGPU switched power rail for GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VLP	B+ to +3VLP power rail for suspend power	ON	ON	ON
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+3VSDGPU	+3VS to +3VSDGPU switched power rail for GPU	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.				

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X	VGA Internal Thermal Sensor	1001 111x (0x9E)

EC SM Bus2 address

PCH SM Bus address

Device	Address
ChannelA DIMM0	1001 000x JDIMM1
ChannelB DIMM1	1001 010x JDIMM2

BOM Config

UMAO: EDP@/IOAC@/BL@/EMC@/UMAO@/
DIS GV2: EDP@/IOAC@/BL@/EMC@/VGA@/
DIS GE: EDP@/IOAC@/BL@/EMC@/VGA@/

CPU config
CPU config + X76
CPU config + X76

GC6@/N14PGV2@/GV2GT@/8X@/
GC6@/N14MGE@/8X@/

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%				
Ra/Rc/Re	100K +/- 5%				
Board ID	Rb / Rd / Rf	VAD_BID_min	VAD_BID_typ	VAD_BID_max	
0	0	0 V	0 V	0 V	
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	
4	56K +/- 5%	1.036 V	1.185 V	1.264 V	
5	100K +/- 5%	1.453 V	1.650 V	1.759 V	
6	200K +/- 5%	1.935 V	2.200 V	2.341 V	
7	NC	2.500 V	3.300 V	3.300 V	

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

USB Port Table

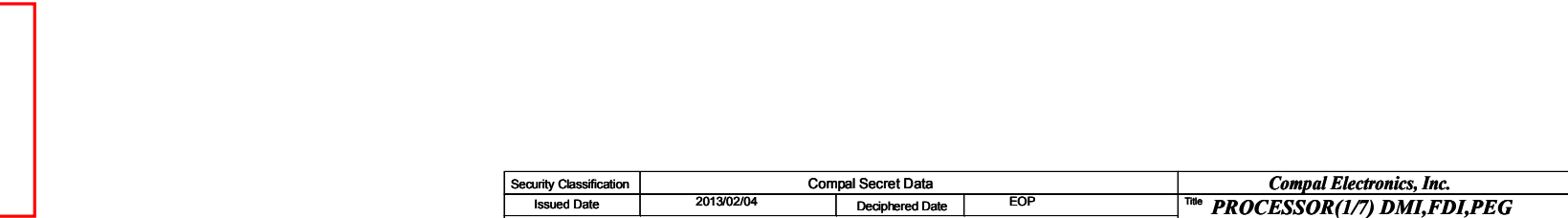
USB 2.0	Port	3 External USB Port
EHCI1	0	USB Port(Left 3.0)
	1	USB Port(Right 2.0)
	2	USB Port(Right 2.0)
	3	Touch Screen
	4	
	5	
	6	

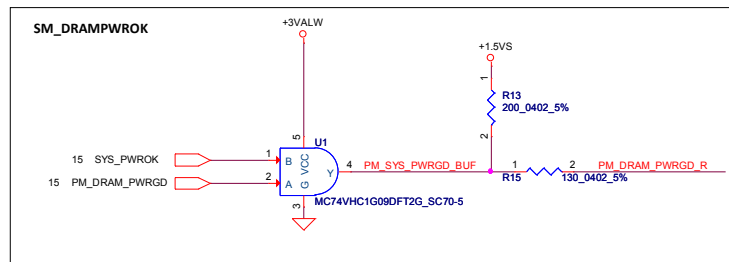
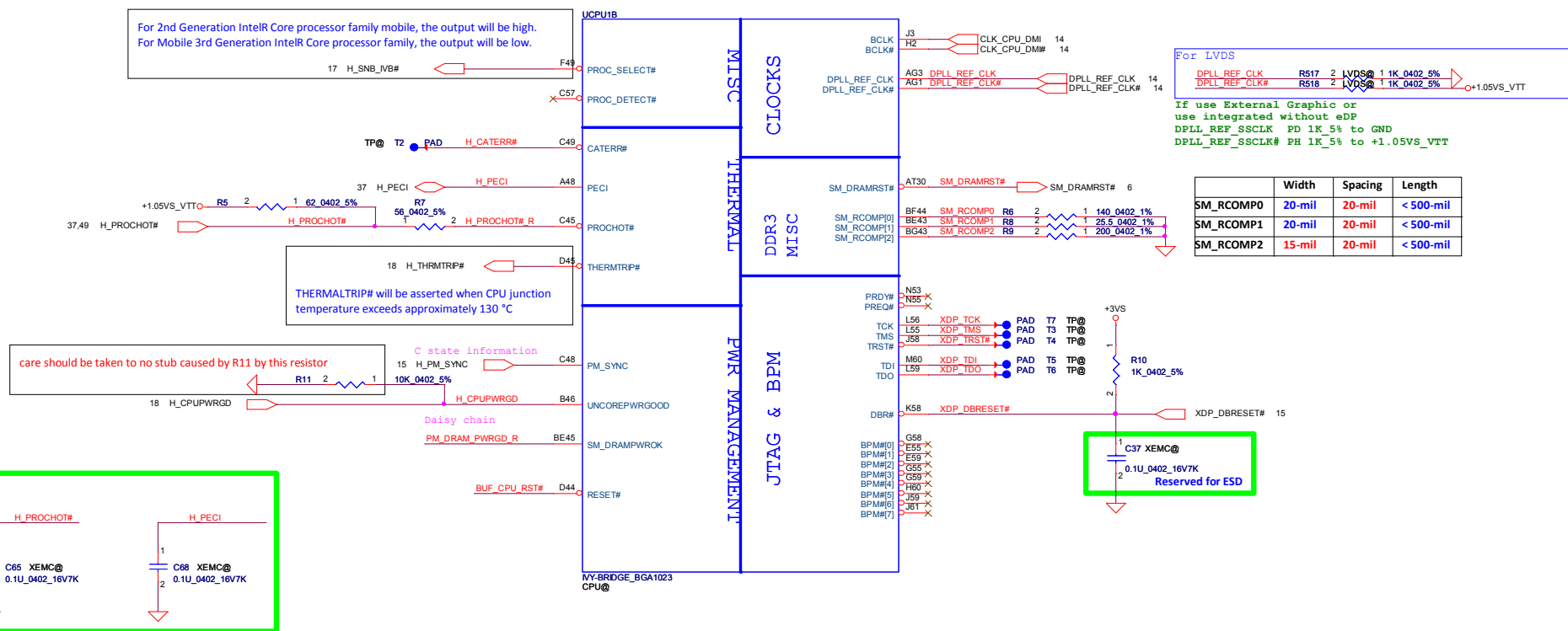
USB 2.0	Port	
EHCI2	8	Mini Card (WLAN+BT)
	9	
	10	Camera
	11	
	12	
	13	

USB 3.0	Port	
XHCI	0	USB Port(Left 3.0)
	1	
	2	
	3	

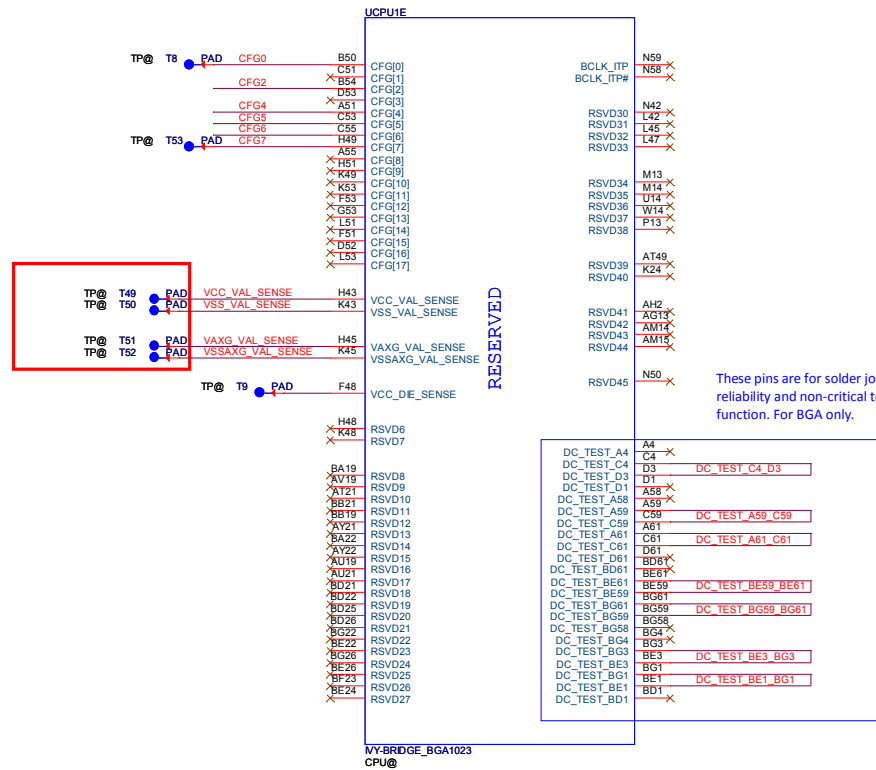
BTO Option Table

BTO Item	BOM Structure
Unpop	@
Connector	CONN@
PCH RTC CMOS	SP@
TEST PAD	TP@
Unpop SPI2	SPI2@
Unpop CPU	CPU@
Unpop GPU	GPU@
Unpop VRAM	VRAM@
Back light	BL@
IOAC	IOAC@
Celeron 847	847@
Celeron 1007	1007@
I3-3227M	I33227@
I5-3337M	I53337@
I7-3537M	I73537@
UMA ONLY GPIO	UMAO@
EDP	EDP@
LVDS	LVDS@
EMC POP	EMC@
EMC NON POP	XEMC@
N14M-GE option	N14MGE@
N14P-GT option	N14PGT@
N14P-GV2 option	N14PGV2@
N14P-GT/GV2 Strap	GV2GT@
VGA SKU	VGA@
VRAM x 8pcs	128@
PEG 16X	16X@
PEG 8X	8X@
GC6	GC6@
NON GC6	NGC6@

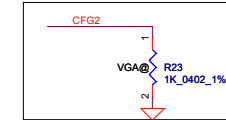




	Width	Spacing	Length
SM_RCOMP0	20-mil	20-mil	< 500-mil
SM_RCOMP1	20-mil	20-mil	< 500-mil
SM_RCOMP2	15-mil	20-mil	< 500-mil



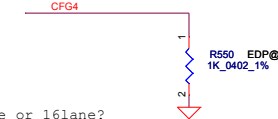
CFG Straps for Processor



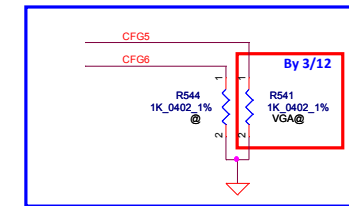
current placement need to support
PEG bus lan reversal

PCIe Static x16 Lane Numbering Reversal

CFG2	1: (Default)Normal Operation Lane # definition matches socket pin map definition
*0:	Lane Reversed



check VGA 8lane or 16lane?



eDP Enable Strap

CFG4	1: (Default)Disable
*0:	Enable

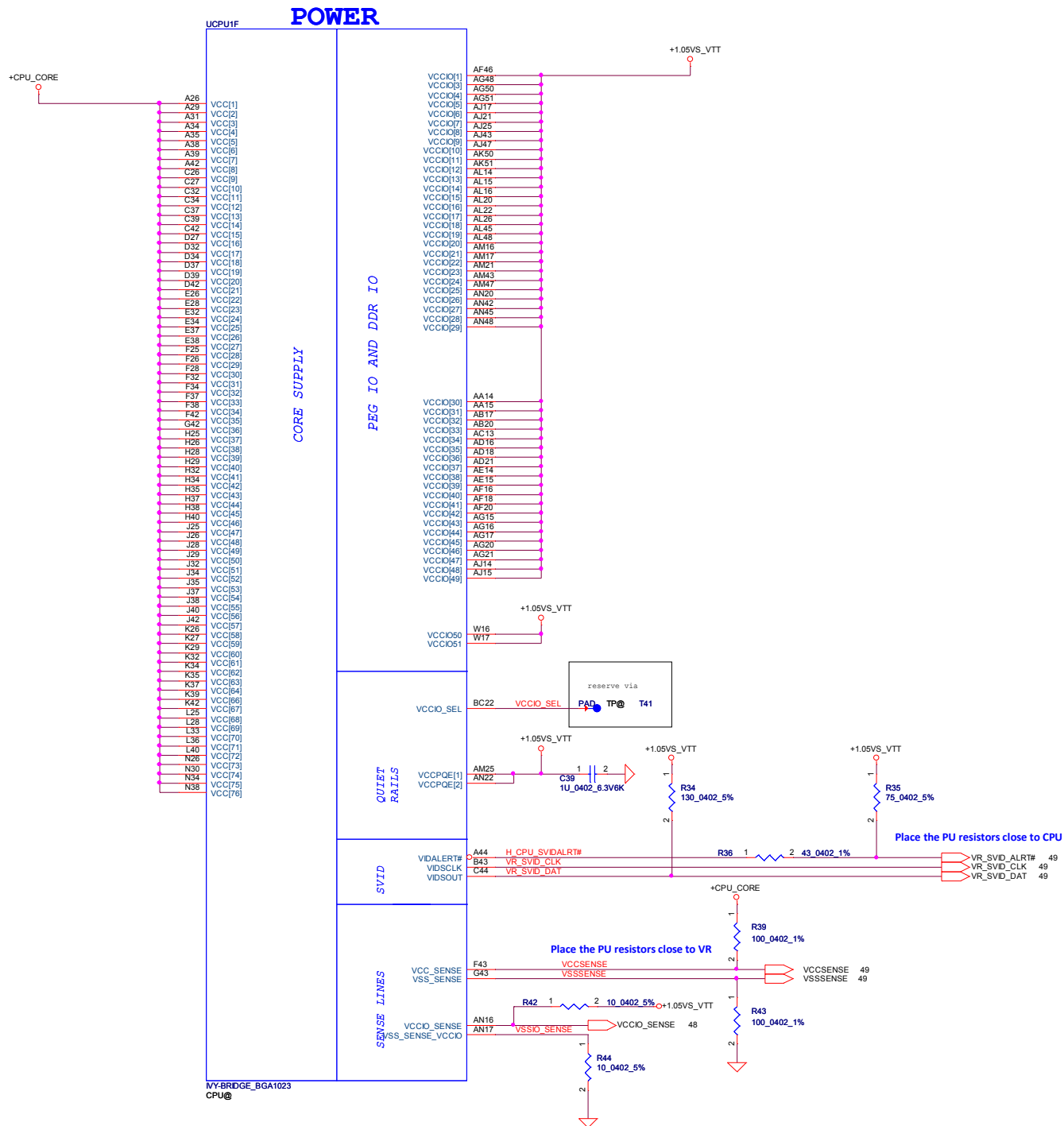
PCIe Port Bifurcation Straps

CFG[6:5]	11: (Default) 1x16 PCI Express
*10:	2x8 PCI Express
01:	Reserved
00:	1x8,2x4 PCI Express

PEG DEFER TRAINING Tacoma_Fall2 1.0 P.12

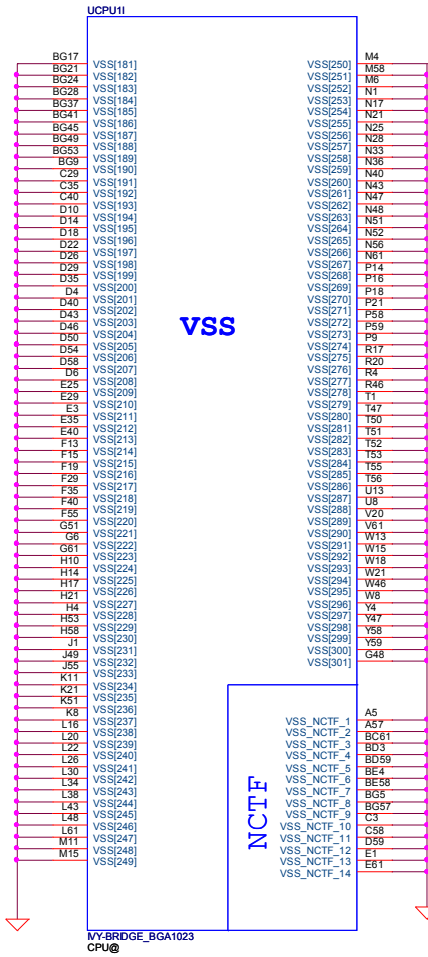
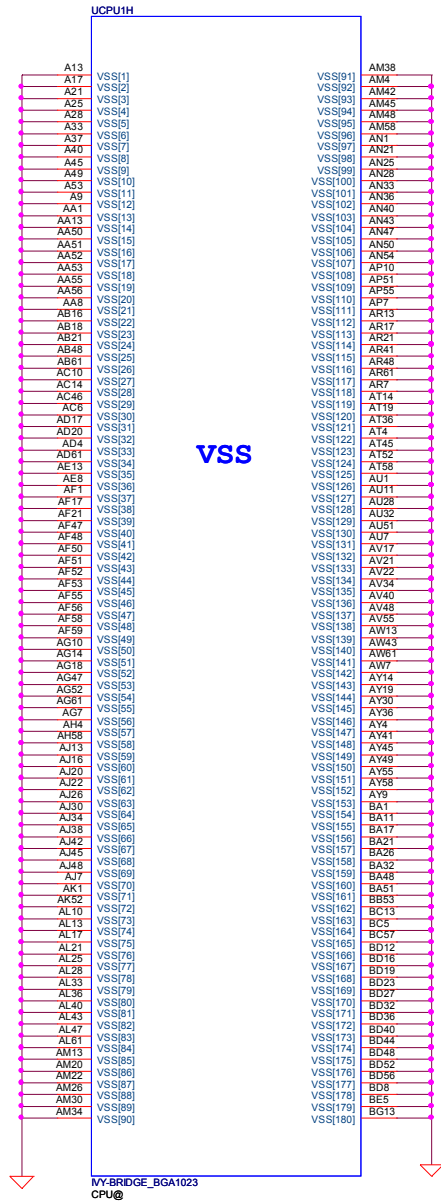
CFG7	*1: (Default) PEG Trains immediately and follows xxRESETB de-assertion
0:	PEG Wait for BIOS for training

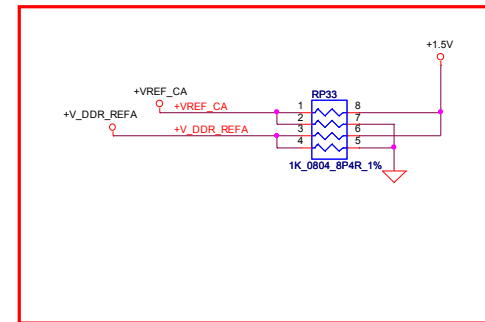
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CPU Power Rail Table			
Voltage Rail	Voltage	S0 Iccmax Current(A)	
VCC	0.65~1.2	33	Processor Core Voltage
VCCIO	1.05	8.5	Processor Uncore Voltage
VDDQ	1.5	5	Memory Controller Voltage
VCCSA	0.675~0.9	4	System Agent Voltage
VCCPLL	1.8	1.2	Processor PLL Voltage
VAXG	0.65~1.25	29	Processor Graphics Voltage

Refer to Mobile 3rd Generation Intel® Core Processor Family External Design Specification (EDS) Volume 1 of 2 Revision 2.2

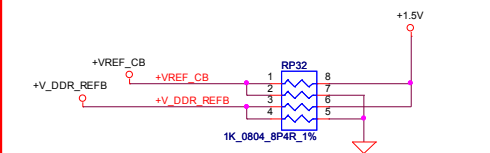




- DDR_A0_DM0
DDR_A0_DM1
DDR_A0_DM2
DDR_A0_DM3
DDR_A0_DM4
DDR_A0_DM5
DDR_A0_DM6
DDR_A0_DM7

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RP 1% P/N SD300002V00

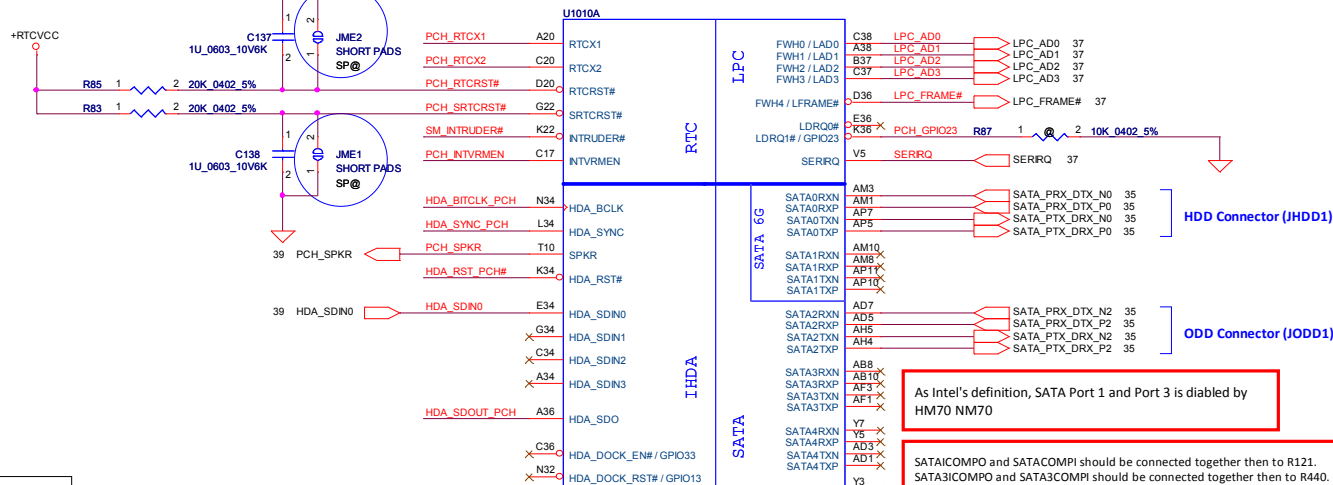
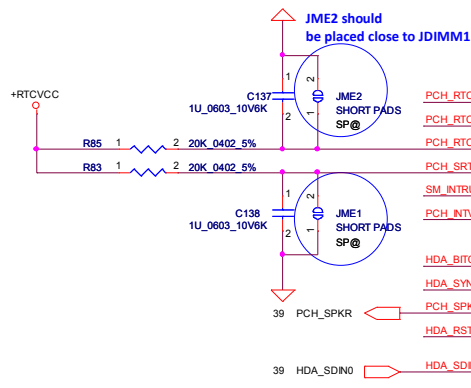
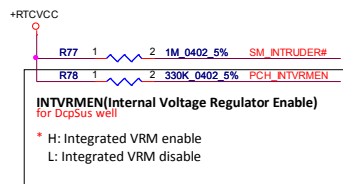


All VREF_DQ and VREFCA should be routed with width at least 20-mil and with spacing at least 20-mil.

1. +V_DDR_REFB
2. +VREF_CB



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[illegible]

37 HDA_SDOUT_PCH

Reserve for EMI

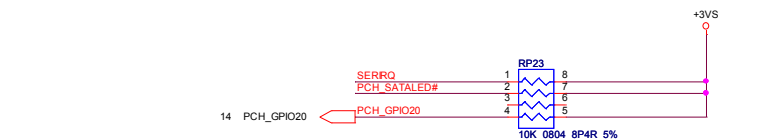
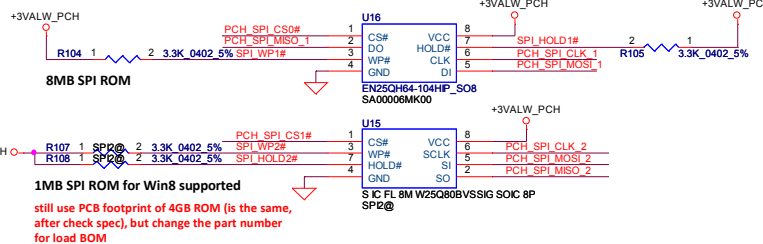
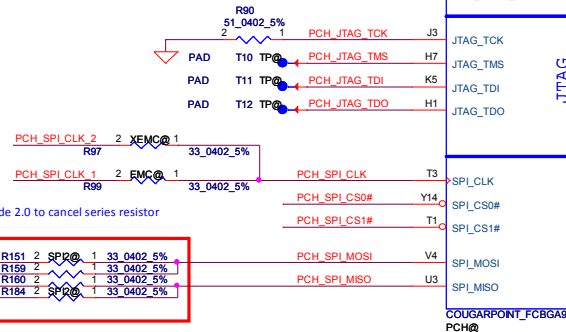
C141
10P_0402_50V8J

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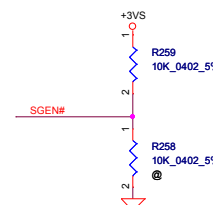
2 1

XEMC@ R109 XEMC@

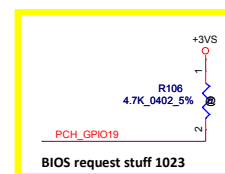
PCH_SPI_CLK 33_0402_5%



SATA1COMPO and SATA1COMPI should be connected together then to R121.
SATA31COMPO and SATA31COMPI should be connected together then to R440.
Trace Impedance= 50-ohm
Keep-out to other Signals, especially to CLK= 15-mil

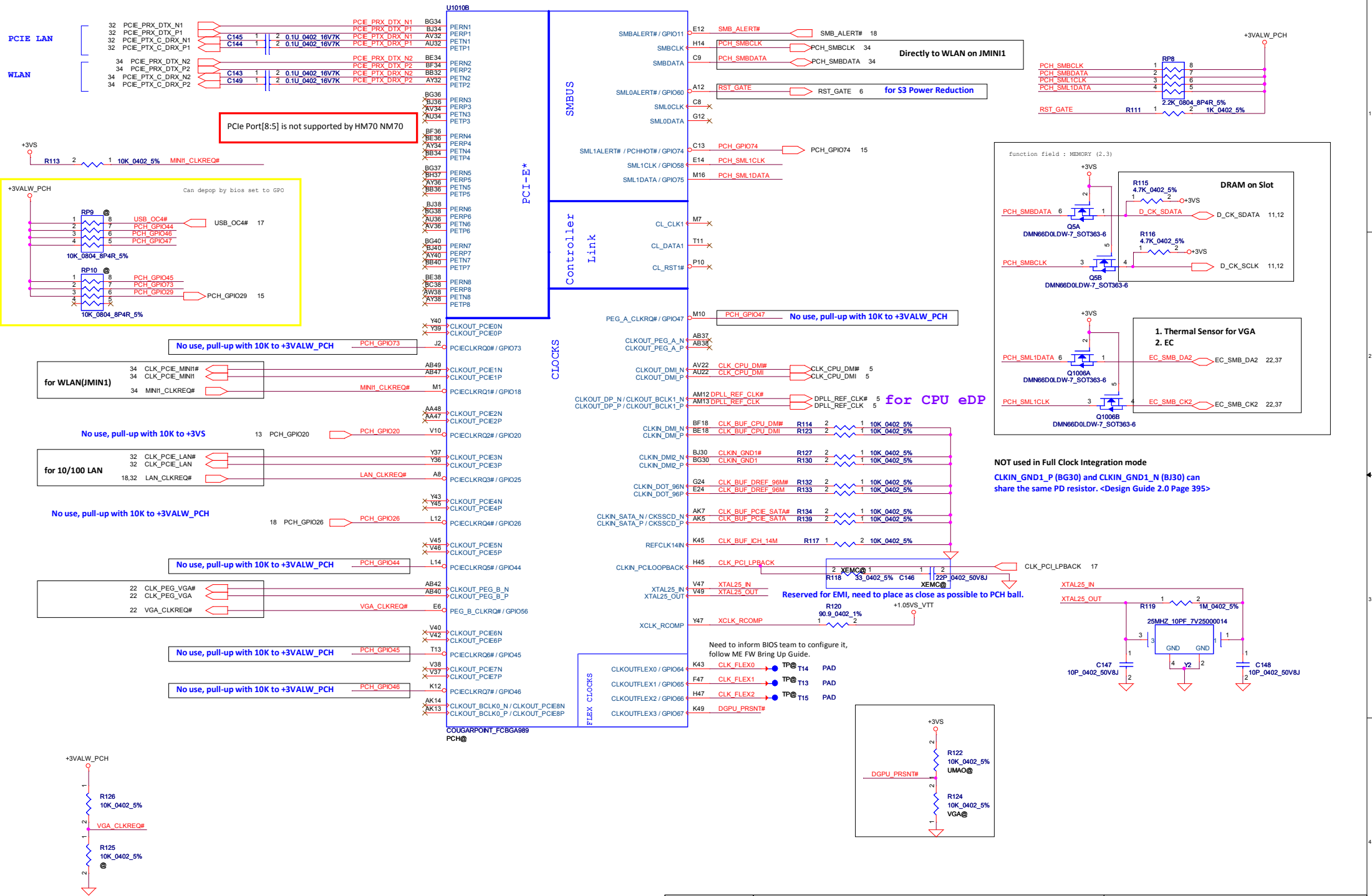


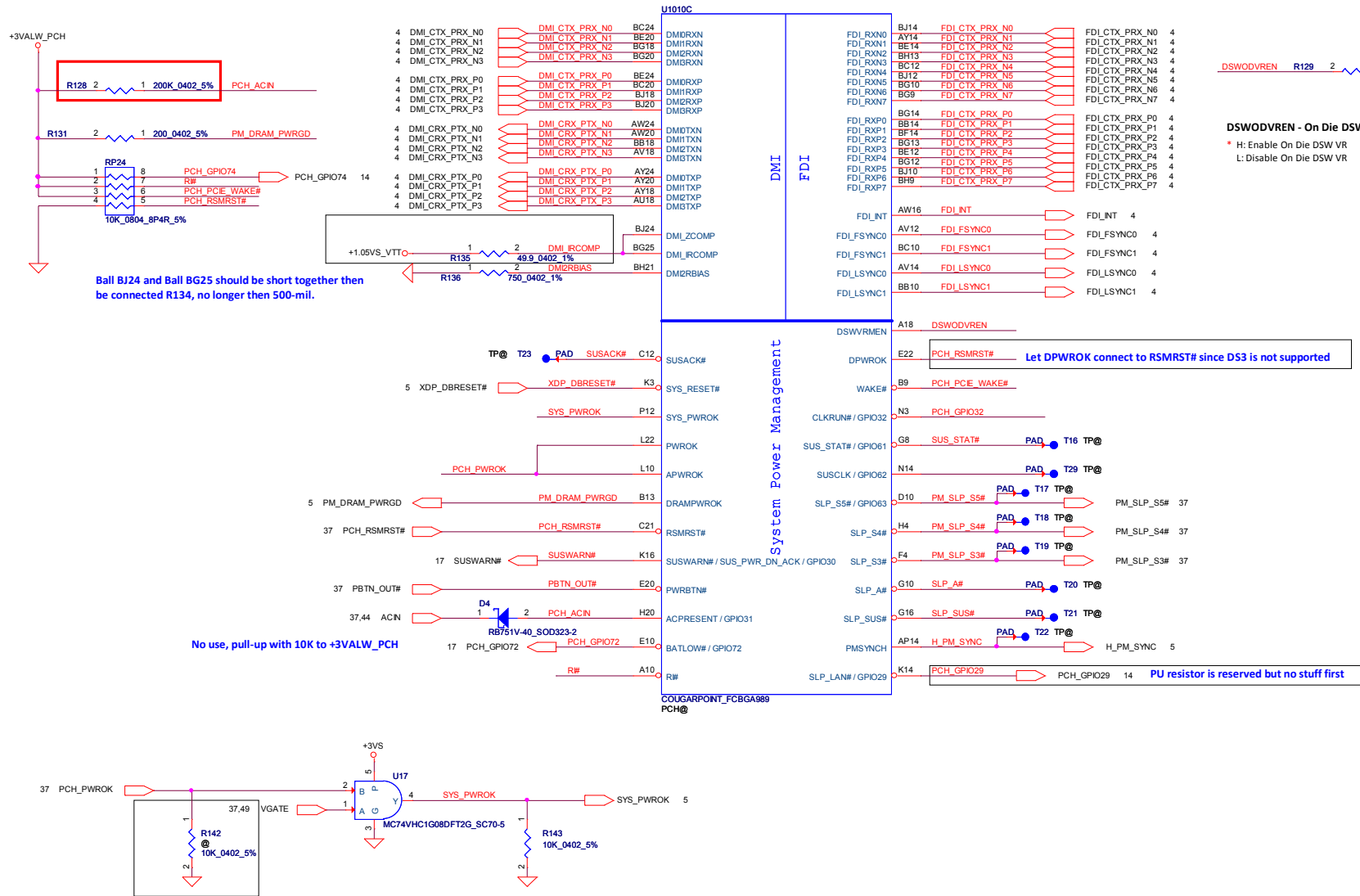
	GPIO21 SGEN#
Switchable GPU	0
*Non-Switchable	1

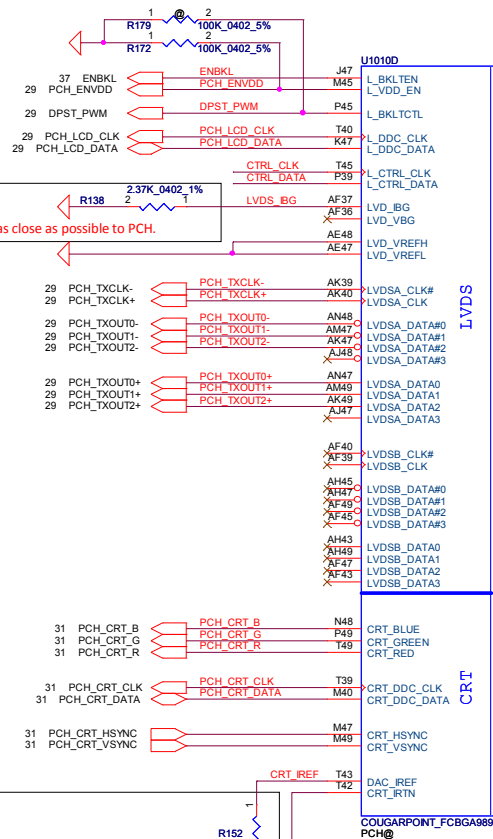
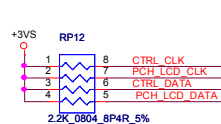


Boot BIOS Destination Selection		
Routing	GTN1#/GPIO51 (BBS1)	SATA1GP/GPIO19 (BBS0)
Reserved	0	1
Reserved	1	0
LPC	0	0
* SPI	1	1

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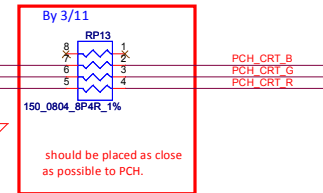


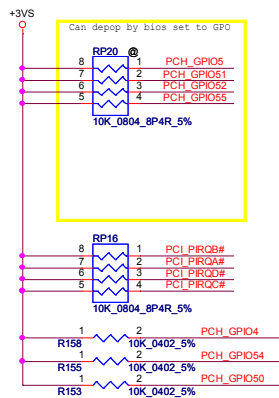


should be placed as close as possible to PCH.

should be placed as close as possible to PCH T43, and keep the trace is at least 30-mil away from other signals (especially clocks).

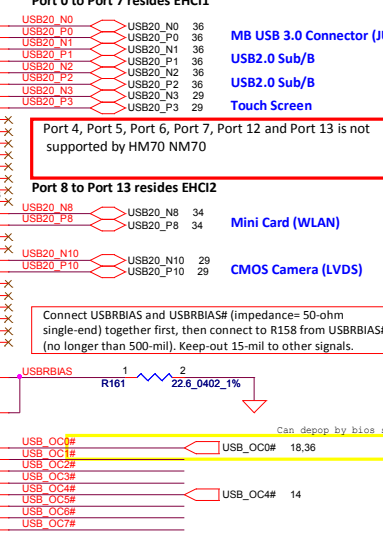
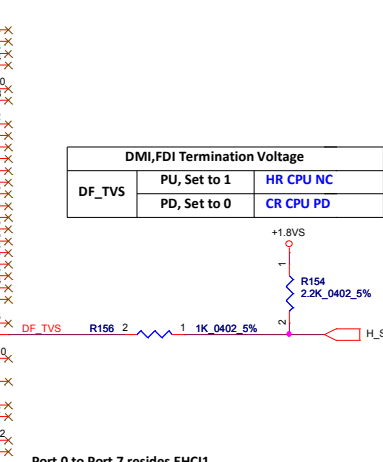
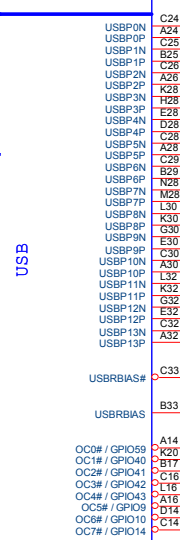
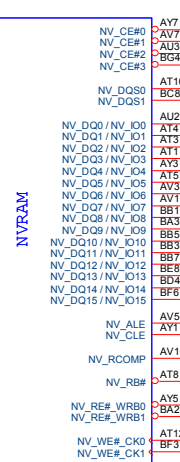
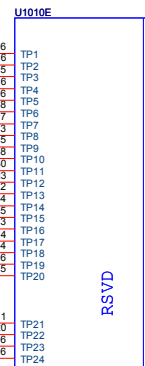
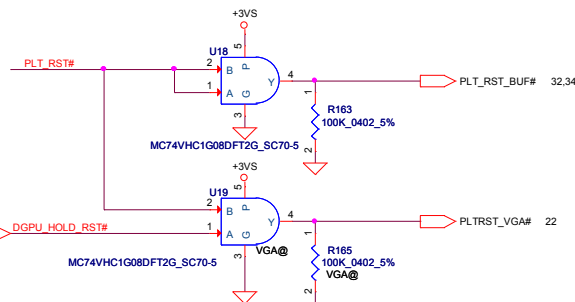
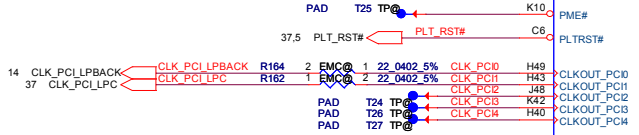
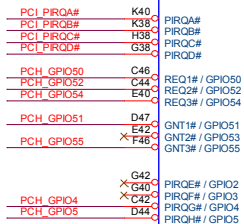
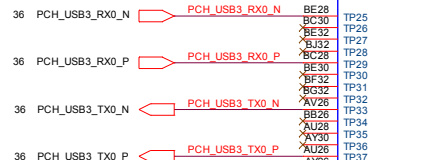
If the LVDS interface is not implemented, all signals associated with the interface can be left as No Connects. The supply pins VCC1X_LVDS and VCCA_LVD can be connected to ground.





In accordance with design guide 2.0 page 274, if default boot destination is SPI, no external pull-up/-down resistors on the board are necessary.

Boot BIOS Destination Selection		
Routing	GTN1#/GPIO15 (BB51)	SATA1GP/GPIO19 (BB50)
Reserved	0	1
Reserved	1	0
LPC	0	0
* SPI	1	1



Processor Select: This pin is an output that indicates if the processor used is Sandy Bridge or Ivy Bridge. For Sandy Bridge the output will be high, and for Ivy Bridge the output will be low.

Sandy Bridge + Ivy Bridge Compatible: Connect DF_TVS signal of the PCH to PROC_SELECT# of the processor through a 1K Ω series resistor. PROC_SELECT# also needs a 2.2K Ω pull up resistor to PCH VccDPTERM rail.

DMI,FDI Termination Voltage		
DF_TVS	PU, Set to 1	HR CPU NC
	PD, Set to 0	CR CPU PD

Port 0 to Port 7 resides EHC11

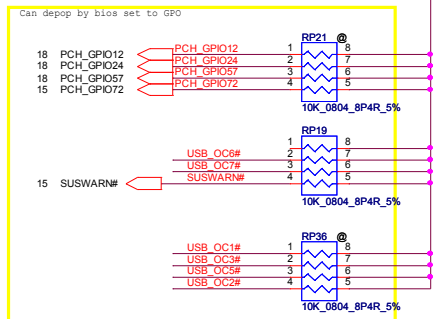
MB USB 3.0 Connector (JUSB1)
USB2.0 Sub/B
USB2.0 Sub/B
Touch Screen

Port 4, Port 5, Port 6, Port 7, Port 12 and Port 13 is not supported by HM70 NM70

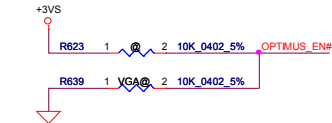
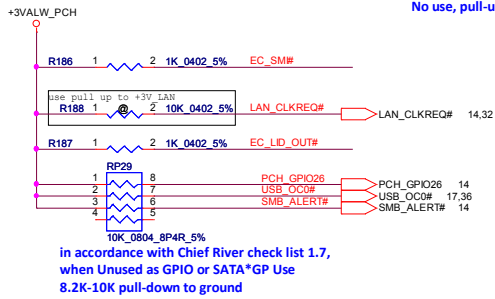
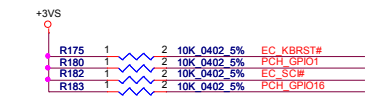
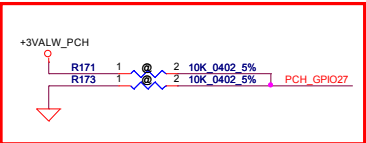
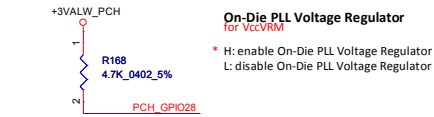
Port 8 to Port 13 resides EHC12

Mini Card (WLAN)
CMOS Camera (LVDS)

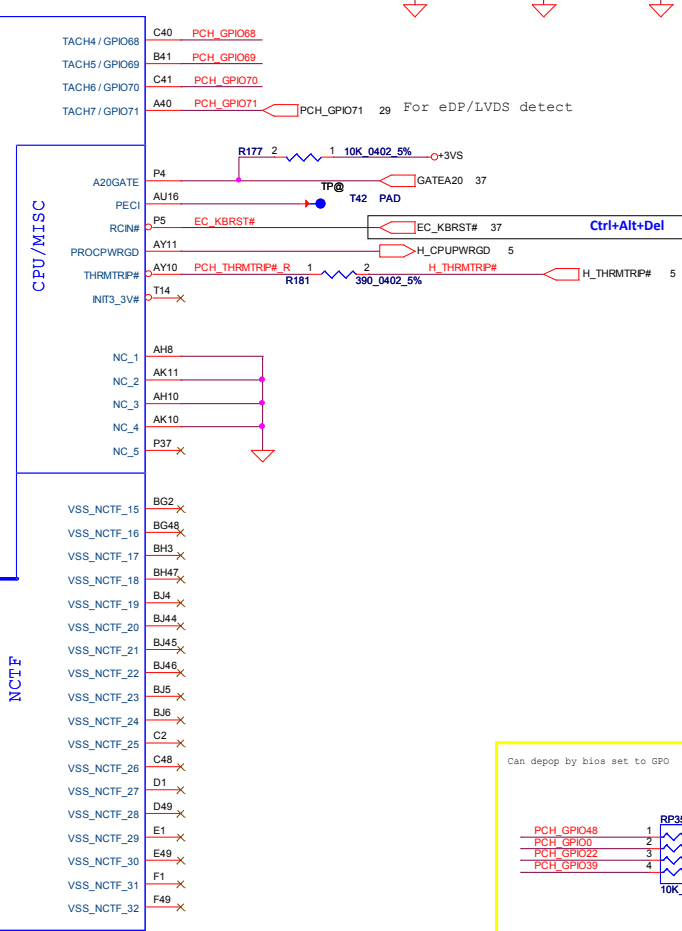
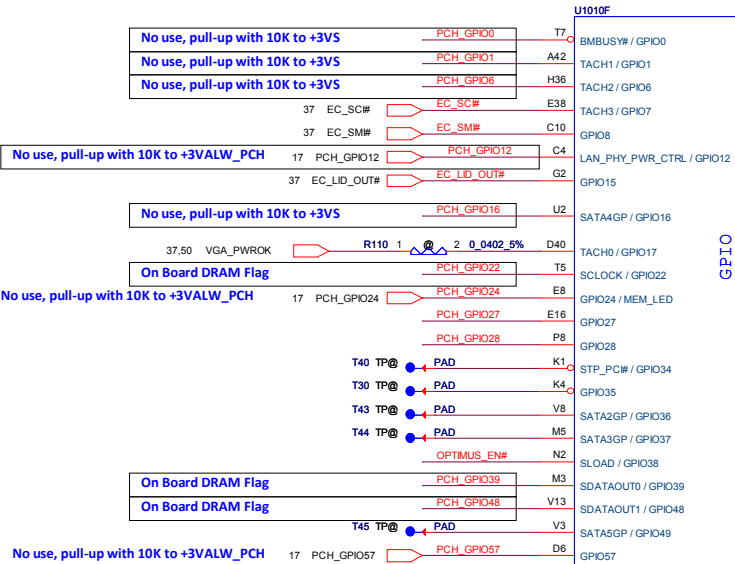
Connect USBRBIAS and USBRBIAS# (impedance= 50-ohm single-end) together first, then connect to R158 from USBRBIAS# (no longer than 500-mil). Keep-out 15-mil to other signals.



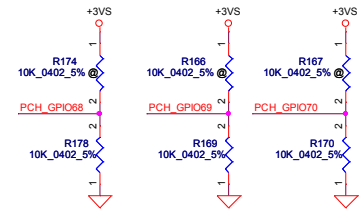
	HM77	HM70	NM70	Note
USB2.0	14	8	8	HM70/NM70 USB port 4, 5, 6,7,12 and 13 are disabled on 8 port SKUs.
USB3.0	4	2	0	USB 3.0 port 3 and 4 are disabled on HM70 USB 3.0 are all disabled on NM70
PCIe	8	4	4	HM70/NM70 PCIe port 5-8 are disabled on this SKU.
SATA	6	4	4	HM70/NM70 SATA port 1 and 3 are disabled on 4 port SKUs. HM70/NM70 SATA 6 Gb/s support on port 0 only. SATA port 0 also supports 3 Gb/s & 1.5 Gb/s HM77 SATA 6 Gb/s support on port 0 & port 1. SATA port 0 and 1 also support 3 Gb/s & 1.5 Gb/s.



	GPIO38
	OPTIMUS_EN#
* OPTIMUS	0
DIS Only	1

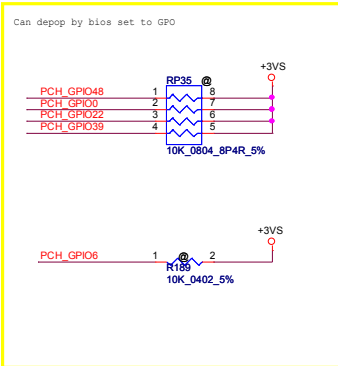
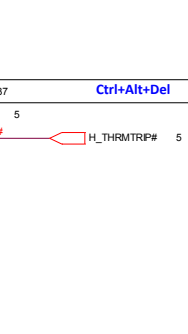


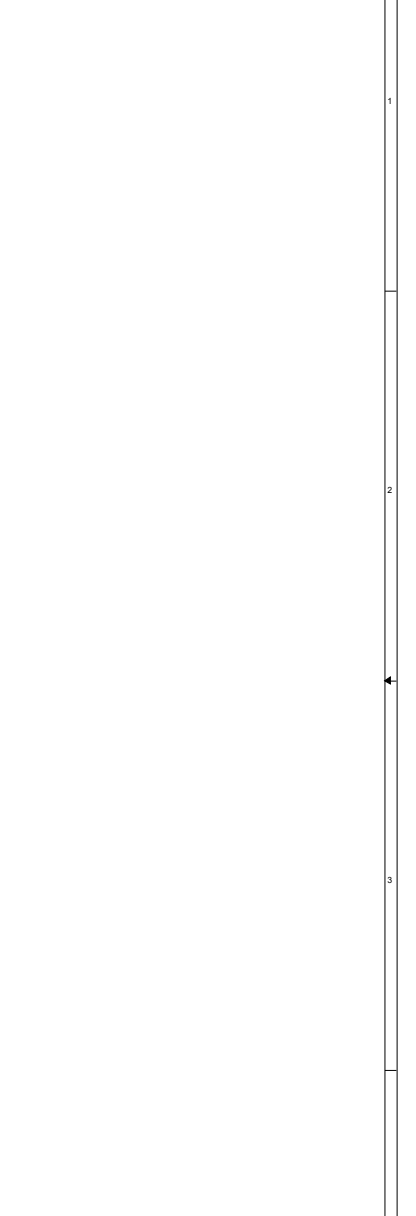
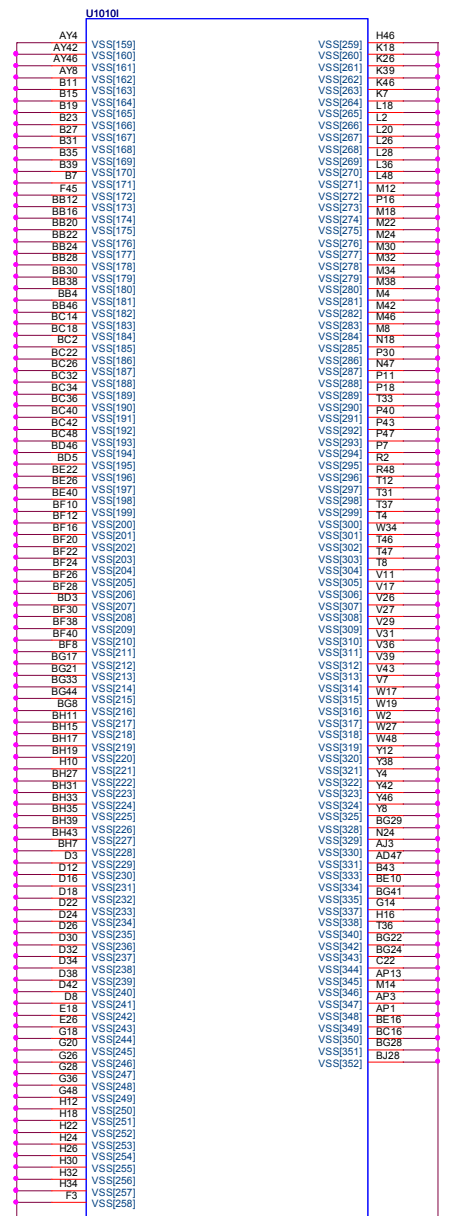
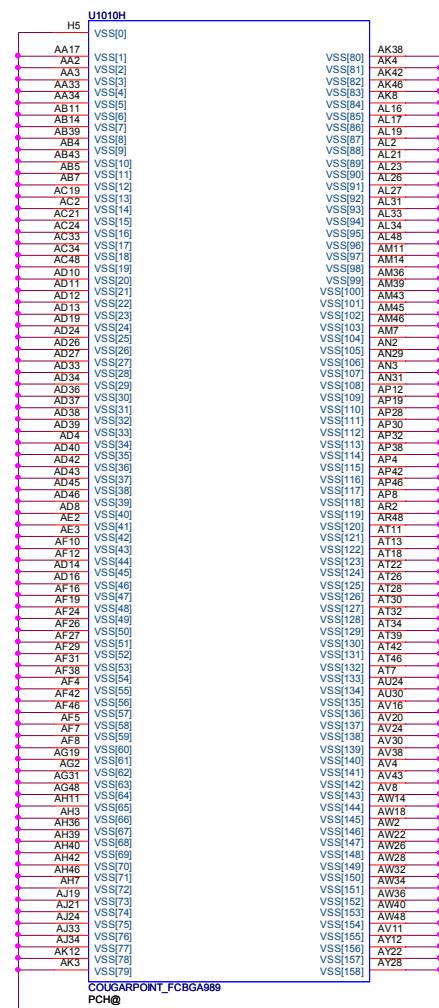
For common BIOS code



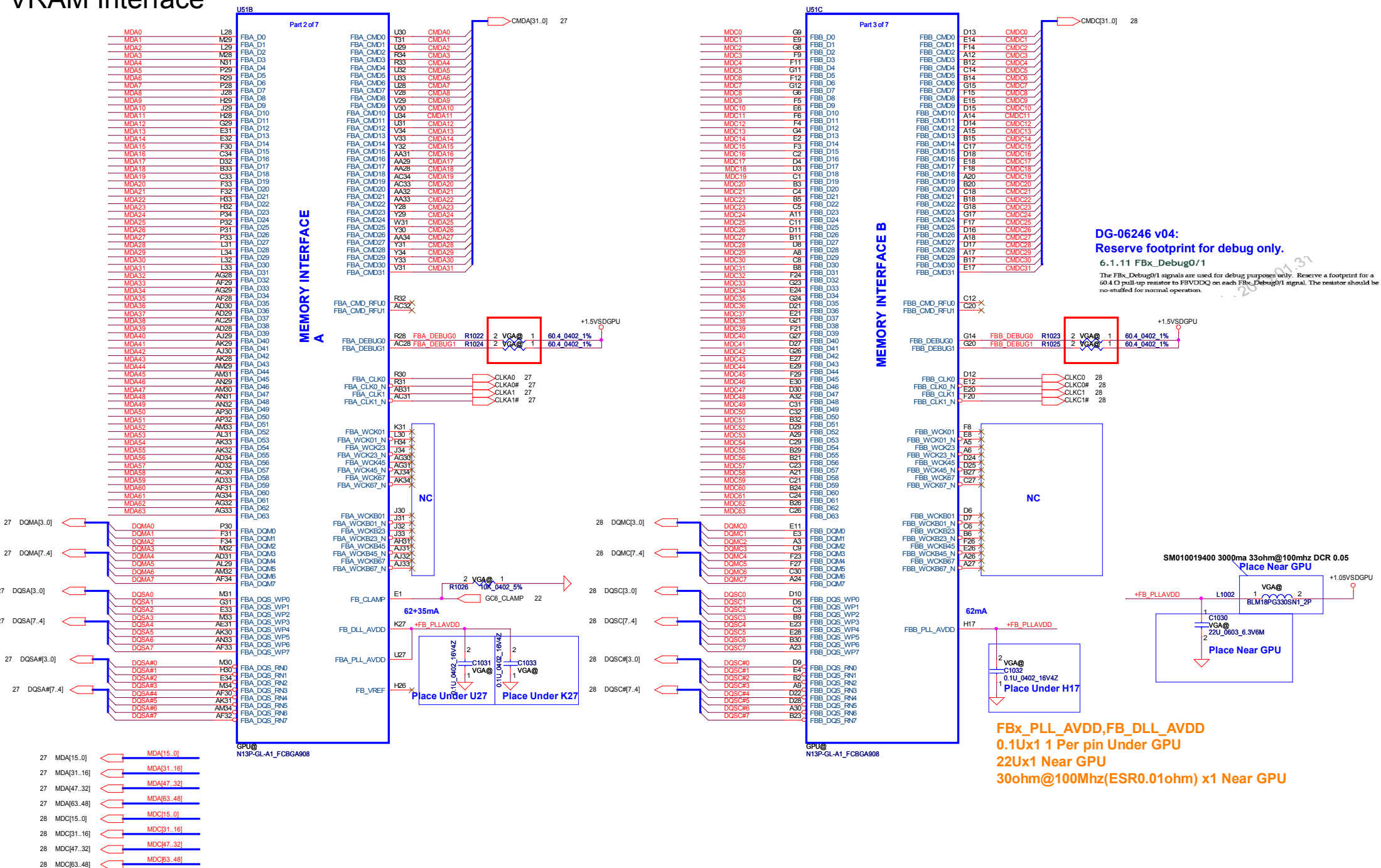
Project ID	GPIO68	GPIO69	GPIO70
Q5WE0	1	0	0
Q7YE0	1	0	1
Q5Wxx-QC	1	1	0
V5VT1	1	1	1
*Z5WE1_CR	0	0	0

For eDP/LVDS detect



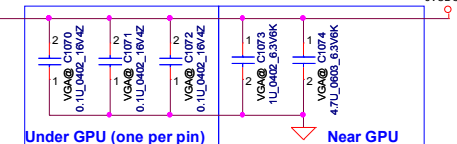
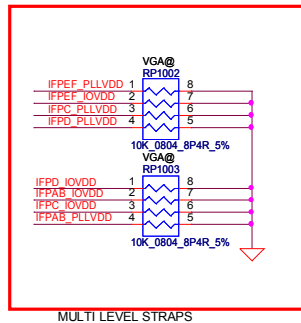
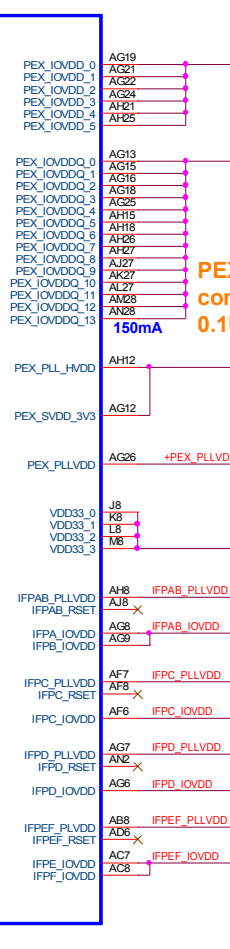


VRAM Interface



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Date: 2/12/2013				Sheet 2 of 55		

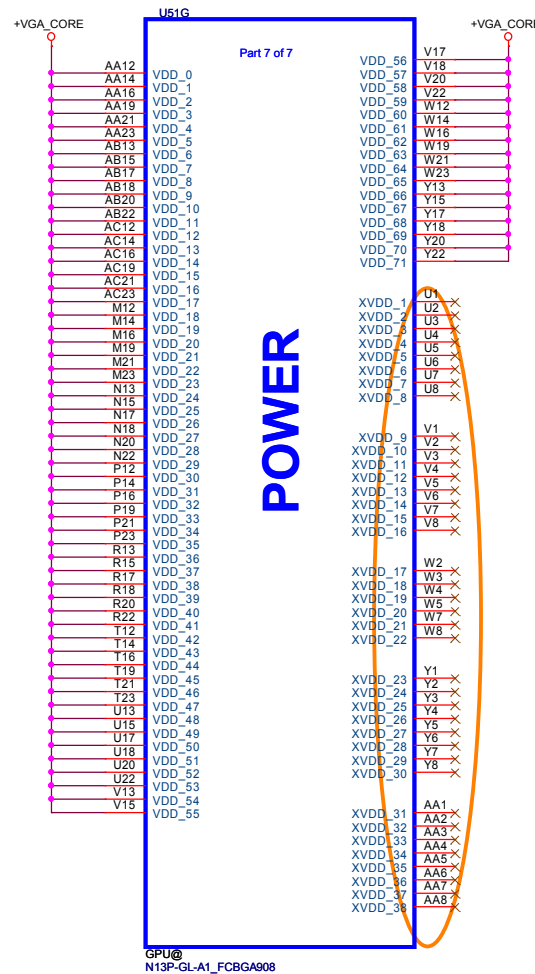
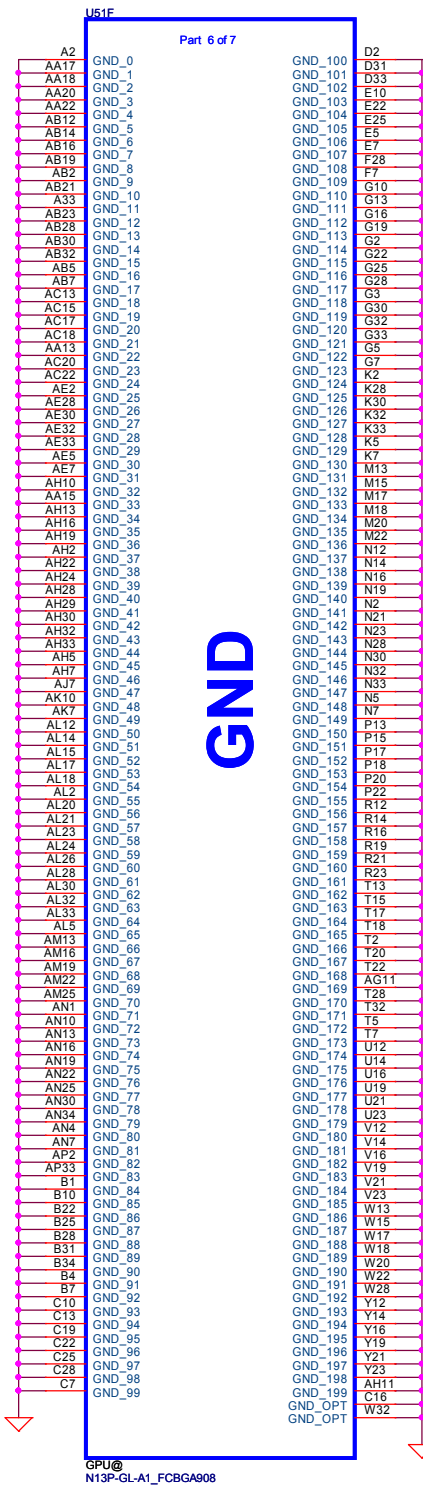
NV DG PEX_IOVVD/Q combined
1Ux4 Under GPU
4.7Ux2 Near GPU
10Ux4,22Ux4 Midway GPU & Power supply



Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed CK (MHz)	Memory Date Code Minimum	Status
256M×16 DDR3	Samsung	0xB	1.5 V / 1.5 V	K4W4G1646B-HC11	900	N/A	Production ready
	Micron	0xD	1.5 V / 1.5 V	MT41K256M16HA- 107G:E	900	N/A	Production ready
	Hynix	0x3	1.5V / 1.5V	H5TQ4G63MFR-11C	900	N/A	Production ready
		0x4		H5TC4G63AFR-11C		N/A	Post-production candidate

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed CK (MHz)	Memory Date Code Minimum	Status
256Mx16 DDR3	Samsung	0x3	1.5 V / 1.5 V	K4W4G1646B-HC11	900	N/A	Production ready
	Micron	0x1	1.5 V / 1.5 V	MT41K256M16HA-107G:E	900	N/A	Production ready
	Hynix	0x2	1.5V / 1.5V	H5TC4G63AFR-11C	900	N/A	Production ready

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				Date:	Friday, June 07, 2013	(Sheet 25 of 55)

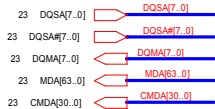


N14M-GE 35A
N14P-GV2 45A
N14P-GT 55A

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								N14P POWER & GND 5/7	
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								LA-9535P M/B Schematics	
								Date: Friday, June 07, 2013	
								Sheet 26 of 55	

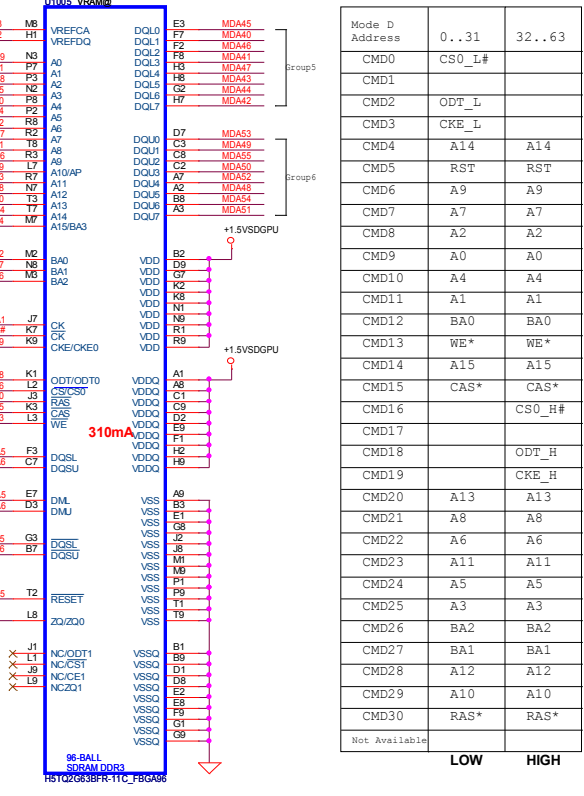
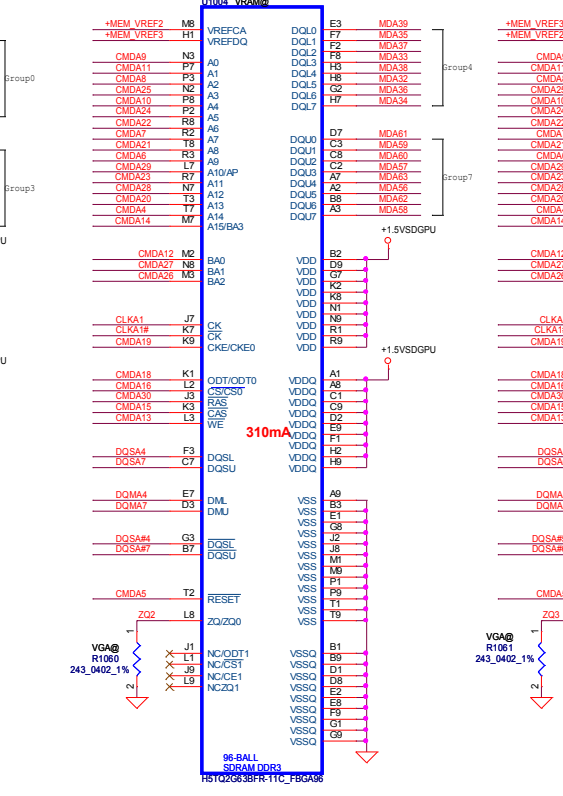
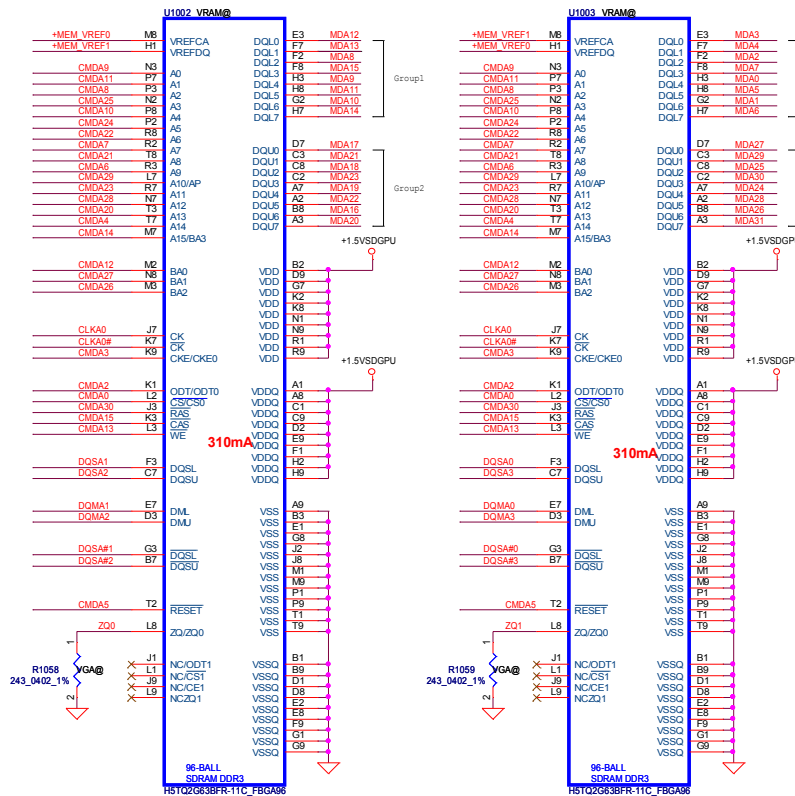
VRAM DDR3 chips

128Mx16 DDR3 *8==>2GB
256Mx16 DDR3 *8==>4GB

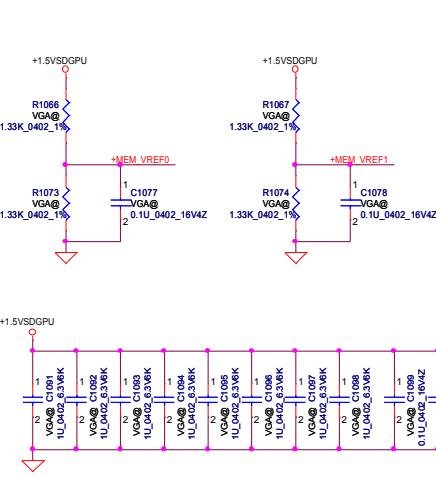


Low 32

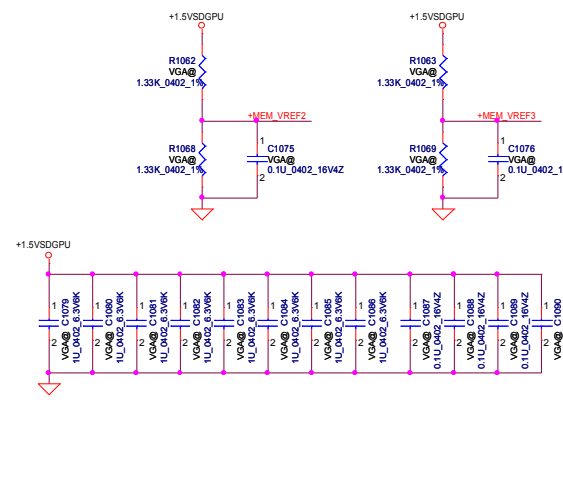
High 32



Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1	ODT_L	
CMD2	CKE_L	
CMD3	A14	A14
CMD4	RST	RST
CMD5	A9	A9
CMD6	A7	A7
CMD7	A2	A2
CMD8	A0	A0
CMD9	A4	A4
CMD10	A1	A1
CMD11	BA0	BA0
CMD12	WE*	WE*
CMD13	CAS*	CAS*
CMD14	CS0_H#	
CMD15	ODT_H	
CMD16	CHE_H	
CMD17	A13	A13
CMD18	A8	A8
CMD19	A6	A6
CMD20	A11	A11
CMD21	A5	A5
CMD22	A3	A3
CMD23	BA2	BA2
CMD24	BA1	BA1
CMD25	A12	A12
CMD26	A10	A10
CMD27	RAS*	RAS*
CMD28		
CMD29		
CMD30		

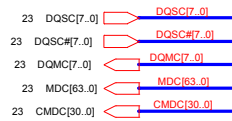


Command Bit	Default Pull-down
ODT#	10k
CKE#	10k
RST	10k
CS*	No Termination



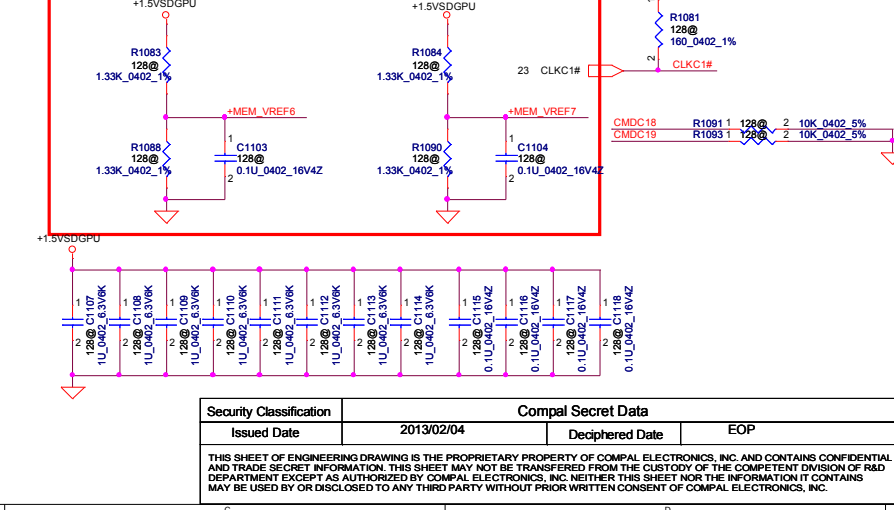
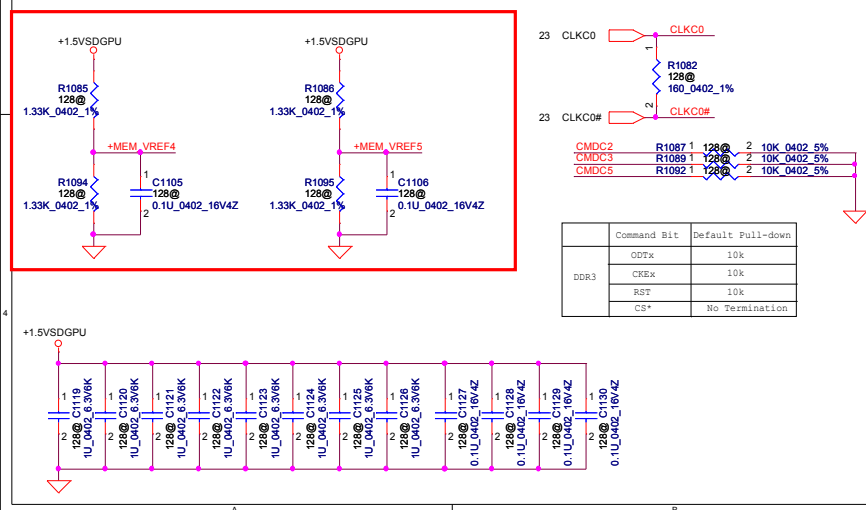
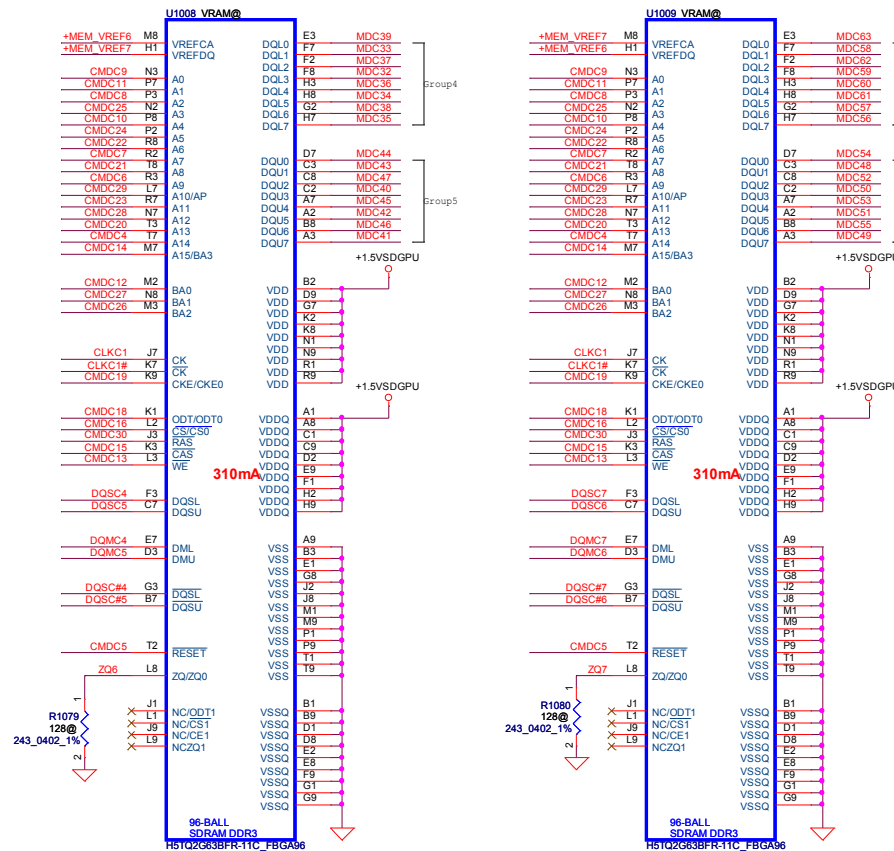
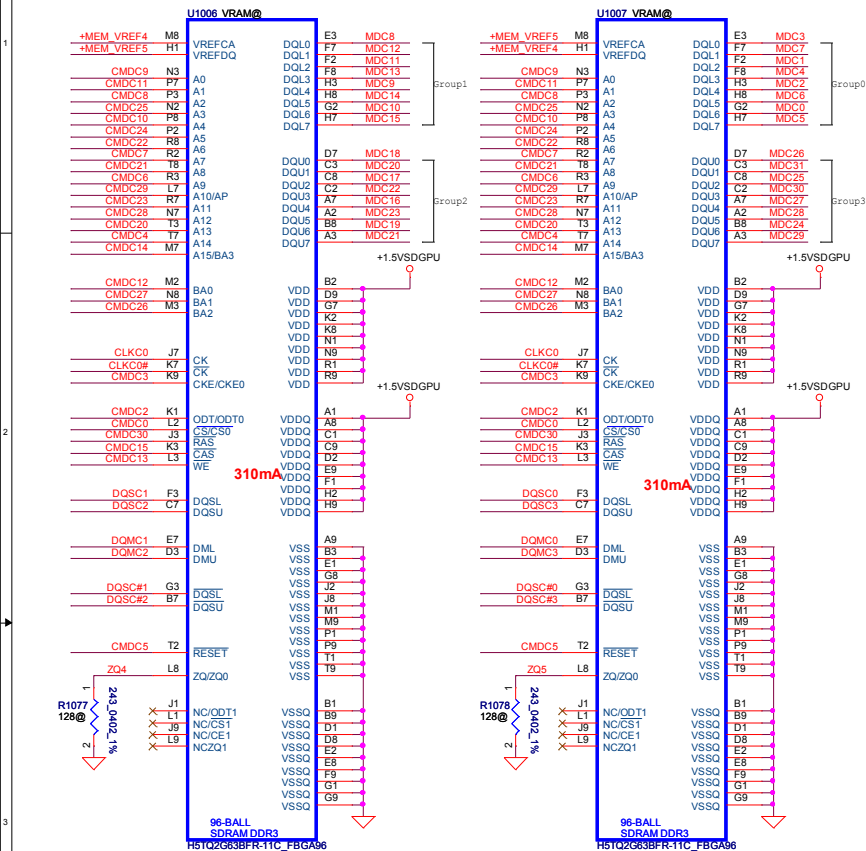
VRAM DDR3 chips

128Mx16 DDR3 *8==>2GB
256Mx16 DDR3 *8==>4GB



Low 32

High 32

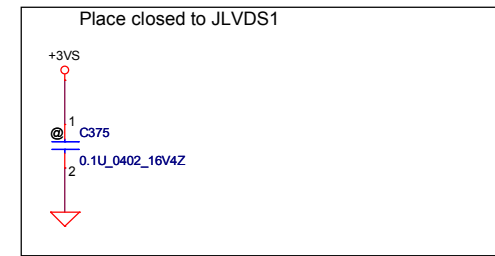
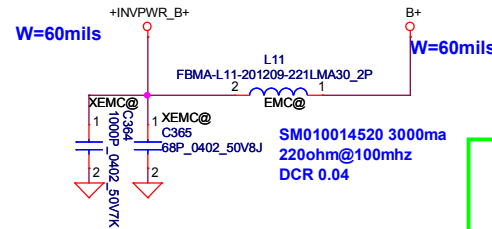
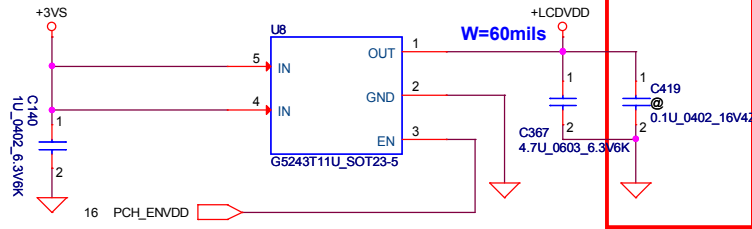


Mode D	Address	0..31	32..63
CMD0	CS0_L#		
CMD1			
CMD2	ODT_L		
CMD3	CKE		
CMD4	A14	A14	
CMD5	RST	RST	
CMD6	A9	A9	
CMD7	A7	A7	
CMD8	A2	A2	
CMD9	A0	A0	
CMD10	A4	A4	
CMD11	A1	A1	
CMD12	BA0	BA0	
CMD13	WE*	WE*	
CMD14	A15	A15	
CMD15	CAS*	CAS*	
CMD16		CS0_H#	
CMD17			
CMD18	ODT_H		
CMD19	CKE_H		
CMD20	A13	A13	
CMD21	A8	A8	
CMD22	A6	A6	
CMD23	A11	A11	
CMD24	A5	A5	
CMD25	A3	A3	
CMD26	BA2	BA2	
CMD27	BA1	BA1	
CMD28	A12	A12	
CMD29	A10	A10	
CMD30	RAS*	RAS*	
Not Available			

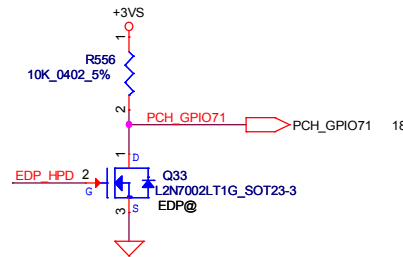
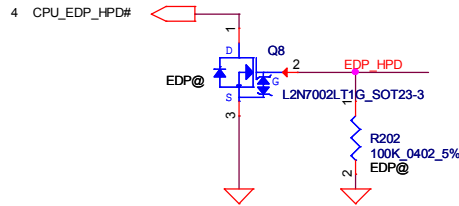
LOW HIGH



LCD POWER CIRCUIT

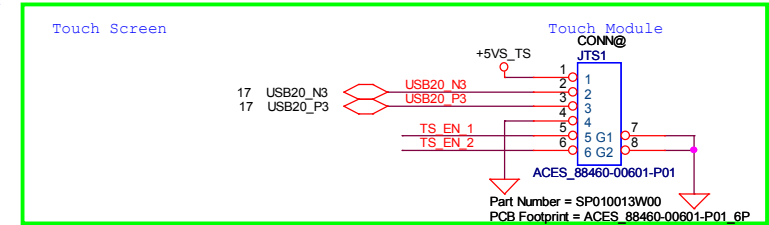
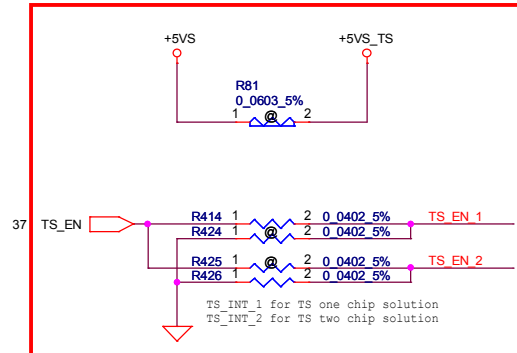
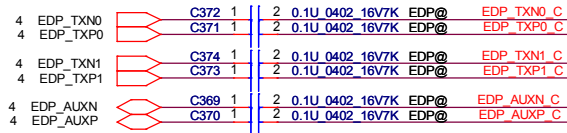


HPD

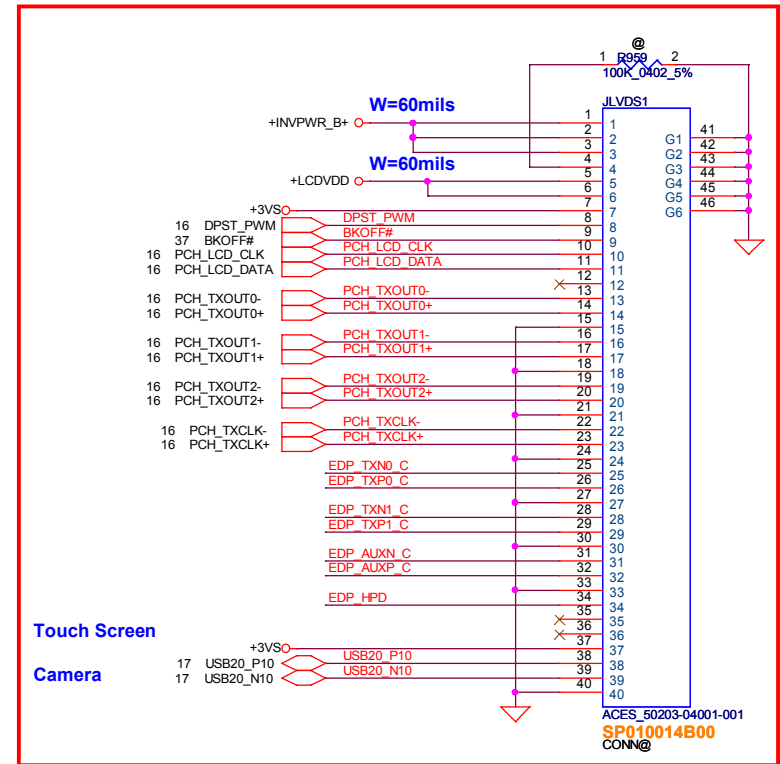


	GPIO71
	PCH_GPIO71
eDP	0
LVDS	1

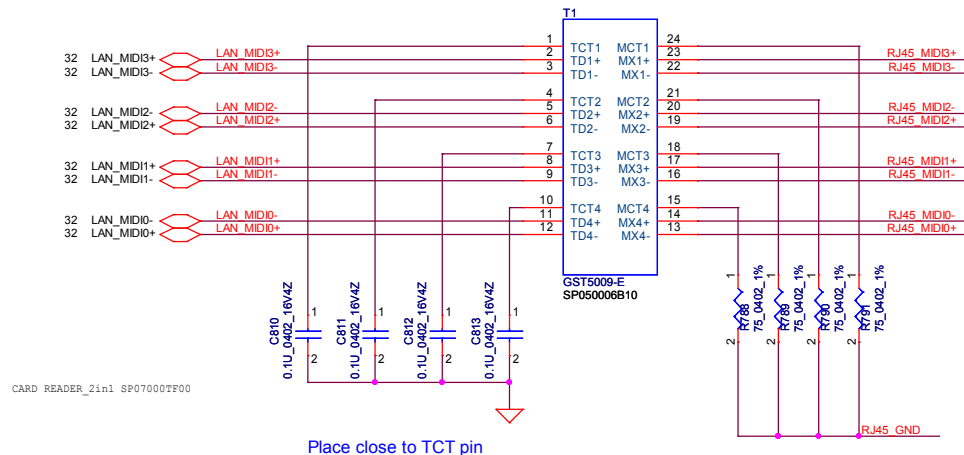
eDP



LCD/LED PANEL Conn.

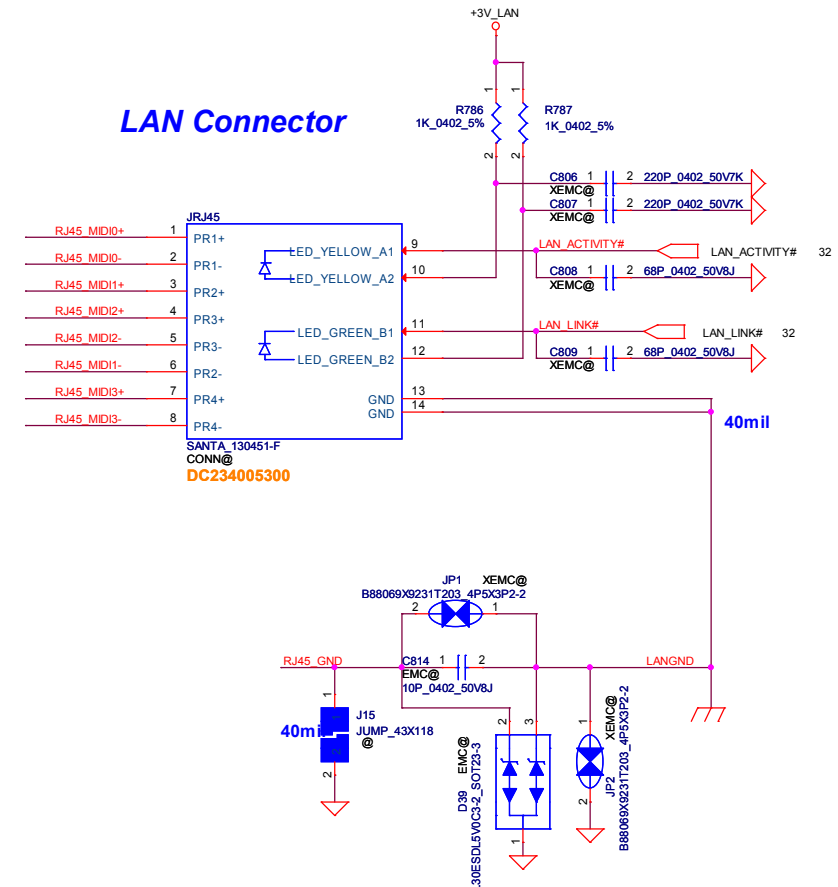
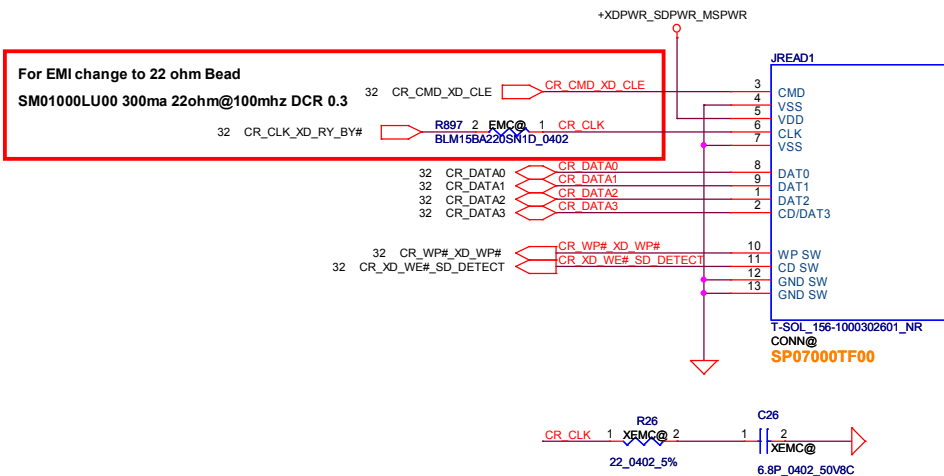


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BOTH HAND: S X'FORM_ GST5009-E LF LAN, SP050006B10
 TIMAG: S X'FORM_ IH-160 LAN, SP050006F00
 FCE: S X'FORM_ NS892407 1G, SP050006800

Card Reader Connector



60mil

J3

470pF_0402_50V7K

4.7uF_0603_6.3V6K

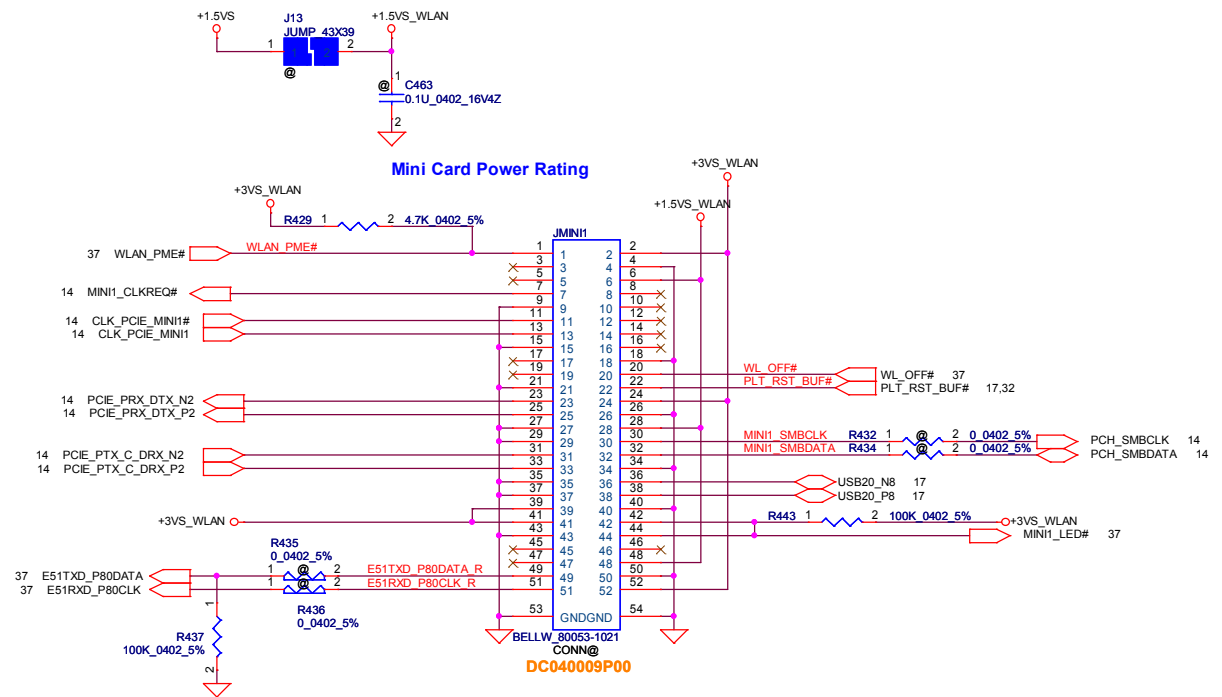
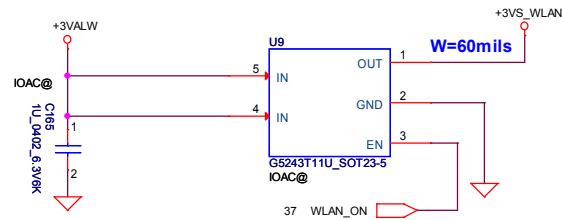
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3V5S

3V5S_WLAN

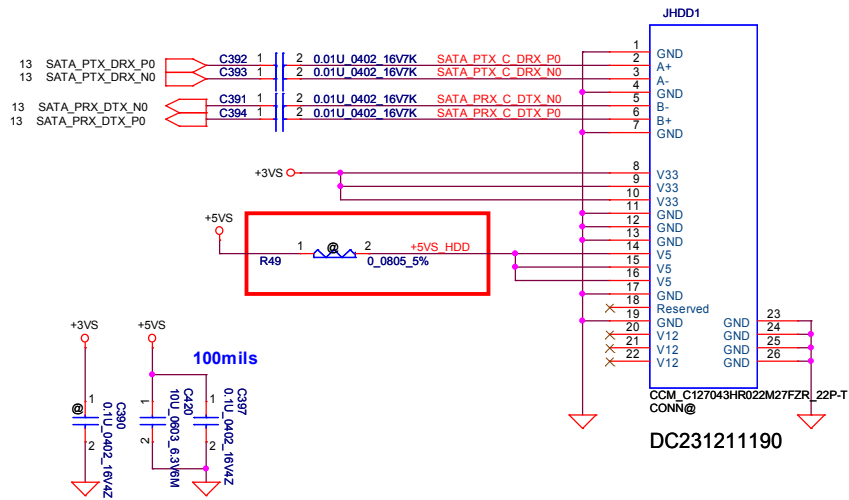
EMC#

Add 3/12

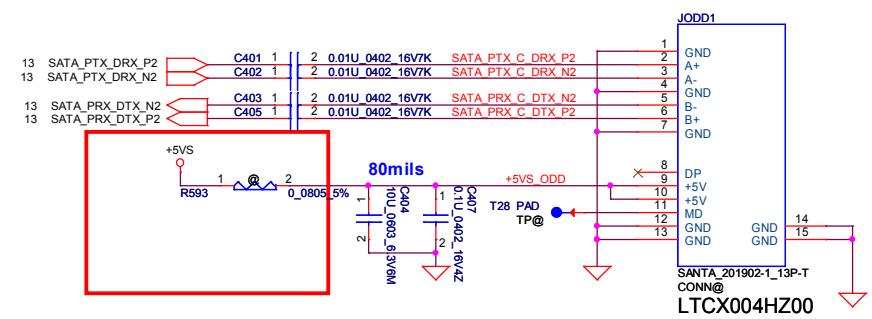


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				Custom	LA-9535P M/B Schematics	1.0
				Date:	Friday, June 07, 2013	Sheet 34 of 55

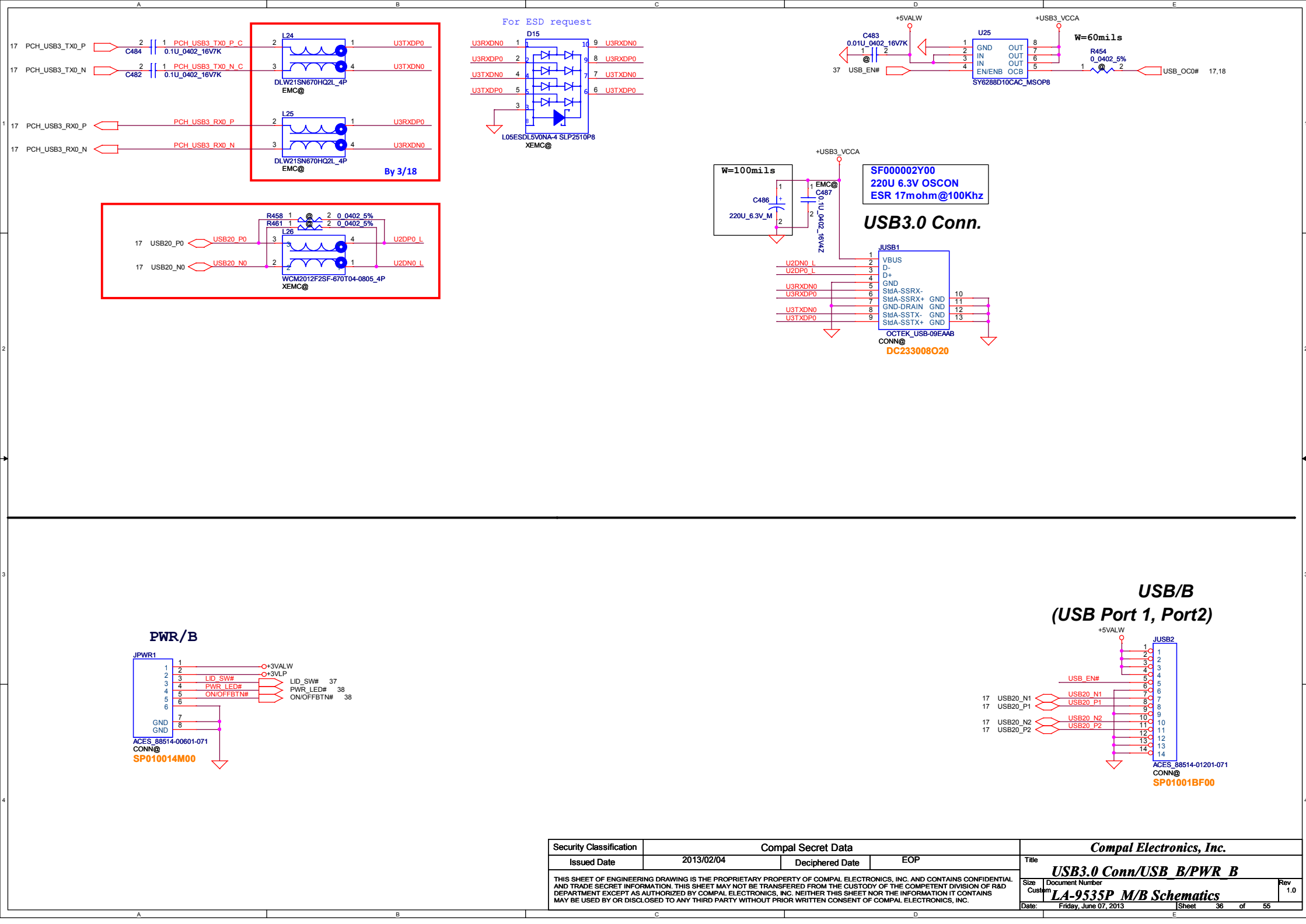
SATA HDD Conn.

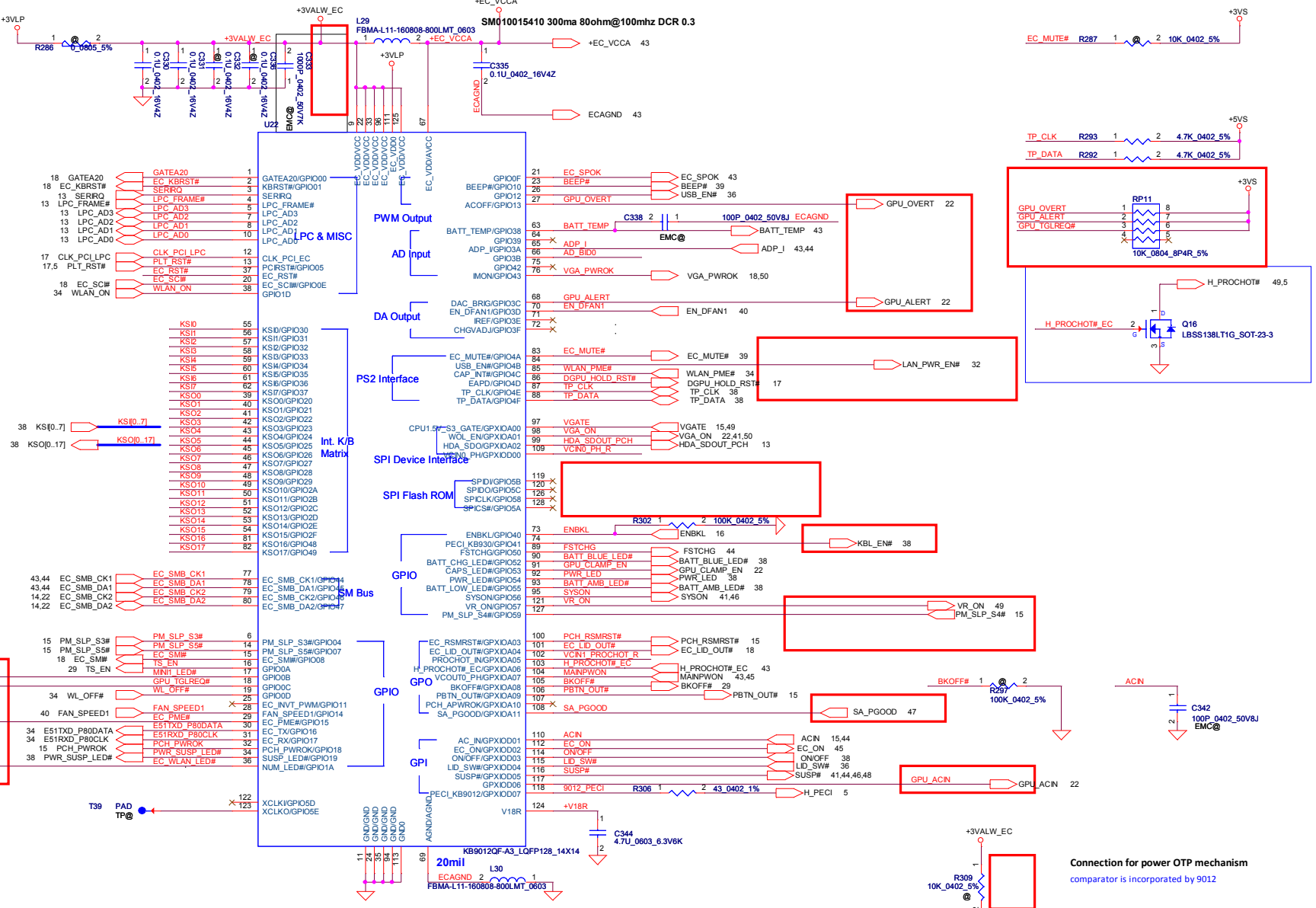
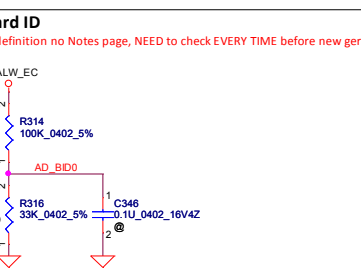
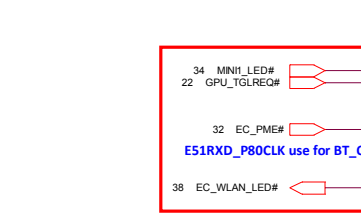
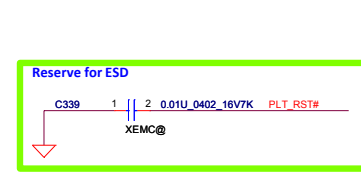
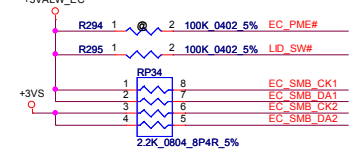
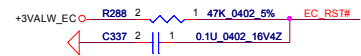
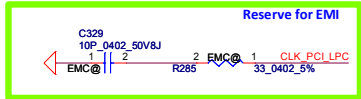


SATA ODD Conn.

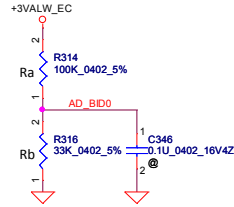


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				Size	Document Number
				Custom	LA-9535P M/B Schematics
Date:	Friday, June 07, 2013	Sheet	35	of	55



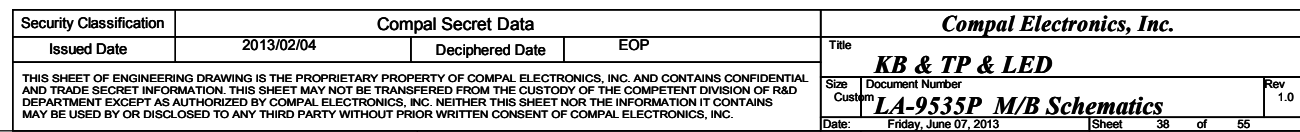


Board ID
See definition no Notes page, NEED to check EVERY TIME before new gerber-out

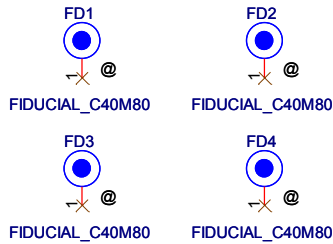
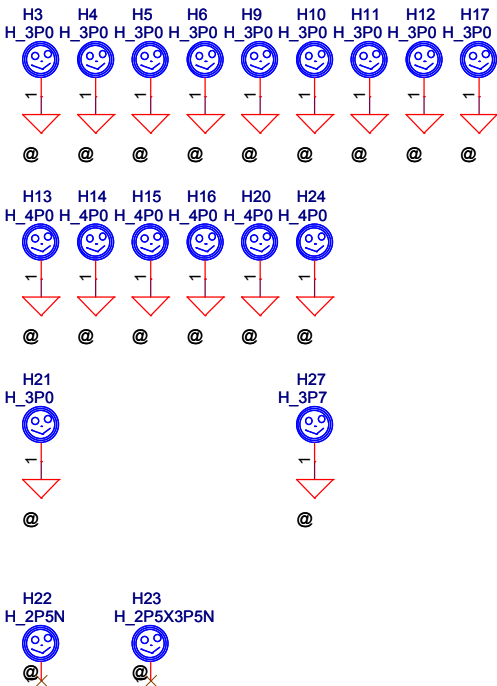
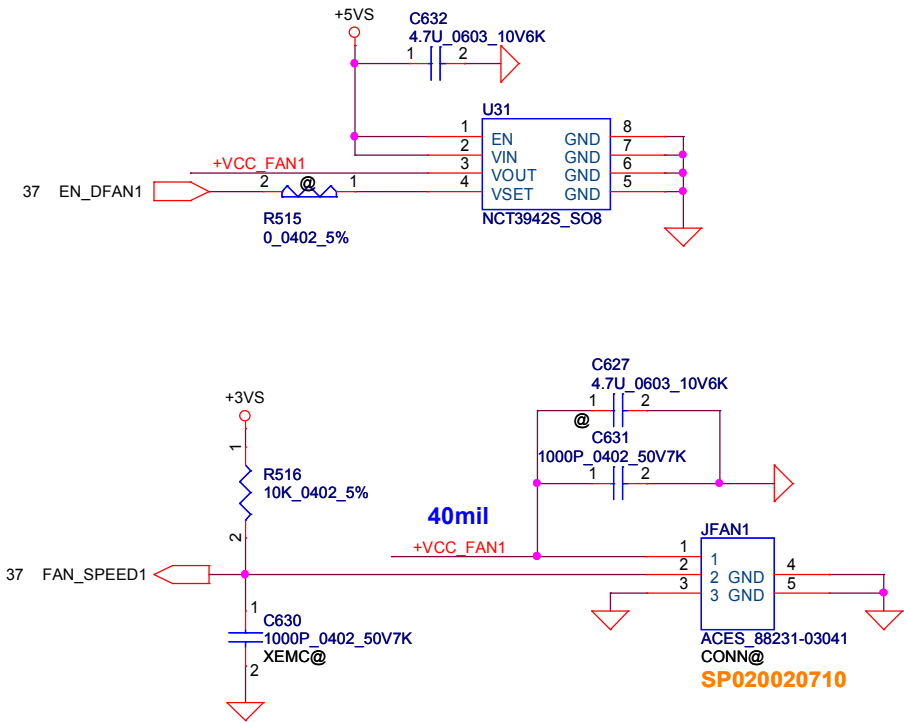


Phase	Revision	BID0	BID1
EVT	0.1	0	X
PVT	0.2	1	X
PVT2	0.3	2	X
MP	1.0	3	X

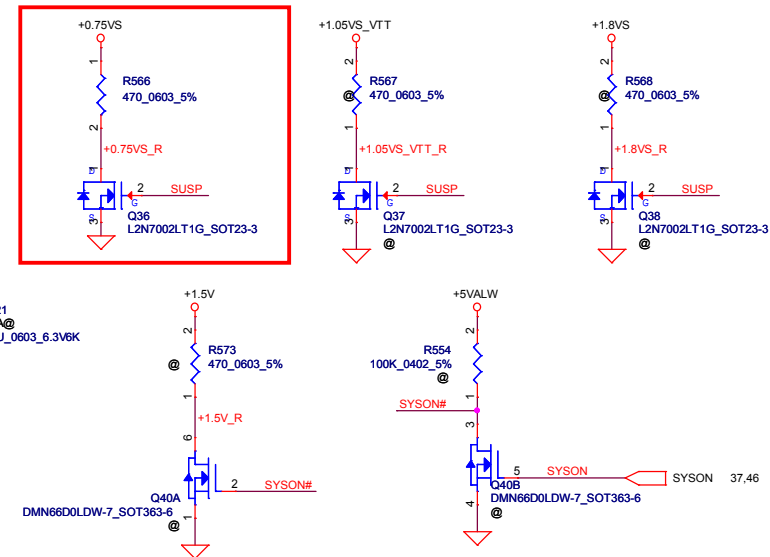
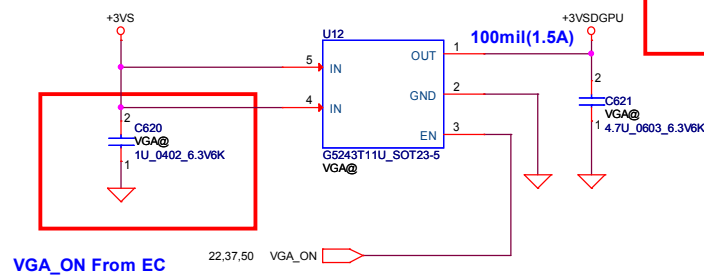
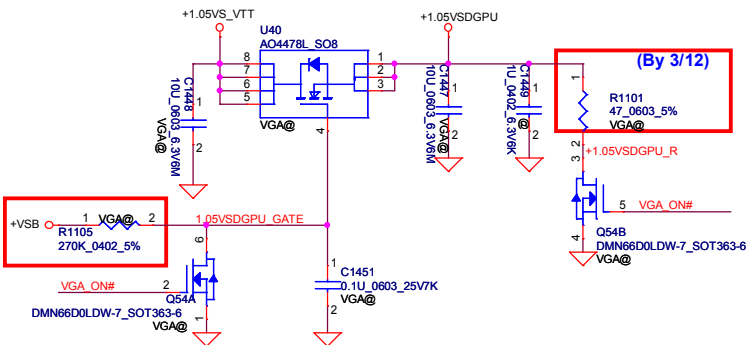
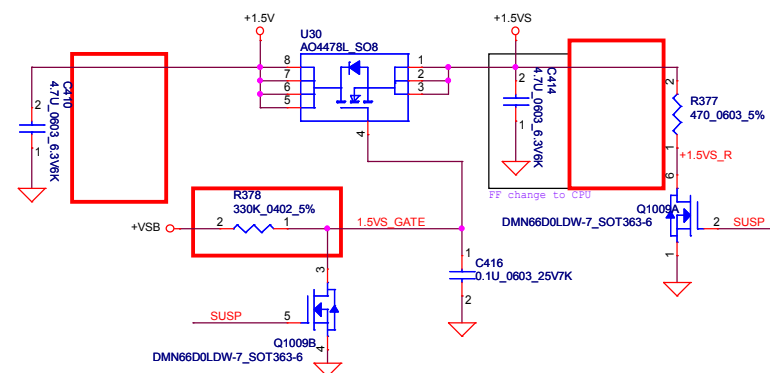
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Issued Date				Deciphered Date				Title			
2013/02/04				EOP				EC ENE-KB9012			
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				Custom				LA-9535P M/B Schematics			
				Date				Friday, June 07, 2013			
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FAN1 Conn

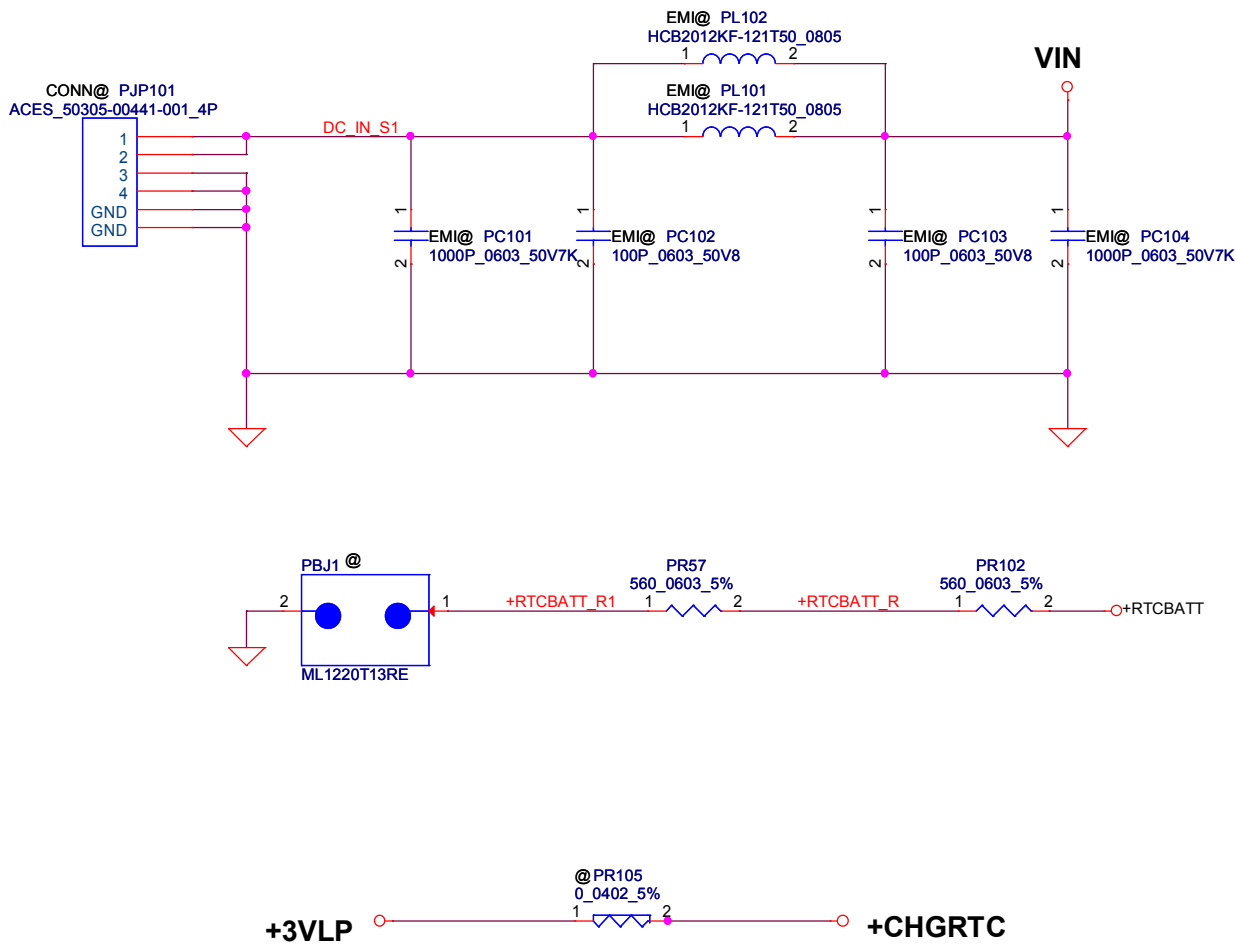


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								Size	Document Number	Rev
								Custom	LA-9535P M/B Schematics	1.0
								Date:	Friday, June 07, 2013	Sheet

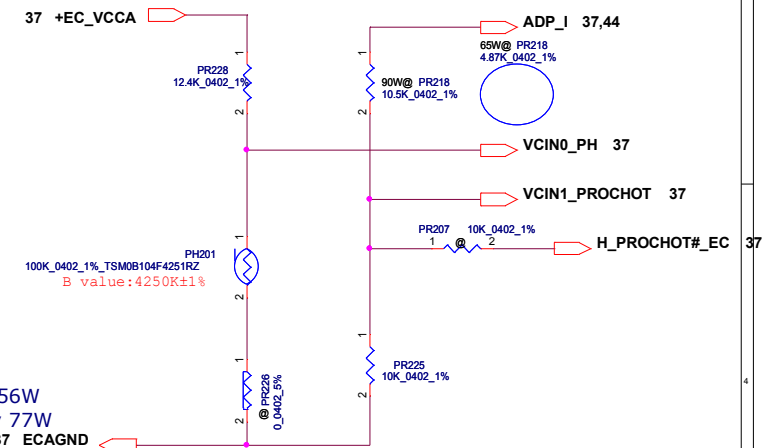
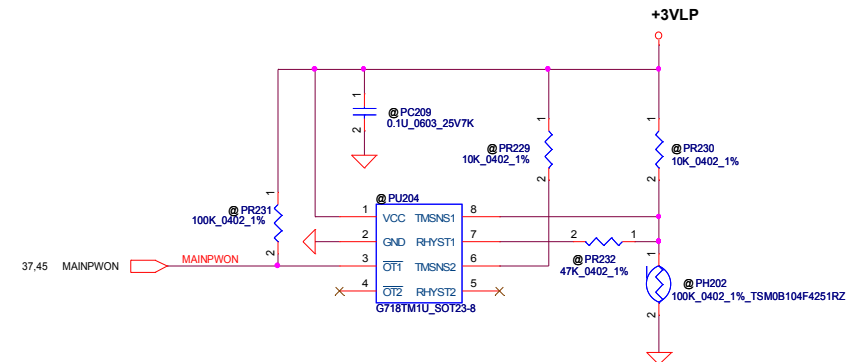


The schematic diagram shows the VGA input circuit for the Q34. The circuit includes a 100K_0402_5% resistor (R560) connected to +5VALW and a 100K_0402_5% resistor (R561) connected to GND. The VGA_ON signal is connected to the input of the Q34 VGA input pin. The Q34 is a 12N7002LT1G_SOT23-3 device.

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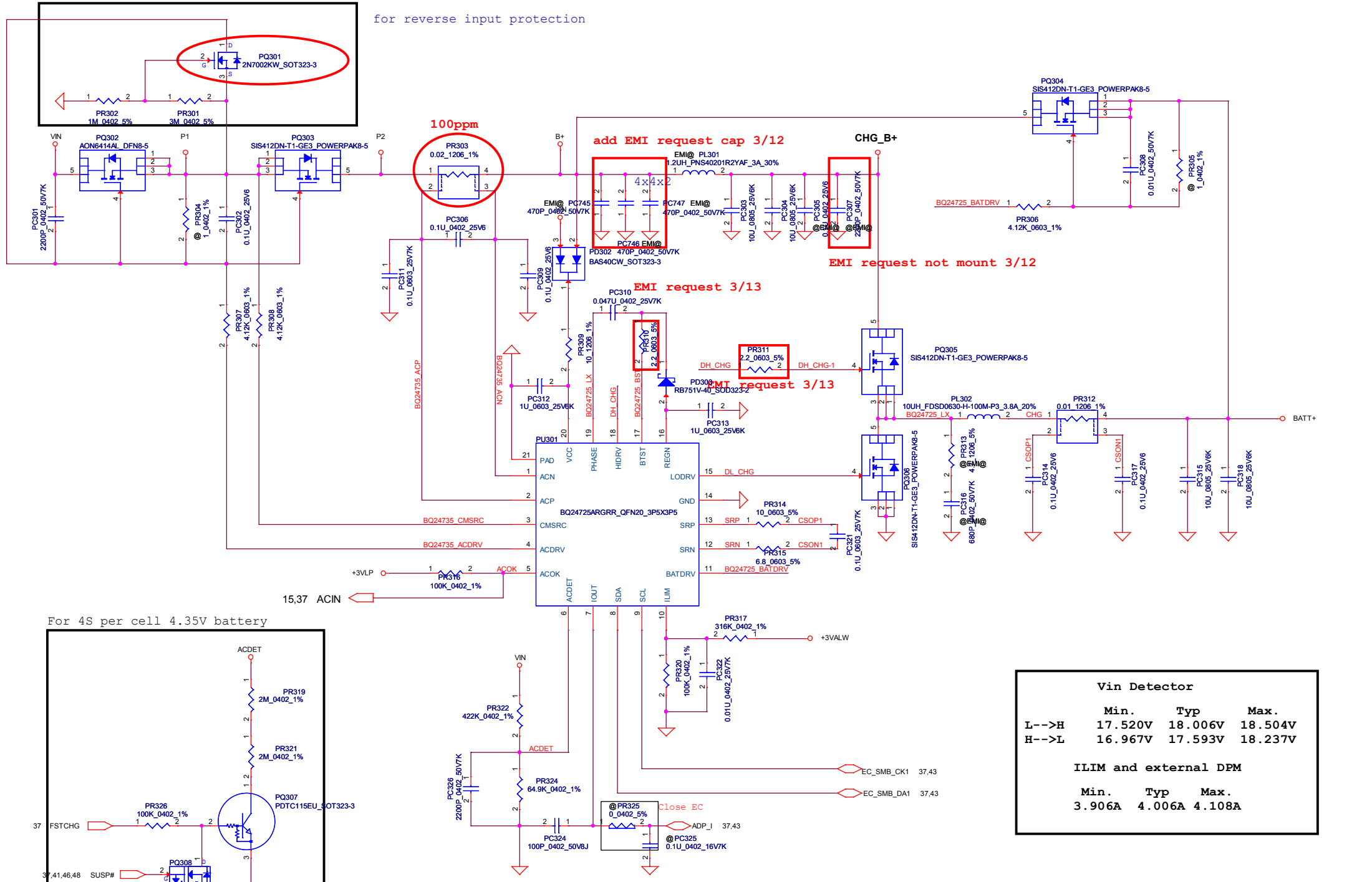


For KB9012 OTP	
92°C	1.2V, Active
56°C	2.255V, Recovery

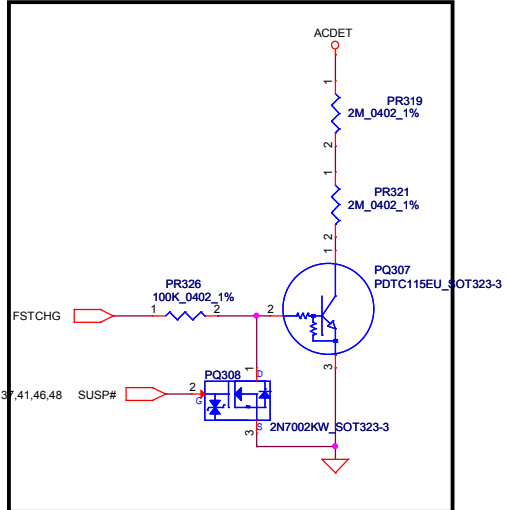
For KB9012 sense 20mΩ	Active	Recovery
65W	84W, 1.2V	56W, 0.793V
90W	117W, 1.2V	77W, 0.791V
120W		

```
PH201 under CPU bottom side :
CPU thermal protection at 92 degree C ( shutdown )
Recovery at 56 degree C
```

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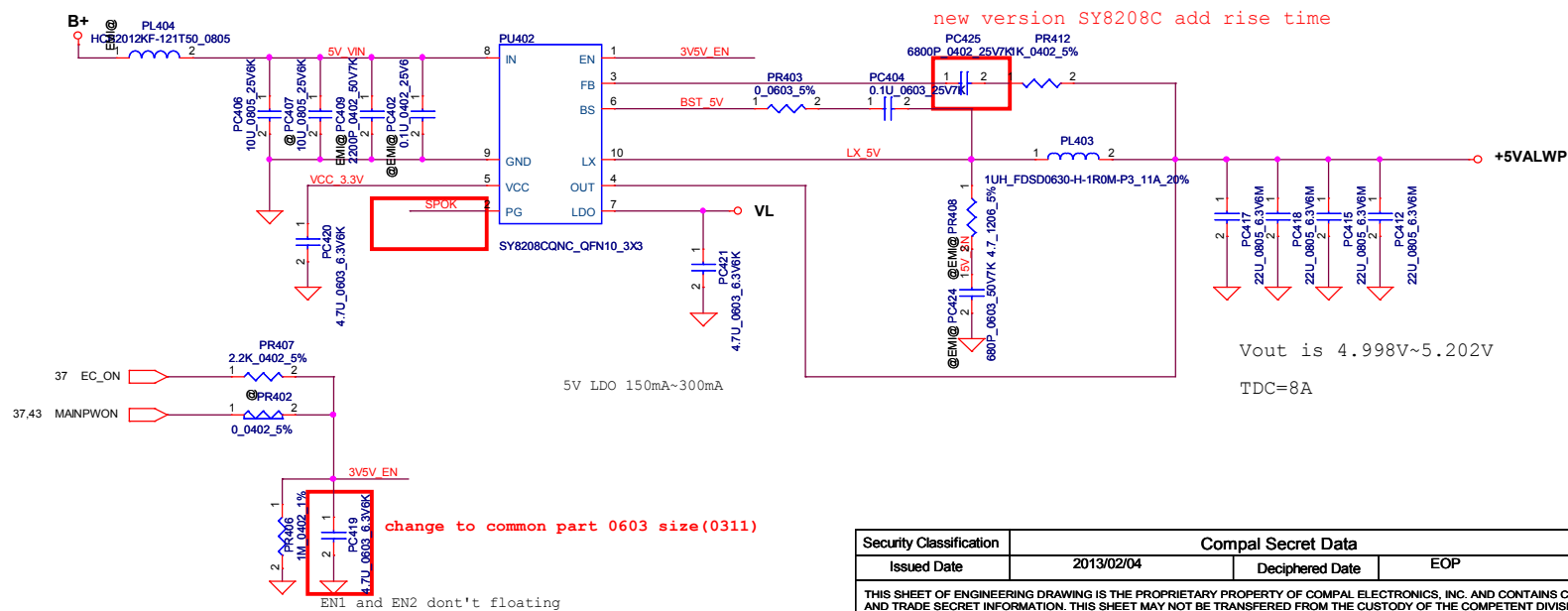
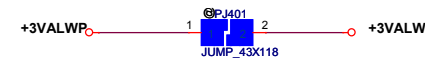
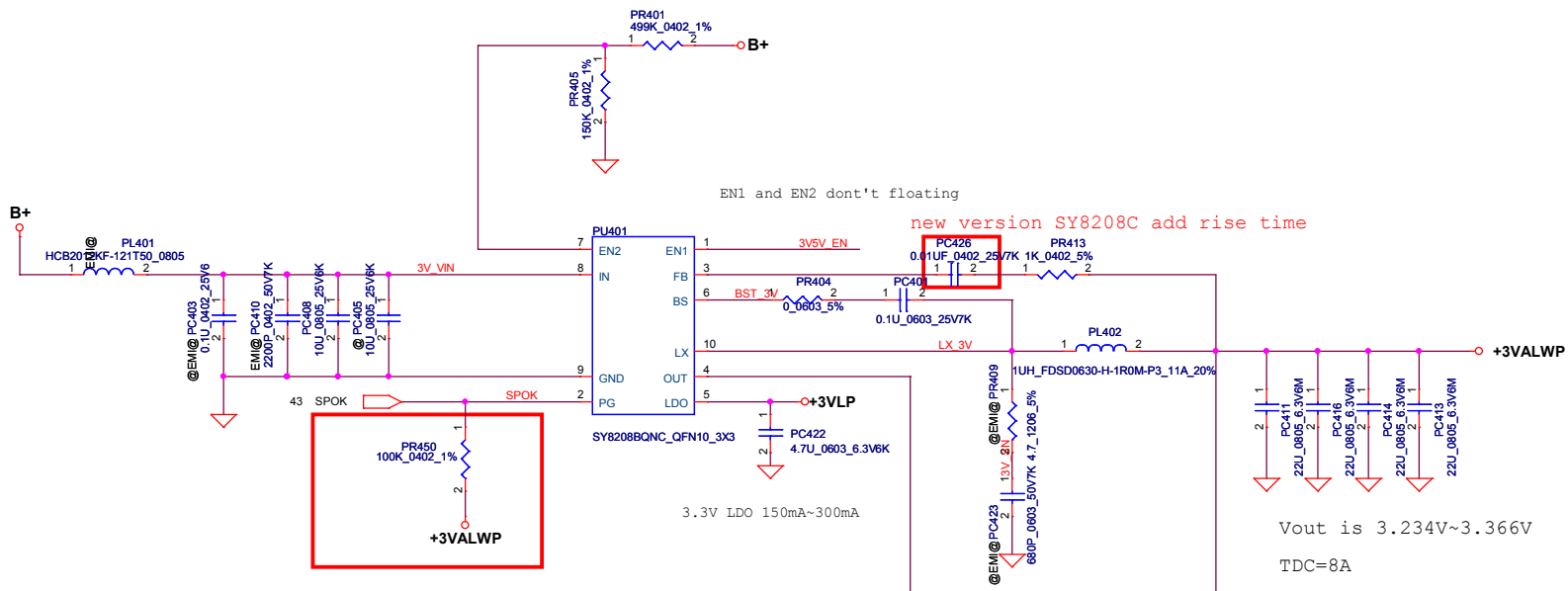


For 4S per cell 4.35V battery



Vin Detector			
	Min.	Typ	Max.
L-->H	17.520V	18.006V	18.504V
H-->L	16.967V	17.593V	18.237V

ILIM and external DPM			
	Min.	Typ	Max.
	3.906A	4.006A	4.108A



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2013/02/04			EOP			Document Number		
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2012/9/6

+0.75VSP

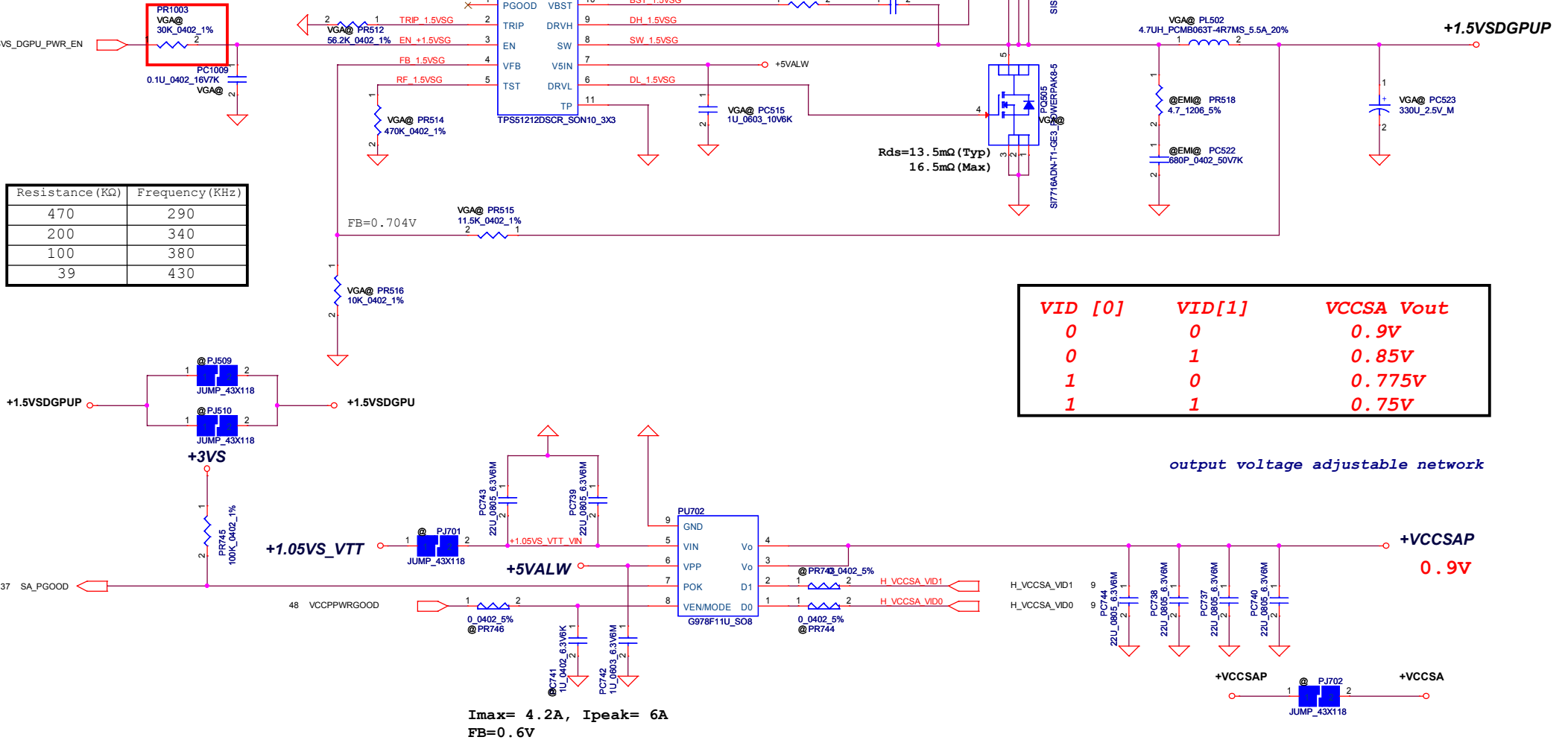


Note: S3 - sleep ; S5 - power off

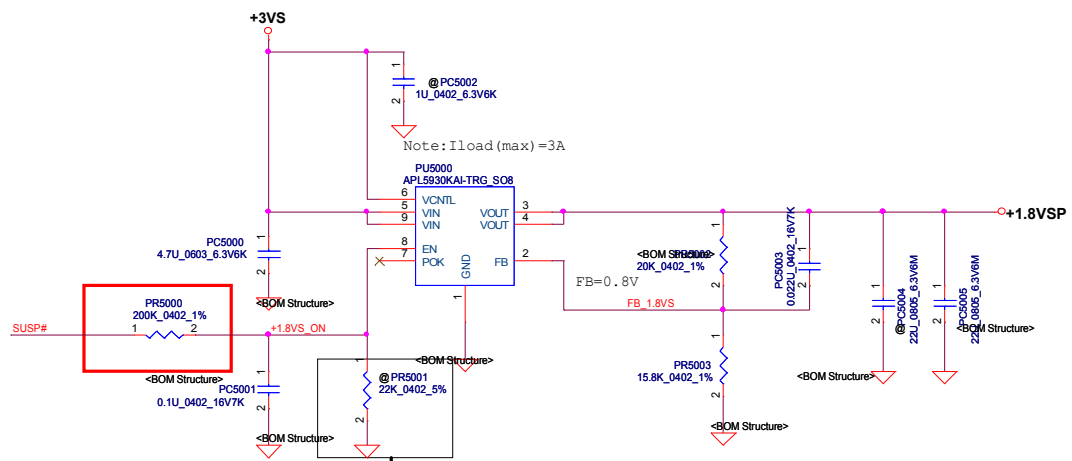
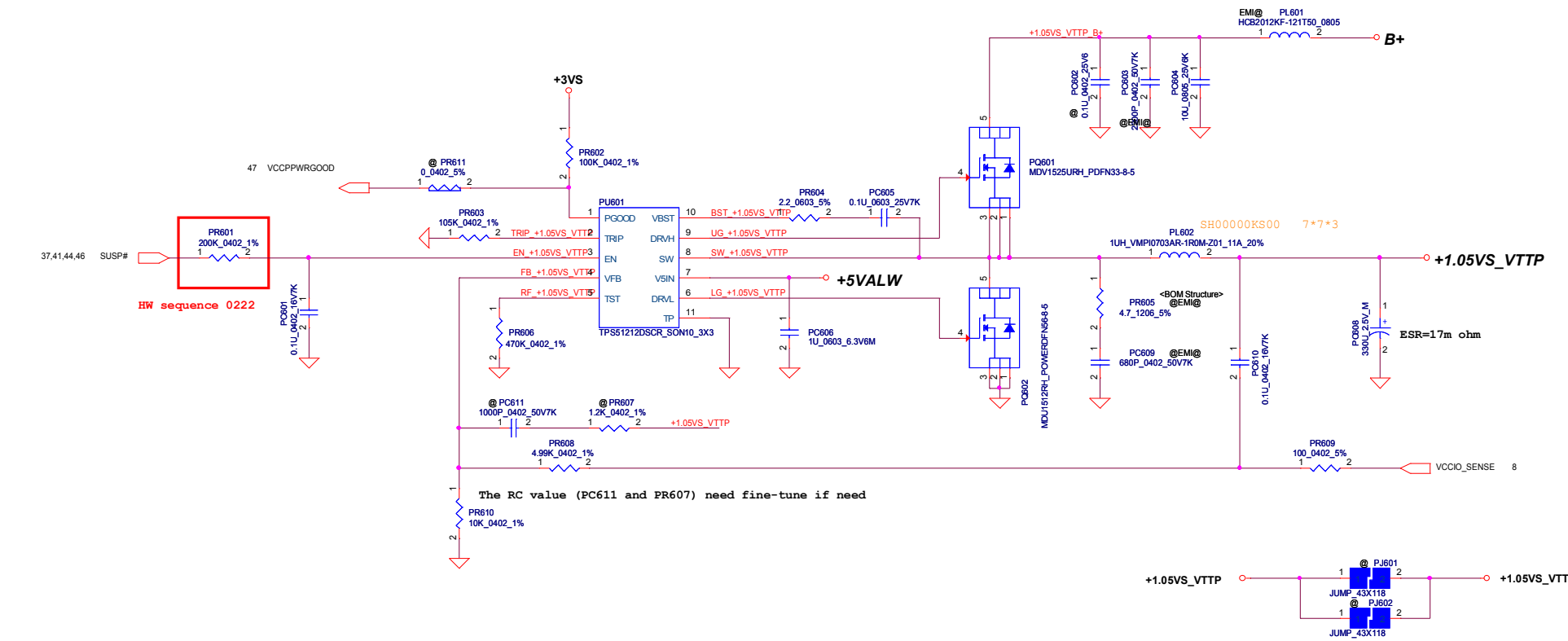
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				Size	Document Number	Rev
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$V_{FB} = 0.704V$
 $V_o = V_{FB} * (1 + 11.5K/10K) = 1.5V$
 $Freq = 290KHz (typ)$
 $C_{esr} = 15m\ ohm$
 $I_{peak} = 4.7A$ $I_{max} = 3.29A$ $I_{ocp} = 5.64A$
 $I_{ocp} = 5.72A \sim 6.43A$

HW sequence (0311)

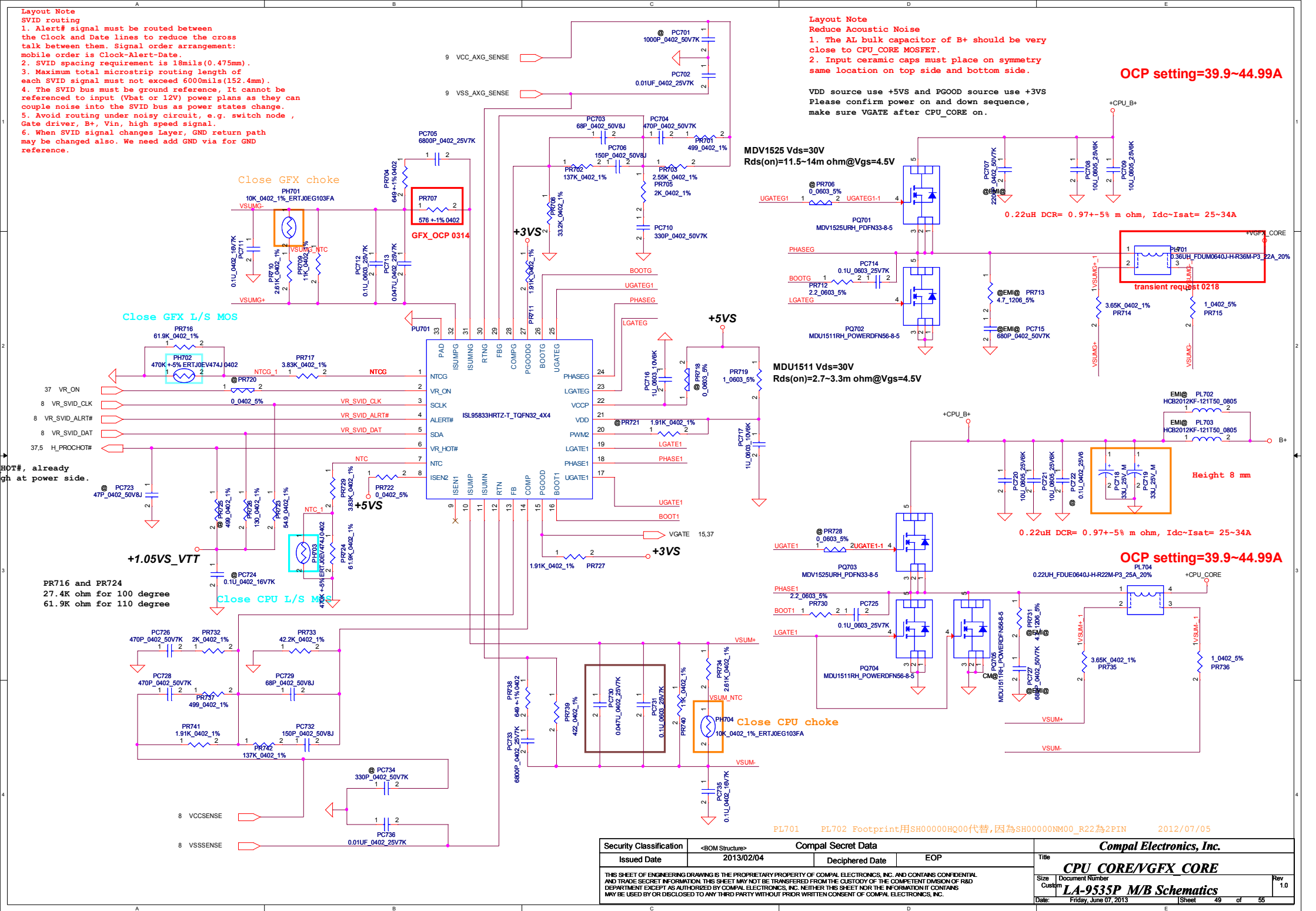


+1.05VSP Ipeak=5.36A ; Imax=3.752A ; 1.2Ipeak=6.432
Delta I=0.xxxxA=>1/2Delta I=0.xxxxA,F= 800K Hz(typ)

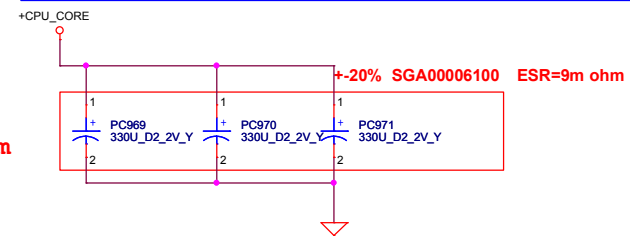
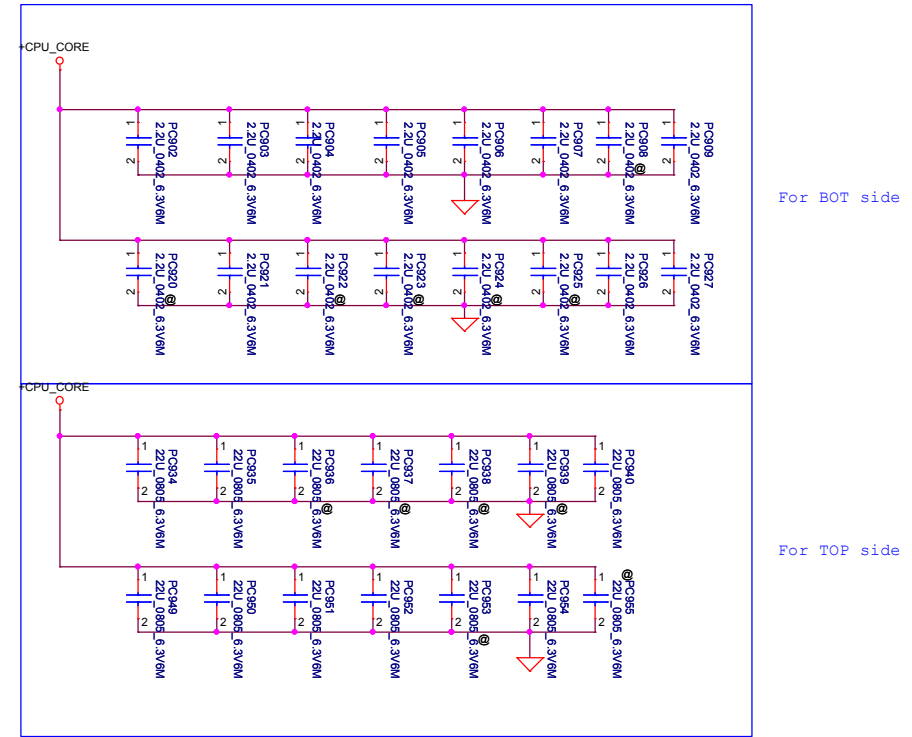
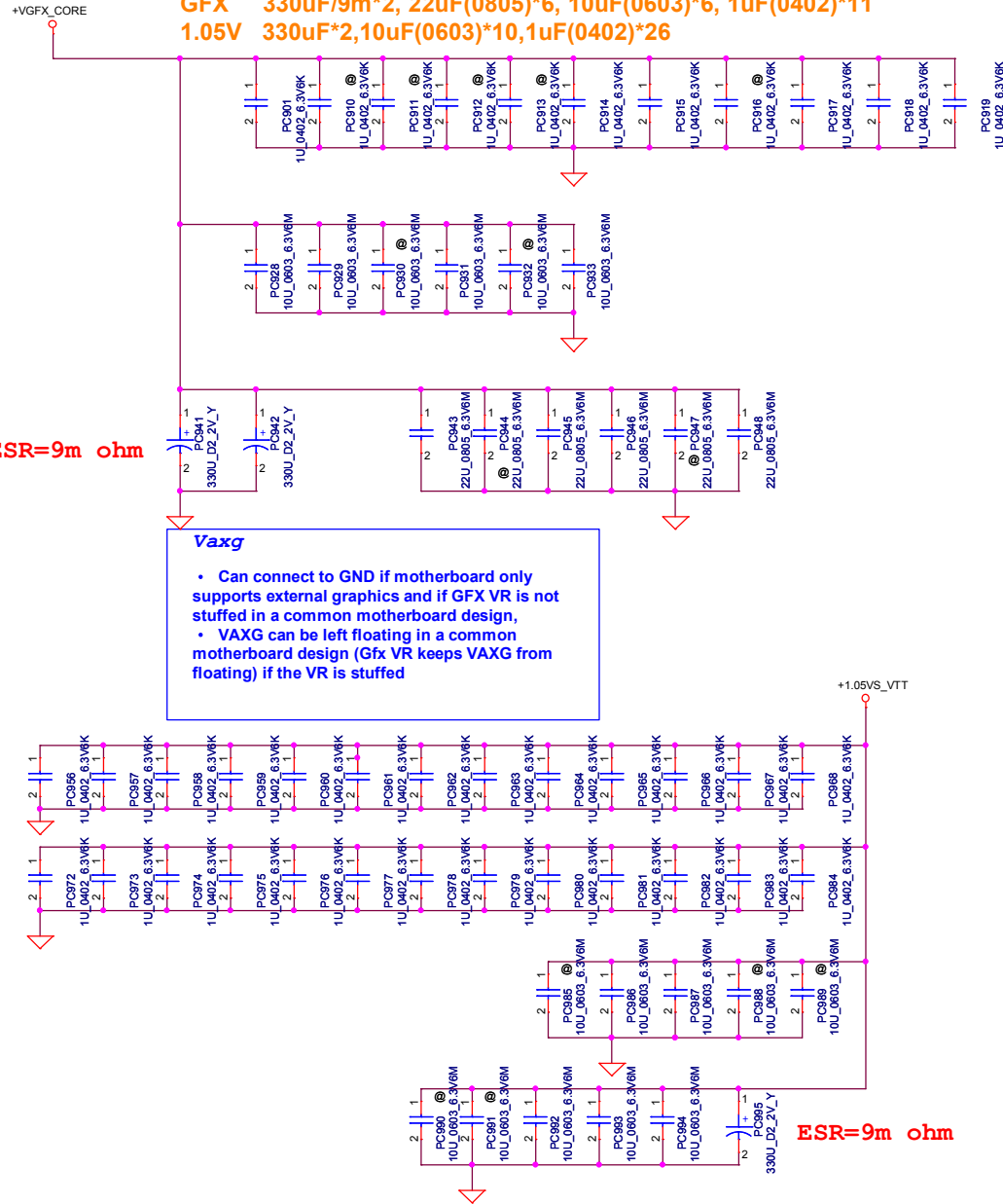


Ien=10uA, Vth=0.3V, notice
the res. and pull high
voltage from HW

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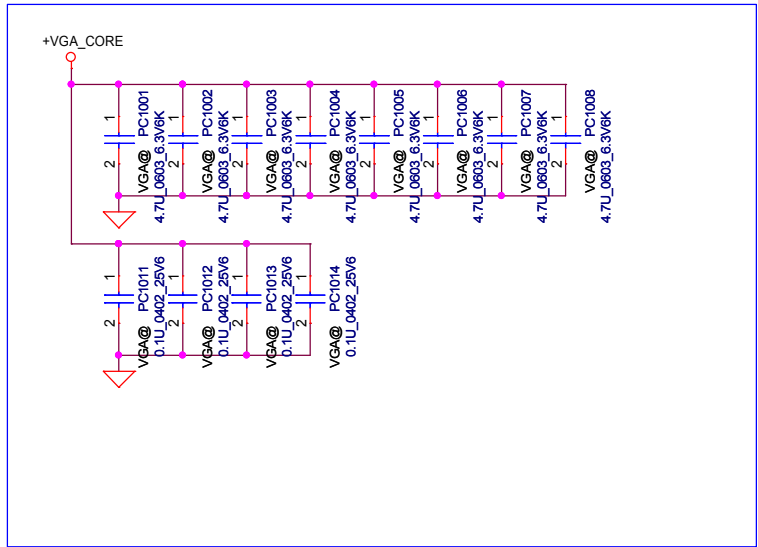


PWR Rule 17W@ULV(CR BGA1023_GT2) CPU2.9m GFx3.9m
CPU 330uF/9m *3, 22uF(0805) *12, 2.2uF(0402)*16
GFx 330uF/9m*2, 22uF(0805)*6, 10uF(0603)*6, 1uF(0402)*11
1.05V 330uF*2,10uF(0603)*10,1uF(0402)*26

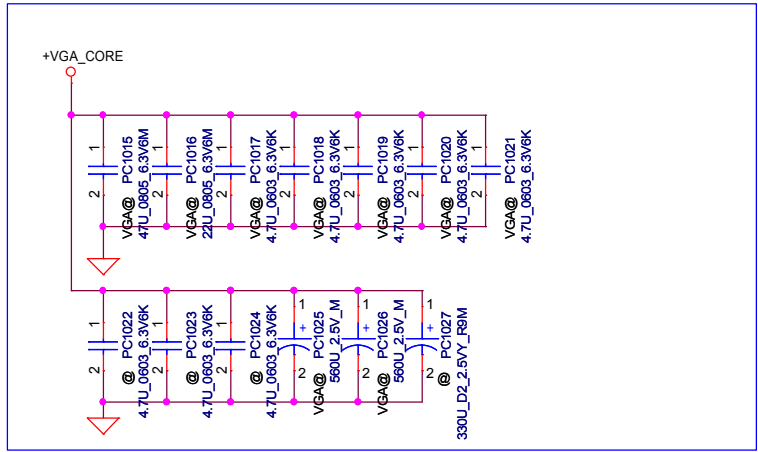


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CPU CORE CAP
LA-9535P M/B Schematics

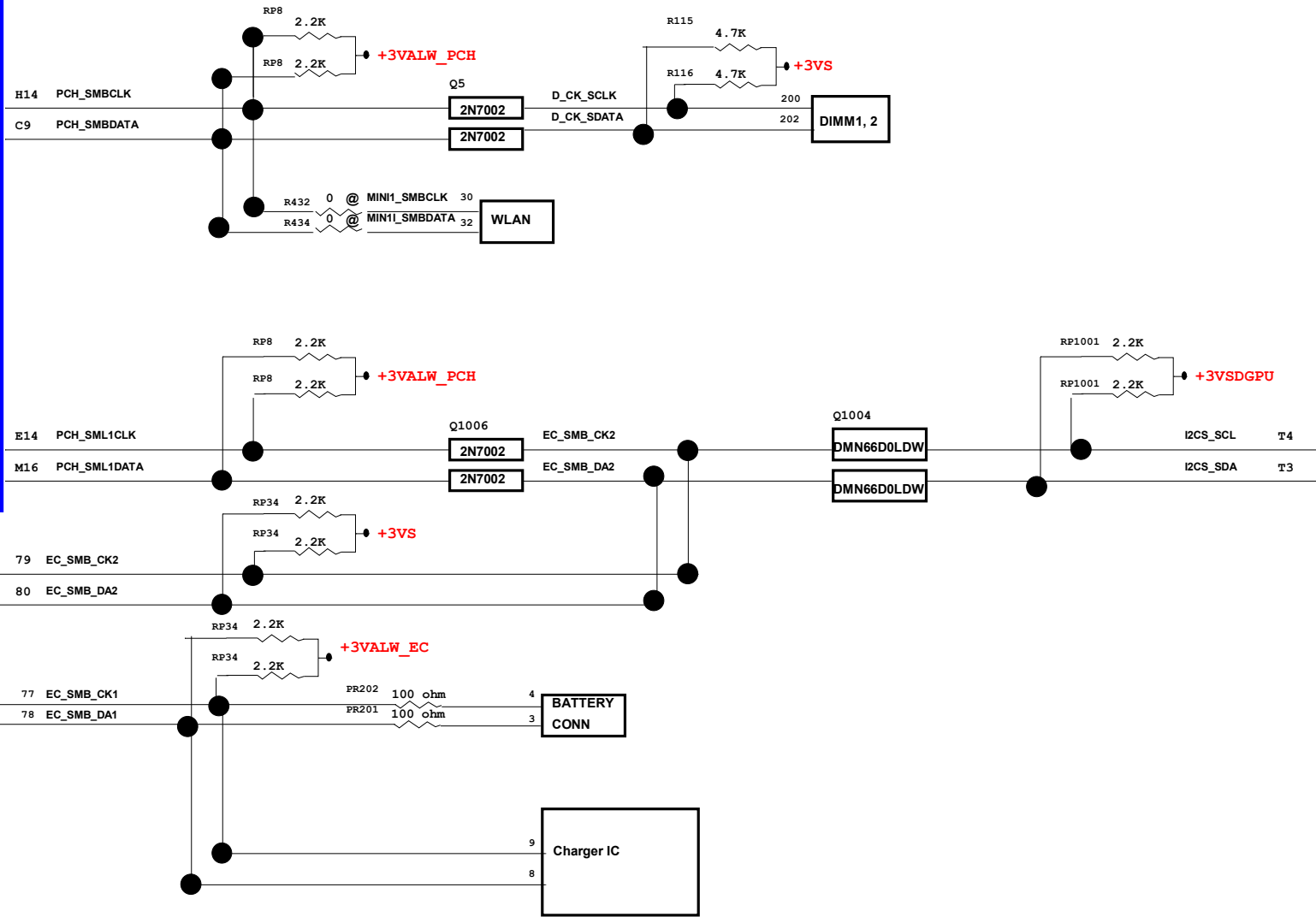
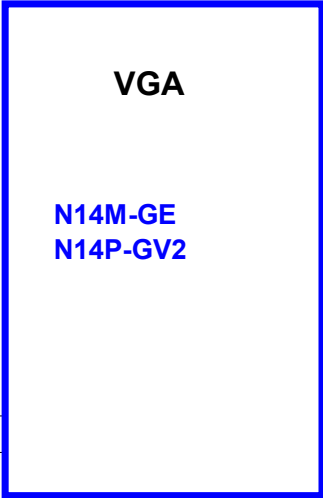
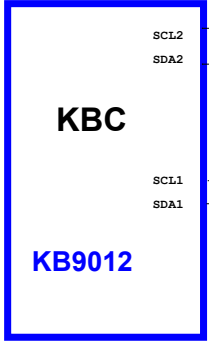
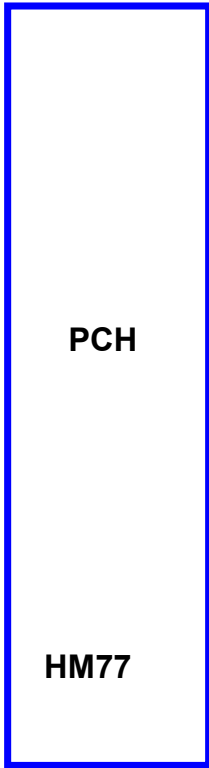


nVidia GB4-128 package
Under GPU
4.7uF 0603 * 10
0.1uF 0402 * 4



nVidia GB4-128 package
Near GPU
47uF 0805 *1
22uF 0805 *1
4.7uF 0805 *5 (0603)
330uF POS *1 <6mΩ

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Version change list (P.I.R. List)

Page 1 of 1
for PWR

Item	Reason for change	PG#	Modify List	Date	Phase
1	For 4S battery request	44	mount PR319,PR321,PR326,PQ307,PQ308	0310	C
2	change size to common part	45	PC419 change to 0603 common part	0310	C
3	HW sequence request	47	PR1003 to 30k	0311	C
4	EMI request	44	not mount PC307	0312	C
5	EMI request	44	add PC745 PC746 PC747	0313	C
6	EMI request	44	change PR311 PR310 to 2.2Ohm	0313	C
7	GFX_OCP	49	change PR707 to 576hm	0314	C
8					
9					
10					
11					
12					
13				3/5	EVT
14				3/5	EVT
15					
16					
17					
18					
19					
20					

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03/06
Change R1033 from 4.99K to 10K(ROM_SO VGA_DEVICE)
Change U51 N14P-GV2 from SA00006B500 to SA00006B510
Change Y6 P/N to SJ10000E800(合併用料)

03/11
Add net +XDPWR_SDPWR_MSPWR_R
Add share rom feature
Add R112 R140 R141 R144
Add EC_SPI_MISO_1 , PCH_SPI_MISO_1
Add EC_SPI_CS0# , PCH_SPI_CS0#
Add EC_SPI_CLK_1 , PCH_SPI_CLK_1
Add EC_SPI_MOSI_1 , PCH_SPI_MOSI_1
R541 pop 1K VGA@
R1101 470-->47 SD013470A80
D1000.3 VGA_PWROK changes into VGA_ON

SW3 @ 拿掉不上
Removed U15,R107,R108
Removed R151,R159,R160,R184,R97
Removed R524,R525,R526 換 RP13 5%--->1%

03/12
Add C441 470pF(SE074471K80),EMC@, EMI solution
Change U51 N14P-GV2 SA00006B510-->SA00006B530 R3 P/N
Change U51 N14M-GE SA000068A00-->SA000068A10 R3 P/N

0313a
Combine with PWR_Z5WE1_LA9535PR02_PWR_0313.DSN

0313b
Remove RP14,
PCH_GPIO2 不接
PCH_GPIO3 不接
PCH_GPIO53 不接

RP13 5%--->1%(SD300002Y00)

0313C
2nd rom 加回去
Add U15,R107,R108
Add R97 R151 R159 R160 R184
Del R112 R140 R141 R144

0314
R285 XEMC@-->EMC@
C329 22P-->10P, XEMC@-->EMC@

Add C230 0.1U for card reader enable

Board ID
R316 0ohm 改 8.2K 上件
R314 @-->改上件
C346 @-->改上件

0314C
R774 change from 10 to 56ohm
R1027,R1028,R1029,R1030,R1035,R1036,R1039,R1033,R1042
at N14M-GE SKU 10K_0402_5% change to 10K_0402_1%

0314d
L33 changes into SM010014520

0315a
Add net CRT_4, CRT_11 for 測點
R541 bom structure--->VGA@
C346 board ID cap改@ 不上

0318
L24,L25 change from SM070001600 (12ohm USB3.0 common mode choke)
to SM070001R00 (Murata 67ohm)

0419
Add Touch screen feature and JTS1

0422
Remove PEG 16X

0425
Add HM70 NM70 文字敘述
Add FFR VRAM strap for N14M-GE N14P-GV2

0502
Update CPU,PCH,VRAM P/N

0505
Pop RP16 for LAN loopback

0528
N14M-GE ROM_SO keep 10K pull low.
N14P-GV2 need change be to EVT R1033 as 4.99K_0402_1%

C142-->15pF(SE071150J80) to meet off mode timing

0604
Correct page1 date code
Update page24 3D device/vga device notice

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						Size		Document Number		Rev	
						Custom		LA-9535P M/B Schematics		1.0	
						Date:		Friday, June 07, 2013		Sheet 55 of 55	

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