

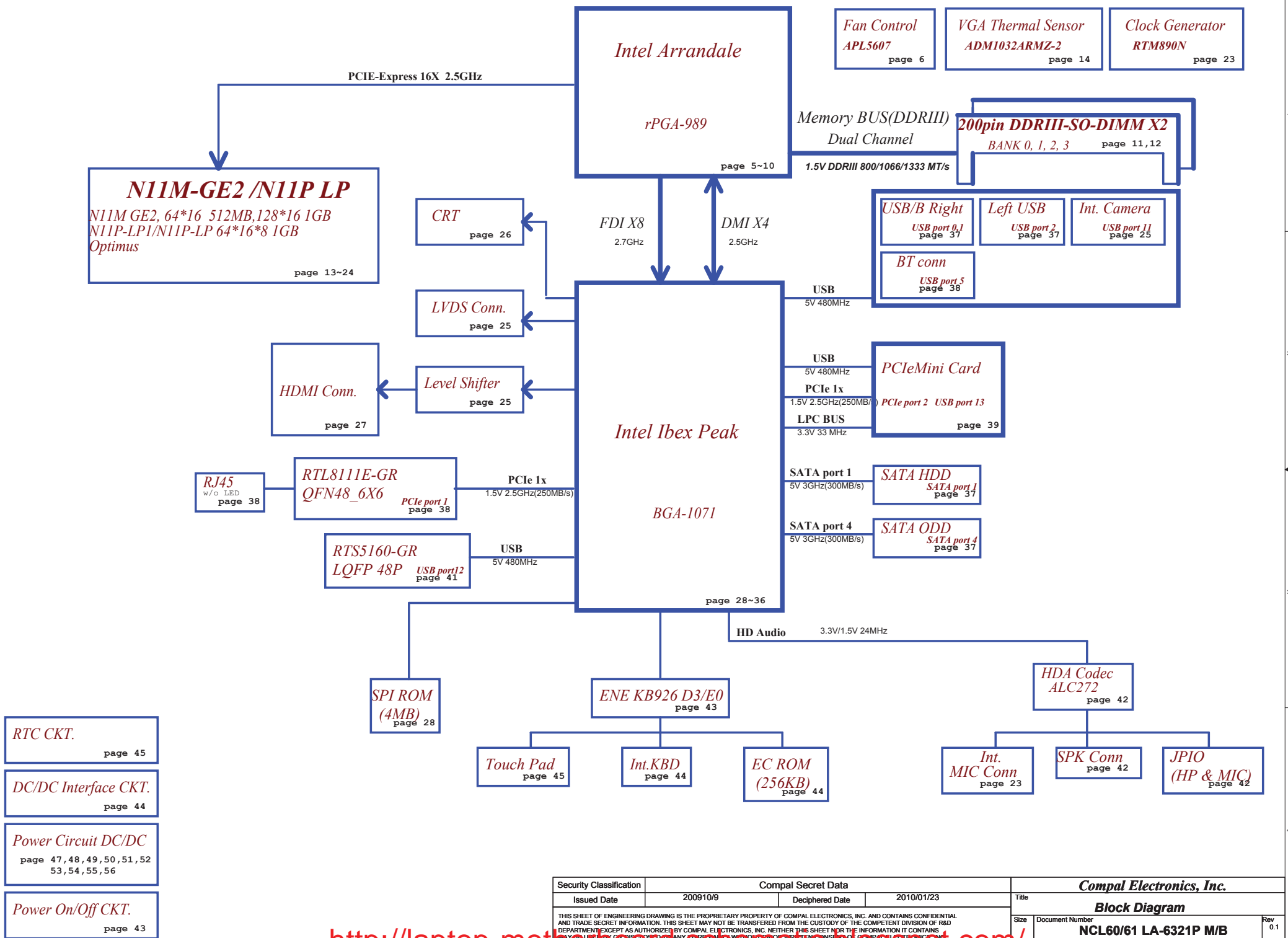
# NCL60/61

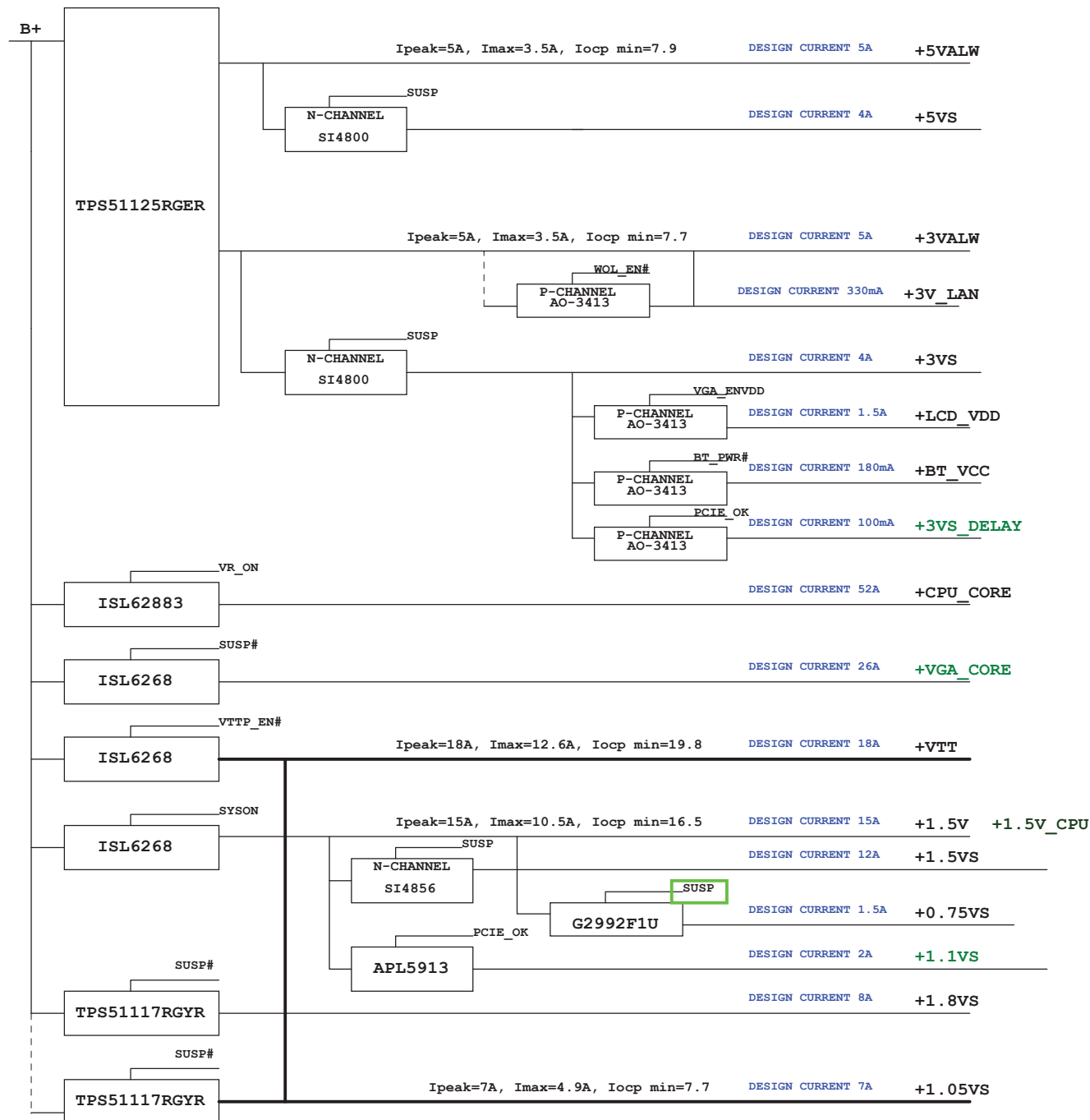
## LA-6321P REV 1.0 Schematic

Intel Processor ARD/ PCH HM55/NV N11M GE2, N11P-LP,  
N11P-LP1 (optimus)

2010-04-19 Rev 1.0

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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				Date: Monday, April 19, 2010	Rev 0.1
				Sheet 1 of 59	





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					NCL60/61 LA-6321P M/B
				Date:	Wednesday, March 24, 2010
				Sheet	3 of 59
				Rev	0.1

Voltage Rails

( O MEANS ON X MEANS OFF )

power plane State	+RTCVCC	+B	+5VL +3VL	+5VALW +3VALW +VSB	+1.5V	+5VS +3VS +1.5VS +VGA_CORE +CPU_CORE +VTT +1.05VS +1.8VS +1.1VS +0.75VS
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

Platform	SKU	CPU	PCH	VGA
Calpella	UMA	Arrandale	HM55	N/A
	DIS (OPT@)	Arrandale	HM55	N11M-GE2

BOM configu table

SKU	Description	Bom configu	
1	UMA W/O TPM W/HDMI	UMA@/PCB@/HDMI@/NTPM@	45188030L01
2	UMA W/O TPM W/O HDMI	UMA@/PCB@/NHDMI@/NTPM@	45188030L02
3	DIS (N11M) W/HDMI W/TPM 1G VRAM	TPM@/PCB@/OPT@/N11M@/SAM1G@/HDMI@	45188030L14
4	DIS (N11M) W/HDMI W/OTPM 1G VRAM	NTPM@/PCB@/OPT@/N11M@/HY1G@/HDMI@	45188030L12
5	DIS (N11M) W/HDMI W/TPM 512MB VRAM	TPM@/PCB@/OPT@/N11M@/HY512@/HDMI@/512@/8PCS@	45188030L11
6	DIS (N11M) W/HDMI W/O TPM 512M VRAM	NTPM@/PCB@/OPT@/N11M@/SM512@/HDMI@	45188030L13
7	DIS (N11P) W/HDMI WTPM 1GB VRAM		
8	DIS (N11P) W/HDMI W/O TPM 1GB VRAM	NTPM@/PCB@/OPT@/N11P@/HDMI@/8PCS@/LP@	45188030L15

N11M	Hynix 512	X7623130L01
N11M	SAM 512	X7623130L02
N11M	Hynix 1G	X7623130L03
N11M	SAM 1G	X7623130L04
N11P	Hynix 1G	X7623130L05
N11P	SAM 1G	X7623130L06

EC SM Bus1 address

Power	Device	Address	Power	Device	Address
+3VL	EC KB926 D3		+3VS	EC KB926 D3	
+3VL	Smart Battery	0001 011x b	+3VS	AMD GPU Thermal Sensor	1001 101x b
			+3VALW	PCH	1001 011x b

EC SM Bus2 address

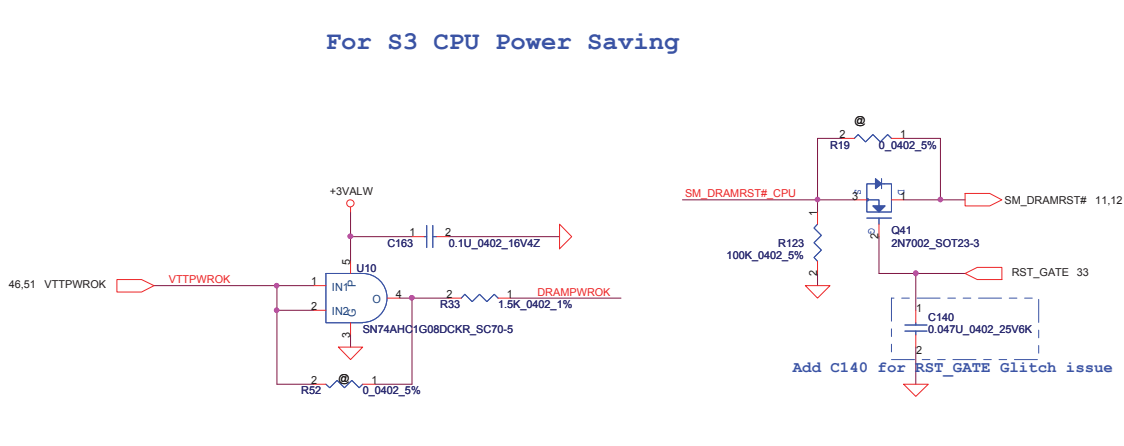
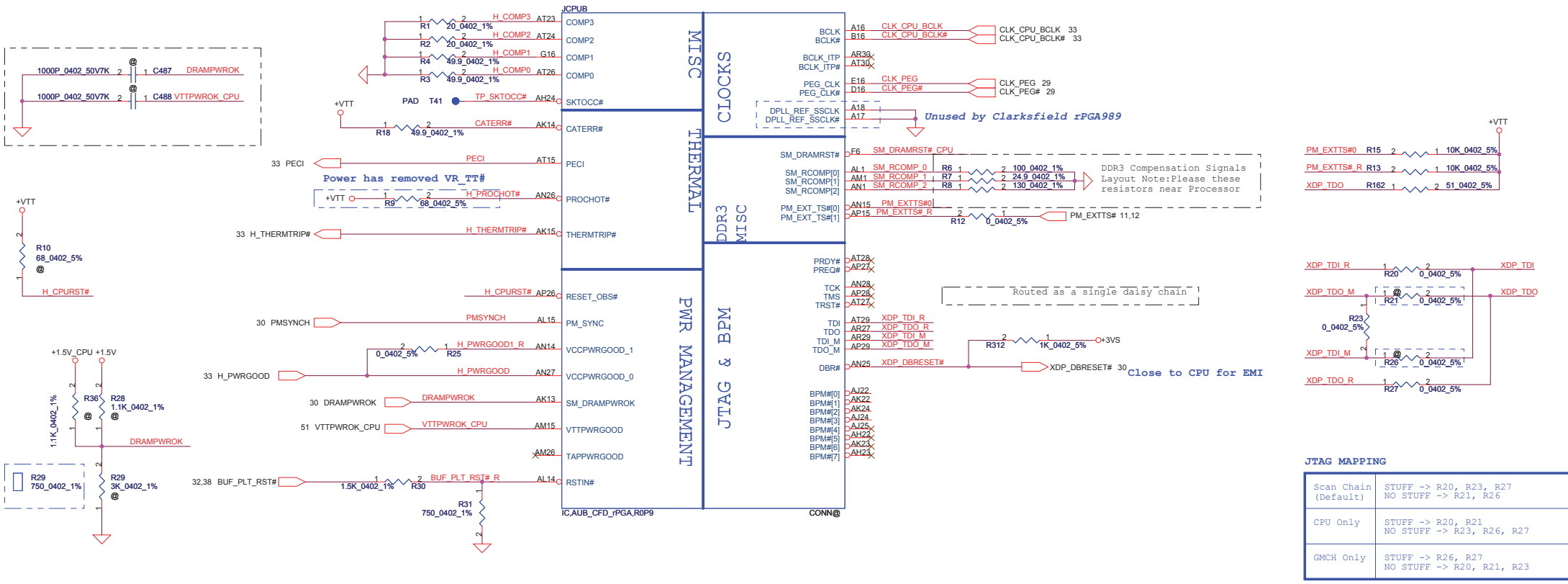
STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON		HIGH	HIGH	HIGH
S1 (Power On Suspend)		HIGH	HIGH	HIGH
S3 (Suspend to RAM)		LOW	HIGH	HIGH
S4 (Suspend to Disk)		LOW	LOW	HIGH
S5 (Soft OFF)		LOW	LOW	LOW
G3		LOW	LOW	LOW

PCH SM Bus address

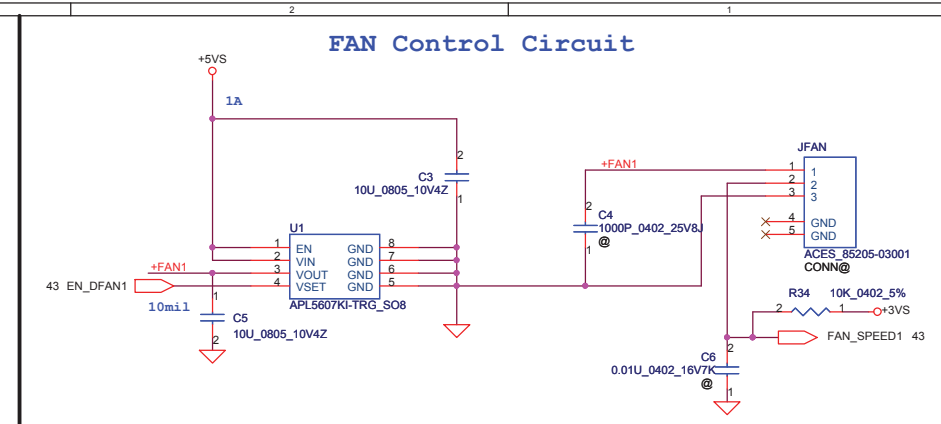
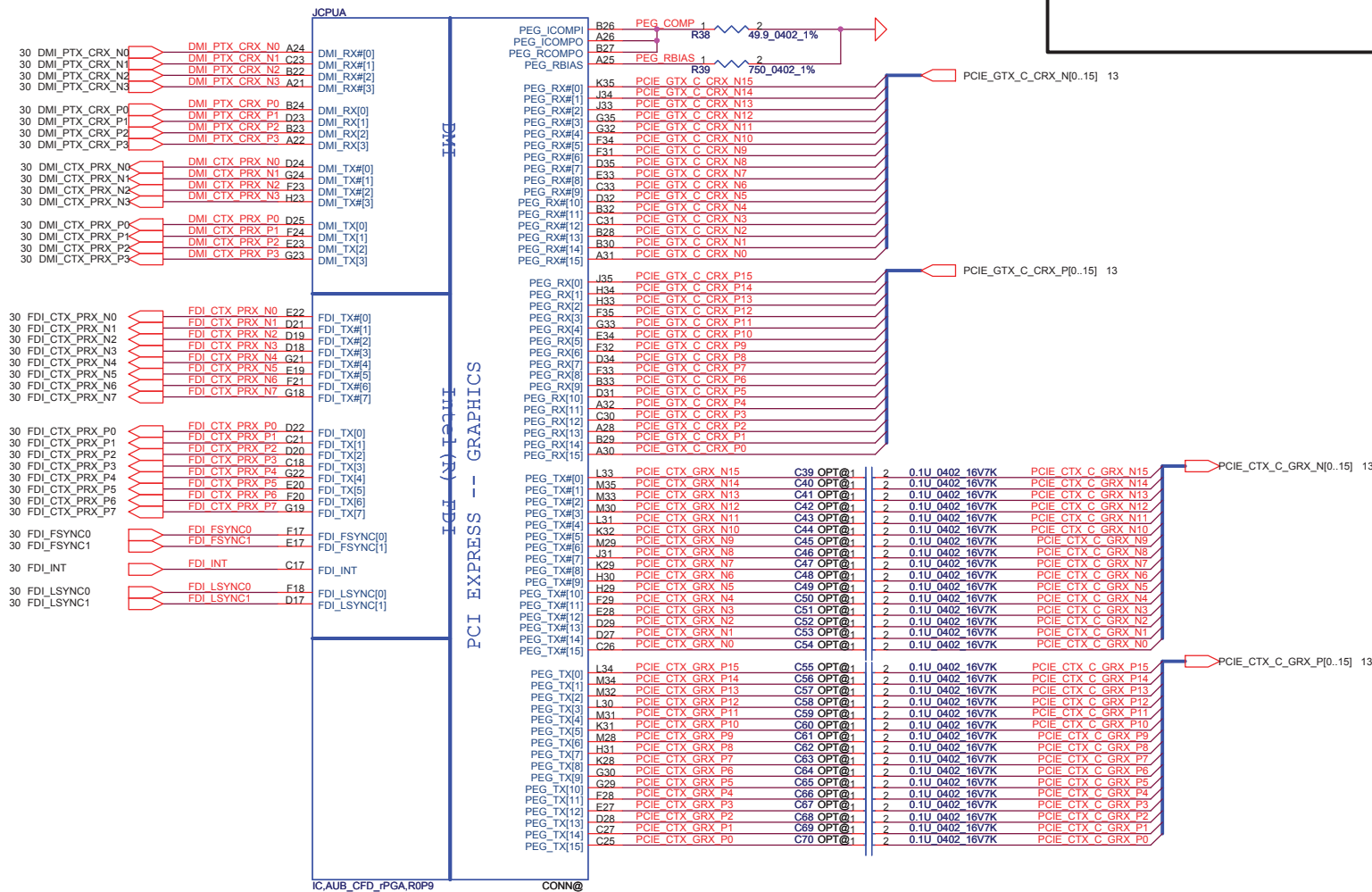
Power	Device	Address
+3VALW	PCH	
+3VS	Clock Generator	1101 001x b
+3VS	DDR DIMMA	1001 000x b
+3VS	DDR DIMMB	1001 010x b
+3VS	WLAN	Reserved for common design.

<input type="checkbox"/> ZZZ HY512@ N11M Hynix 512	<input type="checkbox"/> ZZZ SM512@ N11M SAM 512	<input type="checkbox"/> ZZZ HY1G@ N11M Hynix 1G
<input type="checkbox"/> ZZZ SAM1G@ N11M SAM 1G	<input type="checkbox"/> ZZZ N11P@ N11P Hynix	<input type="checkbox"/> SAM1G N11P SAM @
<input type="checkbox"/> UV1 N11M-GE2	<input type="checkbox"/> UV1 N11P-LP	<input type="checkbox"/> UV1 N11P-LP

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				Size Document Number Custom NCL60/61 LA-6321P M/B
				Date: Wednesday, March 31, 2010 Sheet 4 of 59 Rev 0.1

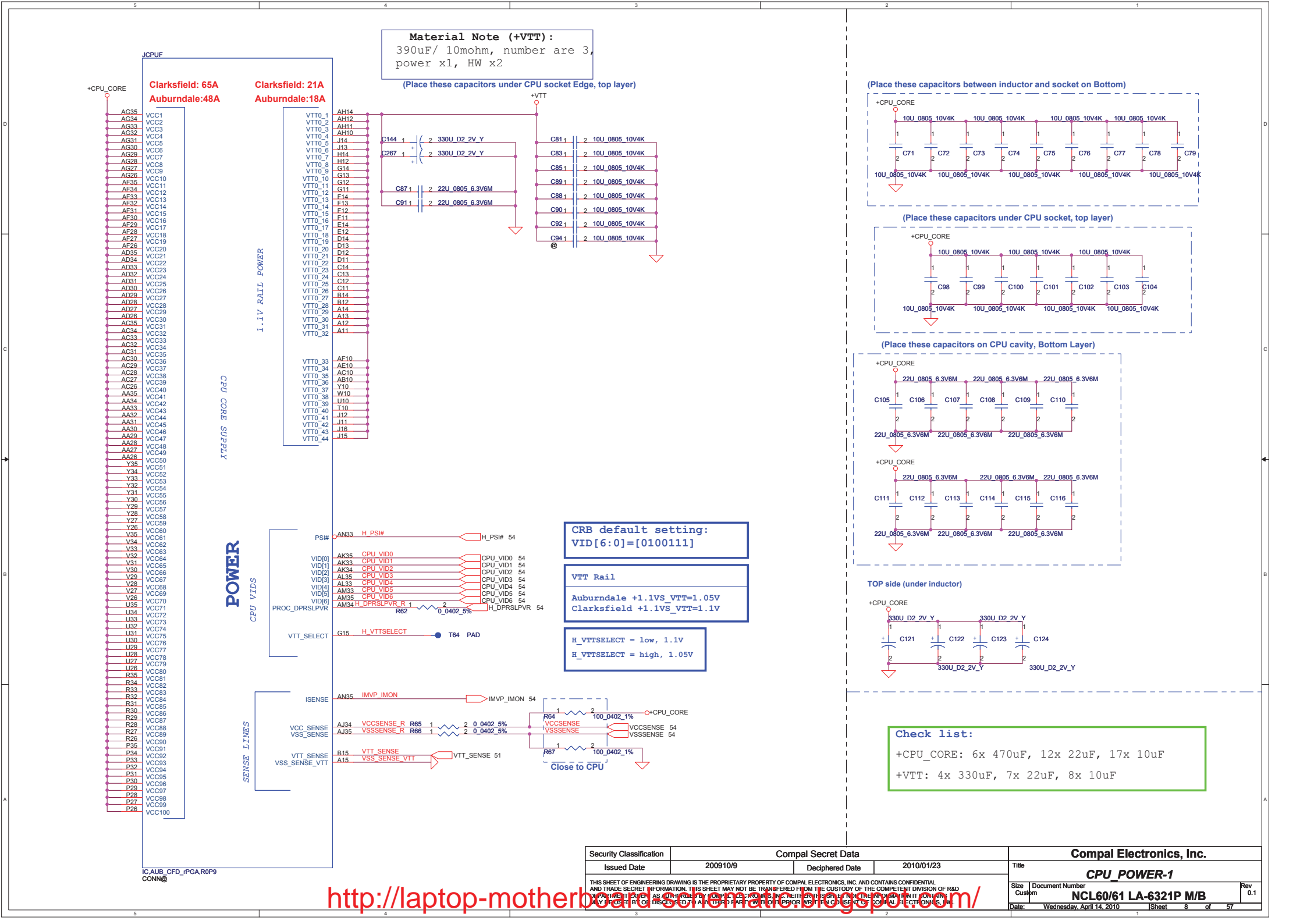


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Size	Custom	Document Number	NCL60/61 LA-6321P M/B	Rev	0.1
Date:	Thursday, April 15, 2010	Sheet	5	of	57

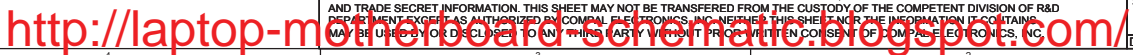


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				Document Number	NCL60/61 LA-6321P M/B
				Date	Wednesday, April 14, 2010
				Sheet	6 of 57

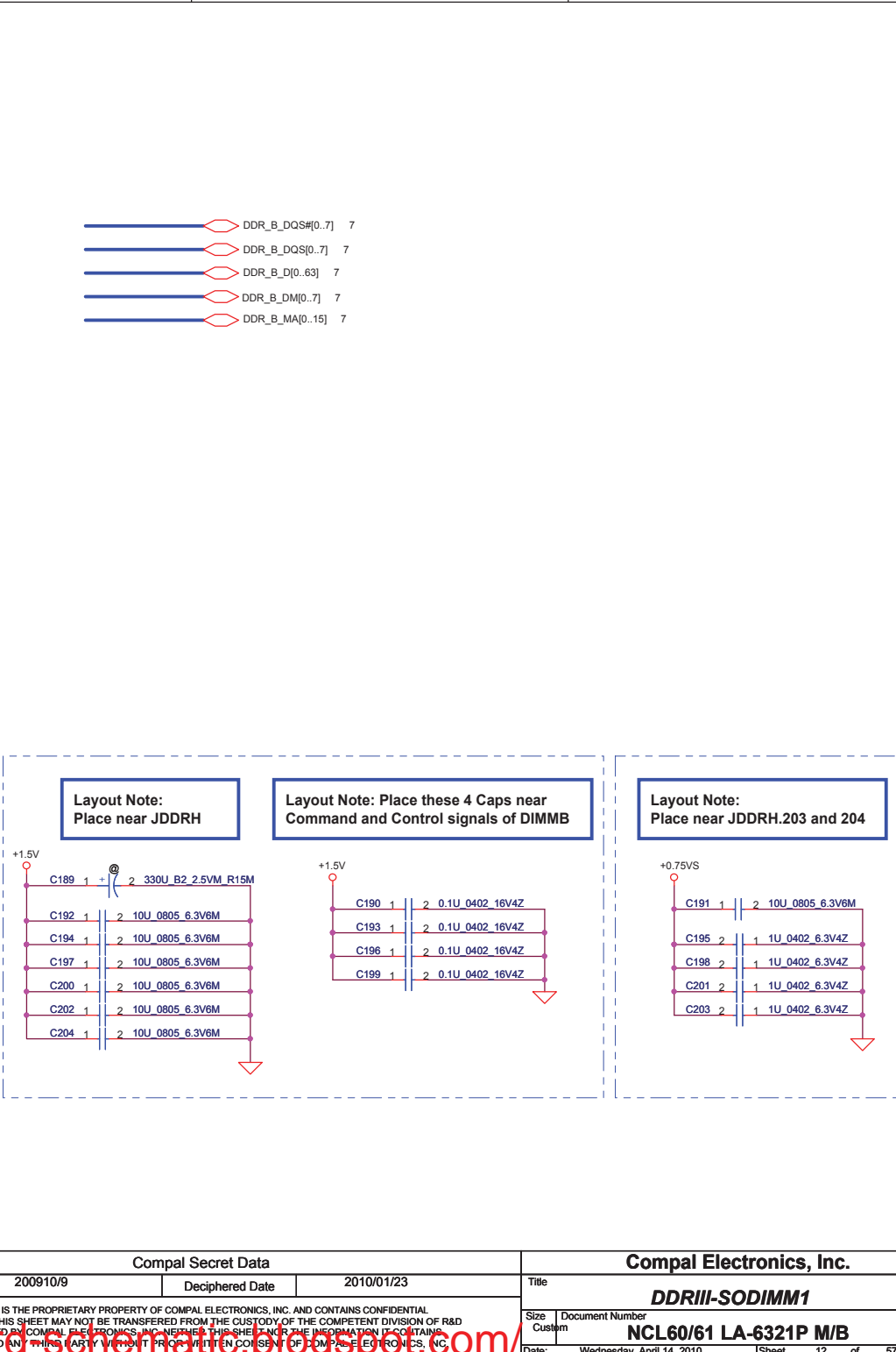
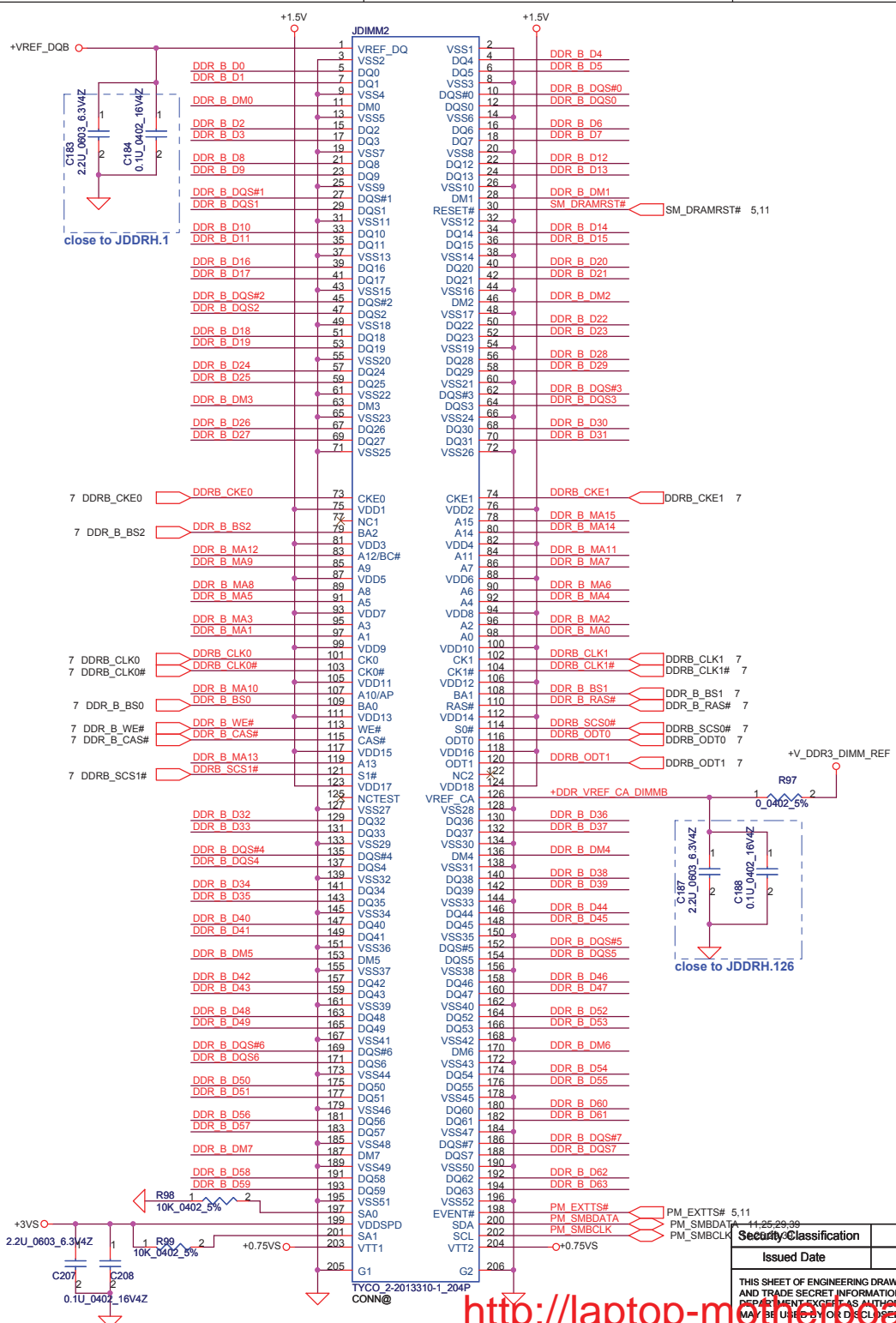










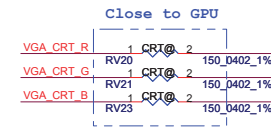
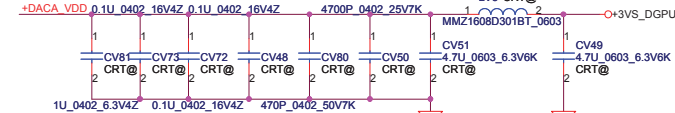
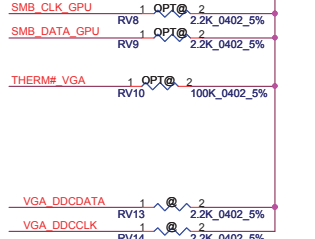
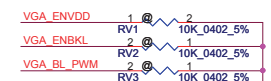
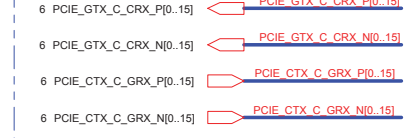
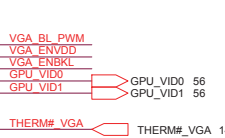
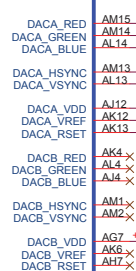
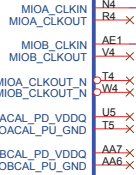
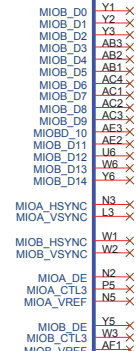
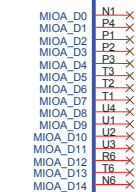
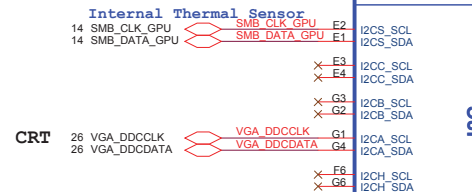
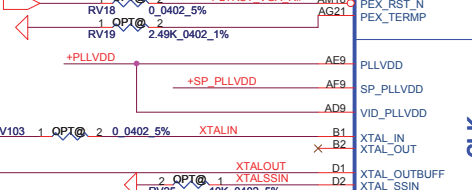
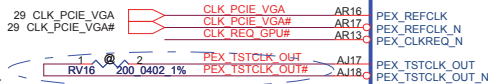
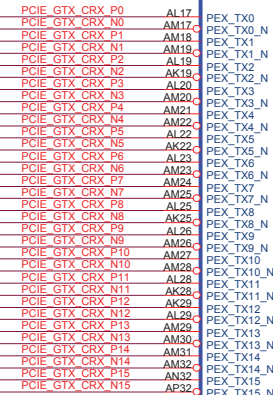
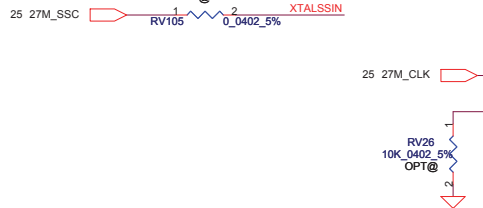
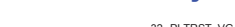
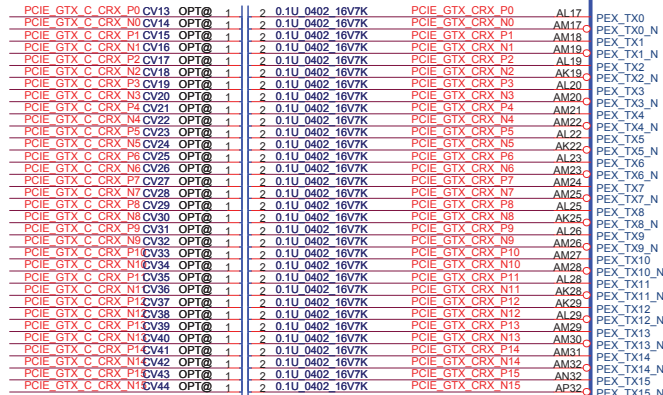
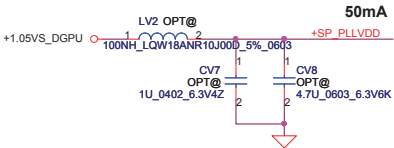


**Layout Note:**  
Place near JDDR.H

**Layout Note:** Place these 4 Caps near Command and Control signals of DIMMB

**Layout Note:**  
Place near JDDR.H.203 and 204

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								Size		Document Number				Rev	
								Custom		NCL60/61 LA-6321P M/B				0.1	
								Date:		Wednesday, April 14, 2010		Sheet		12 of 57	



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					60/61 LA-6321P M/B
				Date	Wednesday, April 14, 2010
				ISheet	13 of 59



N11P-GS1 Performance Mode

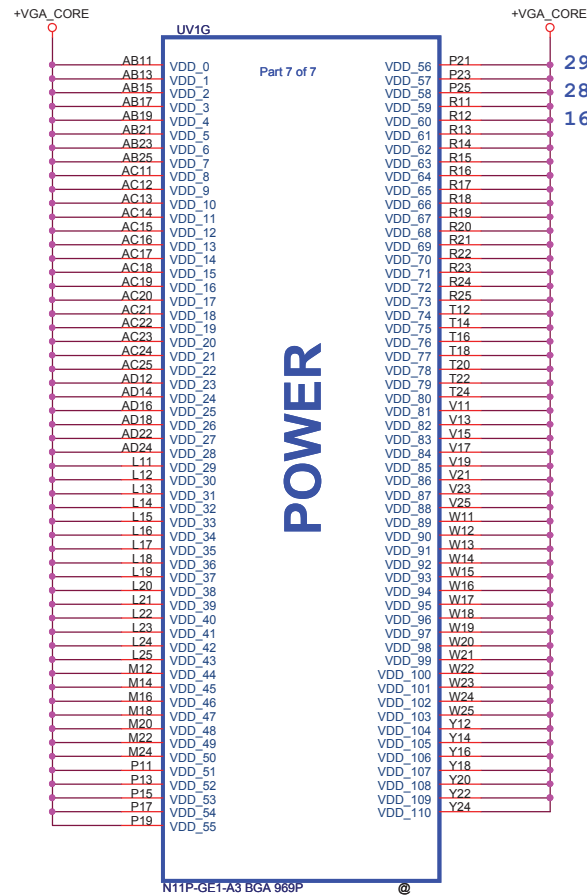
Mode	NVCLK (MHz)	MCLK (MHz)	+VGA_CORE
P0	450	790	0.90 V
P8	405	324	0.85 V
P12	135	135	0.80 V

N11P-GE1 Performance Mode

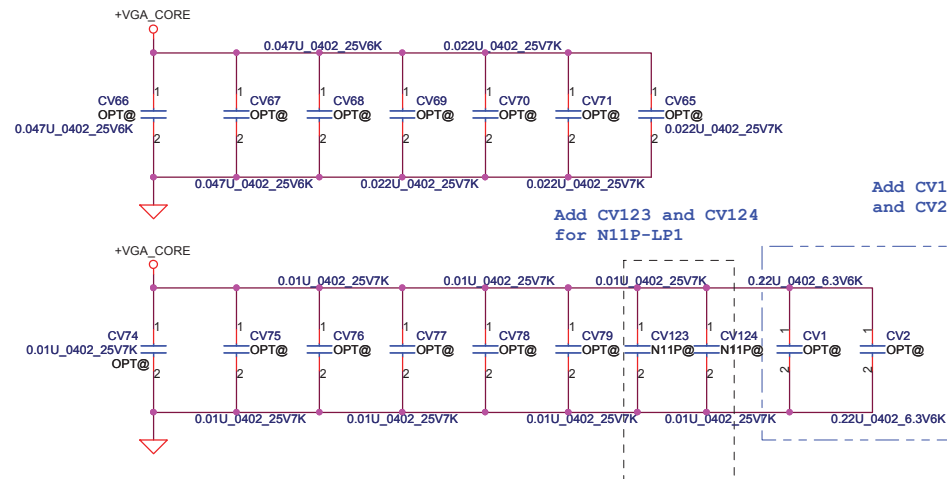
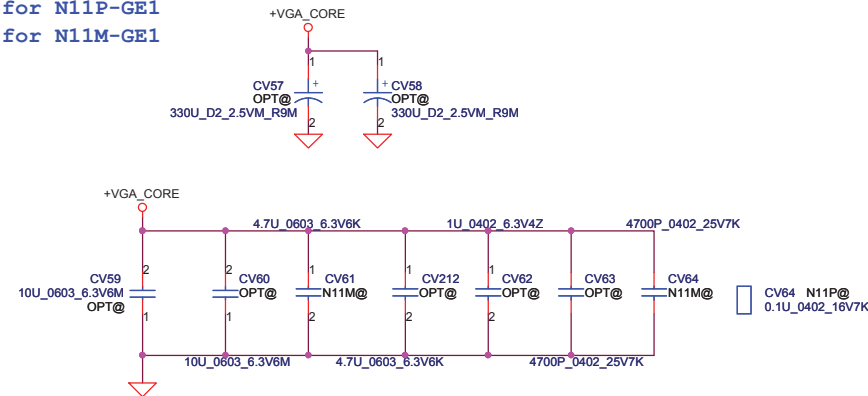
Mode	NVCLK (MHz)	MCLK (MHz)	+VGA_CORE
P0	575	790	0.95 V
P8	405	324	0.85 V
P12	135	135	0.80 V

N11M-GE1 Performance Mode

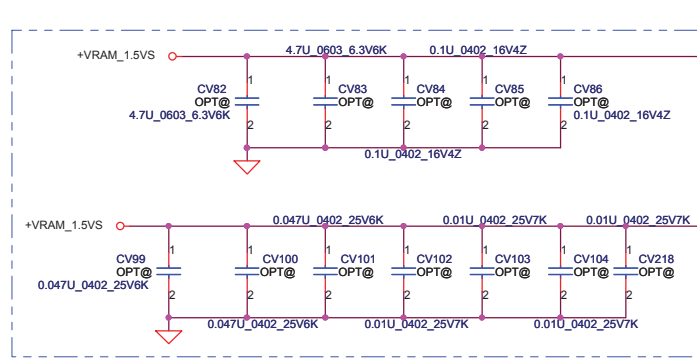
Mode	NVCLK (MHz)	MCLK (MHz)	+VGA_CORE
P0	625	790	1.03 V
P8	405	405	0.85 V
P12	135	135	0.85 V



29A for N11P-GS1  
28A for N11P-GE1  
16A for N11M-GE1



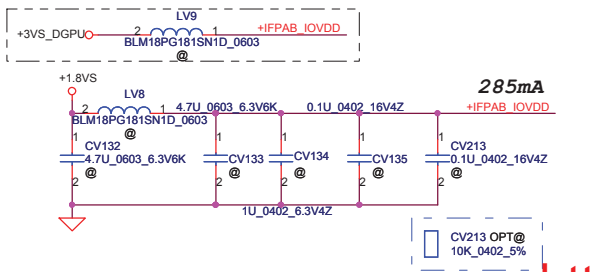
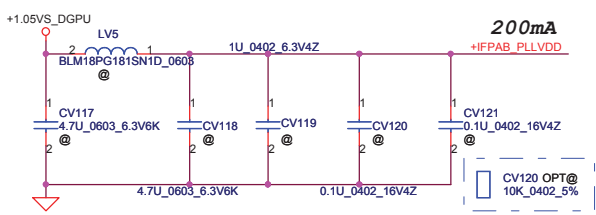
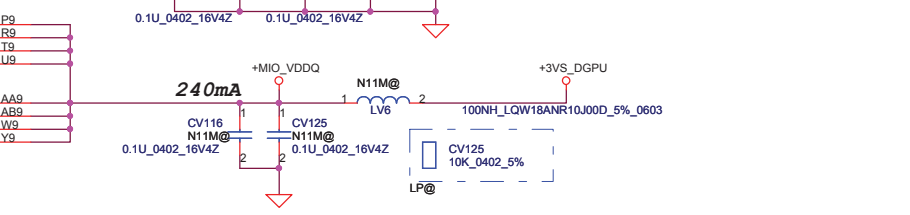
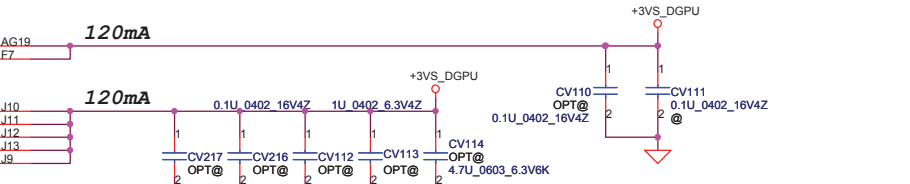
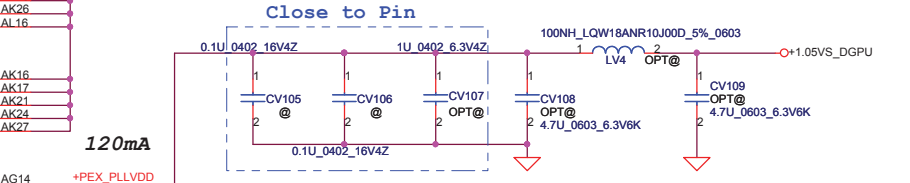
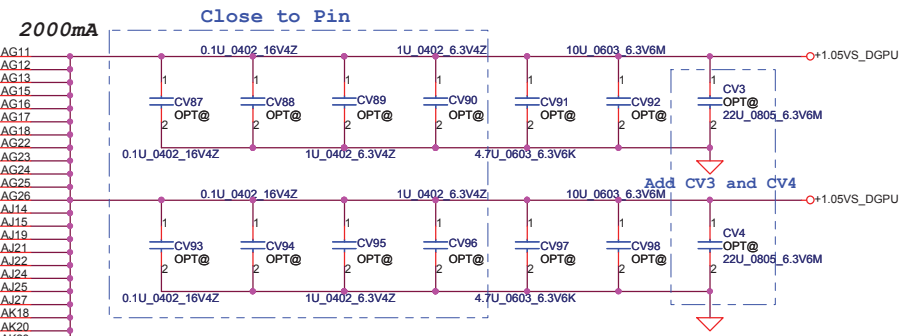
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						NCL60/61 LA-6321P M/B	0.1
					Date:	Thursday, April 15, 2010	Sheet 15 of 59



- 3.5A**
- UVIE
- Part 5 of 7
- 1600mA**
- 2000mA**
- 500mA**
- 110mA**
- 120mA**
- 120mA**
- 240mA**
- 200mA**
- 285mA**

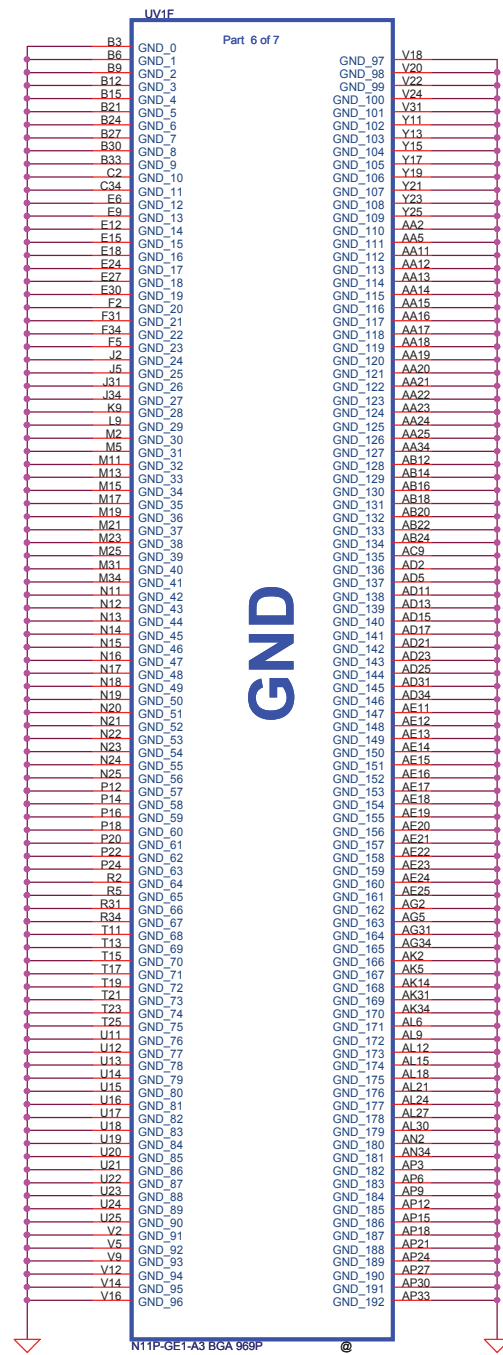
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VDD33\_2  
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MIOA\_VDDQ\_3
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- N11P-GE1-A3 BGA 969P



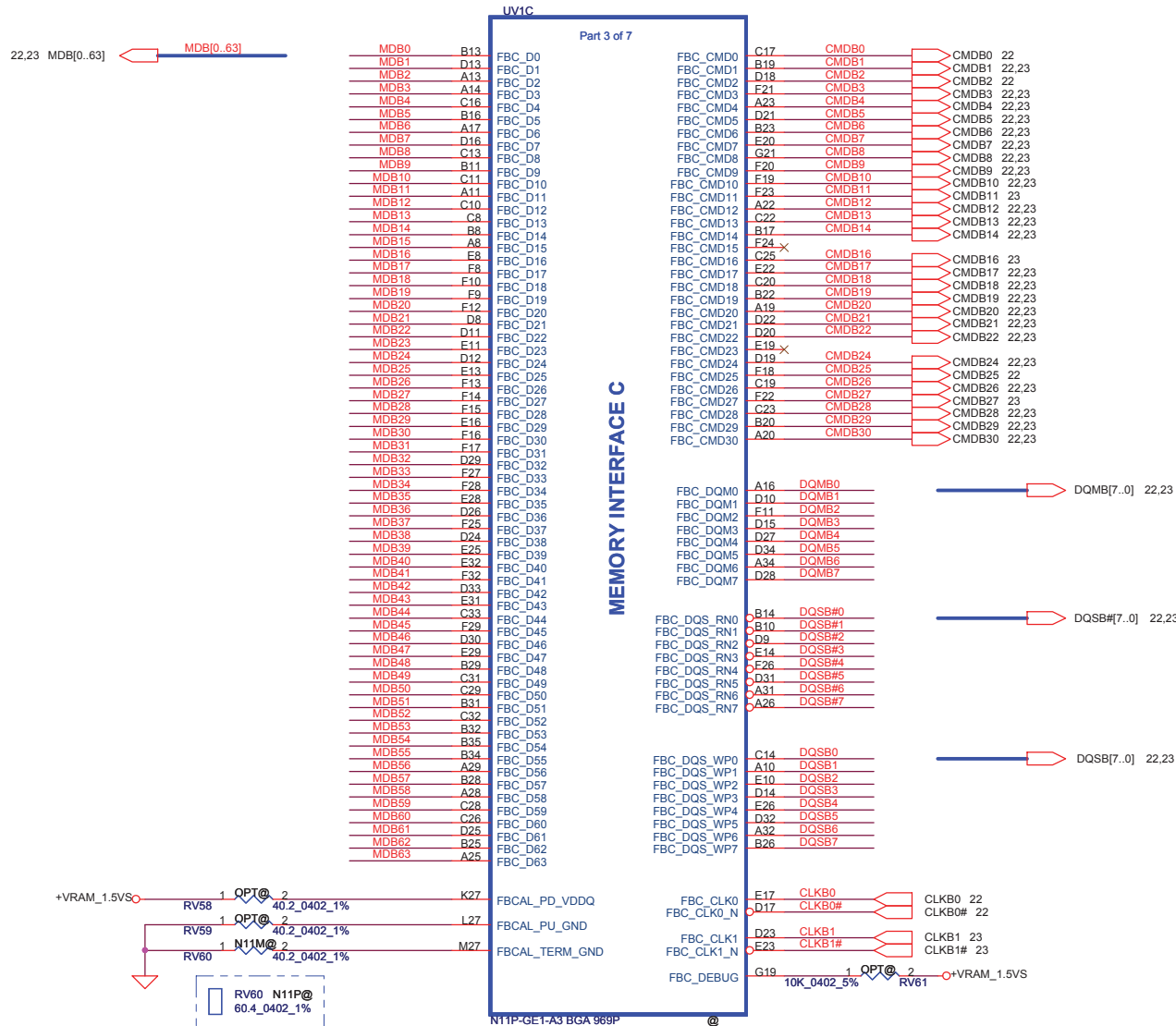
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Size	Document Number	NCL60/61 LA-6321P M/B		Rev	
Date	Wednesday, April 14, 2010	Sheet	16	of	59

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Size		Document Number		Rev	
NCL60/61		LA-6321P M/B		0.1	
Date		Wednesday, March 24, 2010		Sheet 17 of 59	



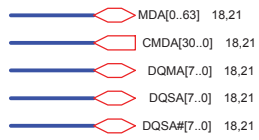
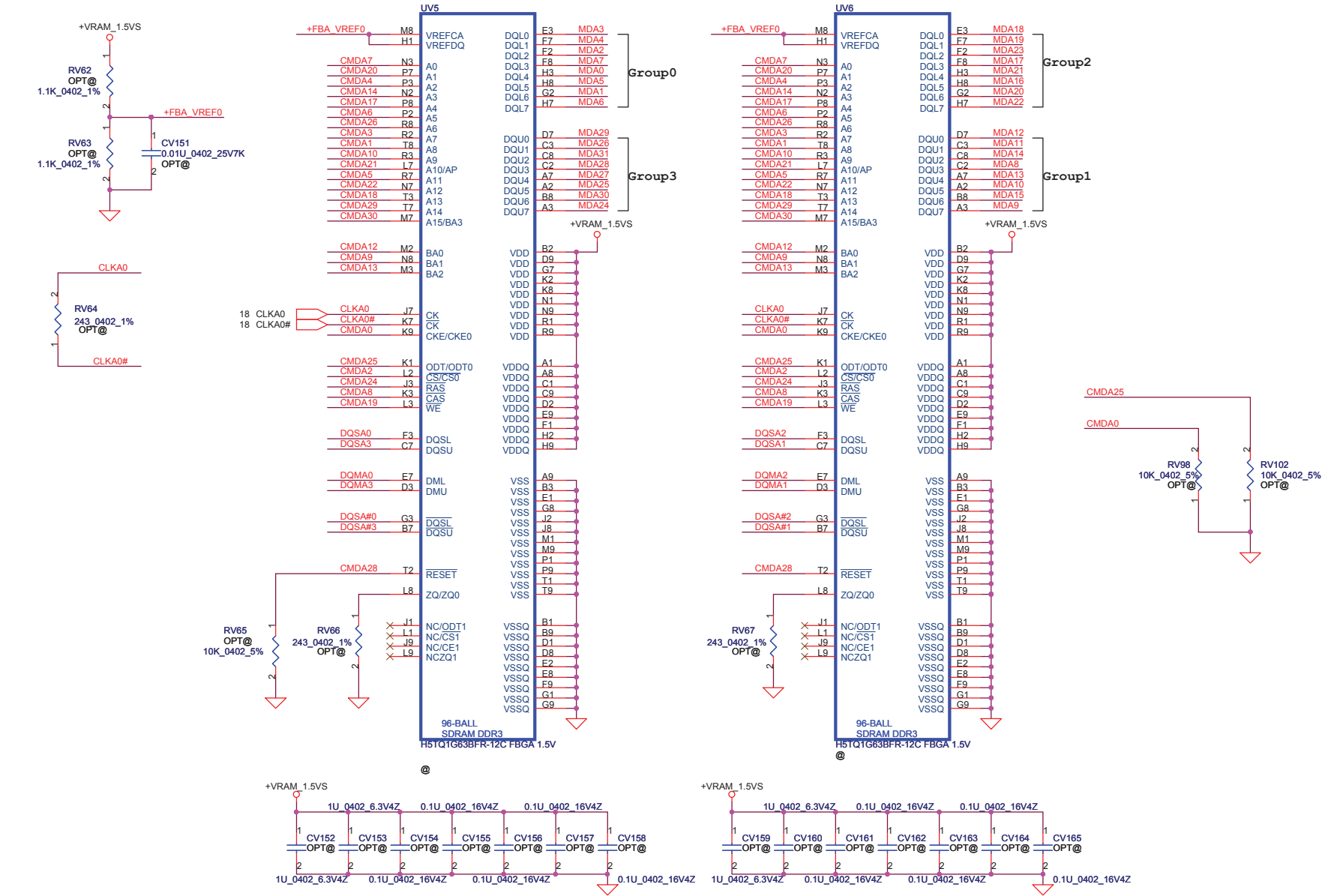


## Mode C - Mirror Mode Mapping

Address	DATA Bus	
	0..31	32..63
CMD0	CKE_L	
CMD1	A8	A8
CMD2	CS0#_L	
CMD3	A7	A6
CMD4	A2	A1
CMD5	A11	A9
CMD6	A5	A4
CMD7	A0	A12
CMD8	CAS#	CAS#
CMD9	BA1	A3
CMD10	A9	A11
CMD11		CS0#_H
CMD12	BA0	BA0
CMD13	BA2	A15
CMD14	A3	BA1
CMD15		CS1#_H
CMD16		ODT_H
CMD17	A4	A5
CMD18	A13	A14
CMD19	WE#	A10
CMD20	A1	A2
CMD21	A10	WE#
CMD22	A12	A0
CMD23	CS1#_L	
CMD24	RAS#	RAS#
CMD25	ODT_L	
CMD26	A6	A7
CMD27		CKE_H
CMD28	RST	RST
CMD29	A14	A13
CMD30	A15	BA2

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				Size	Document Number
				NCL60/61 LA-6321P M/B	
				Date:	Wednesday, April 14, 2010
				Sheet	19 of 59

Memory Partition A - Lower 32 bits



Mode C - Mirror Mode Mapping

DATA Bus		
Address	0..31	32..63
CMD0	CKE_L	
CMD1	A8	A8
CMD2	CS0#_L	
CMD3	A7	A6
CMD4	A2	A1
CMD5	A11	A9
CMD6	A5	A4
CMD7	A0	A12
CMD8	CAS#	CAS#
CMD9	BA1	A3
CMD10	A9	A11
CMD11		CS0#_H
CMD12	BA0	BA0
CMD13	BA2	A15
CMD14	A3	BA1
CMD15		CS1#_H
CMD16		ODT_H
CMD17	A4	A5
CMD18	A13	A14
CMD19	WE#	A10
CMD20	A1	A2
CMD21	A10	WE#
CMD22	A12	WE#
CMD23	CS1#_L	
CMD24	RAS#	RAS#
CMD25	ODT_L	
CMD26	A6	A7
CMD27		CKE_H
CMD28	RST	RST
CMD29	A14	A13
CMD30	A15	BA2

Security Classification

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VRAM A Lower

NCL60/61 LA-6321P M/B

Rev 0.1

Date:

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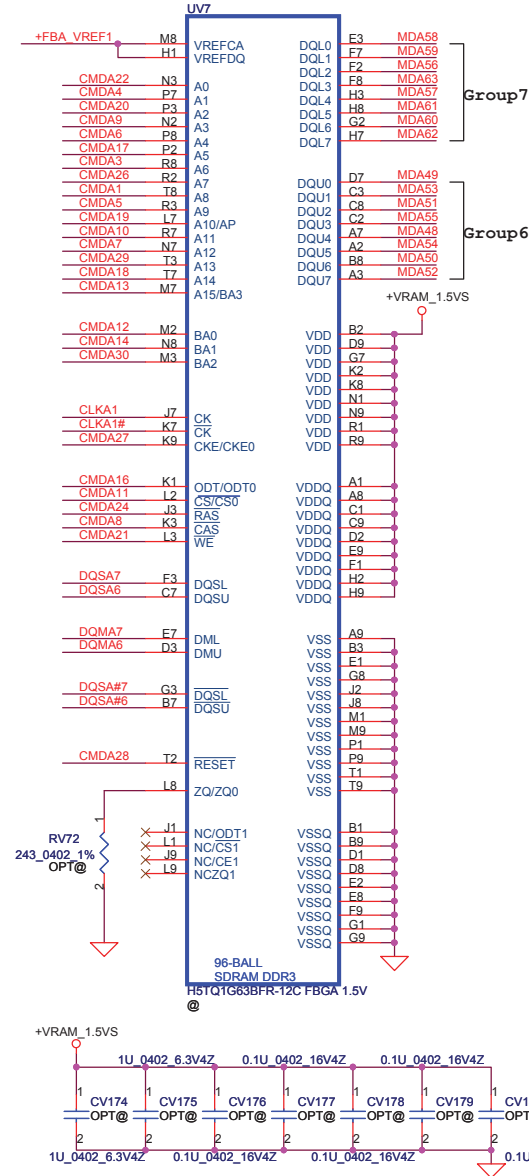
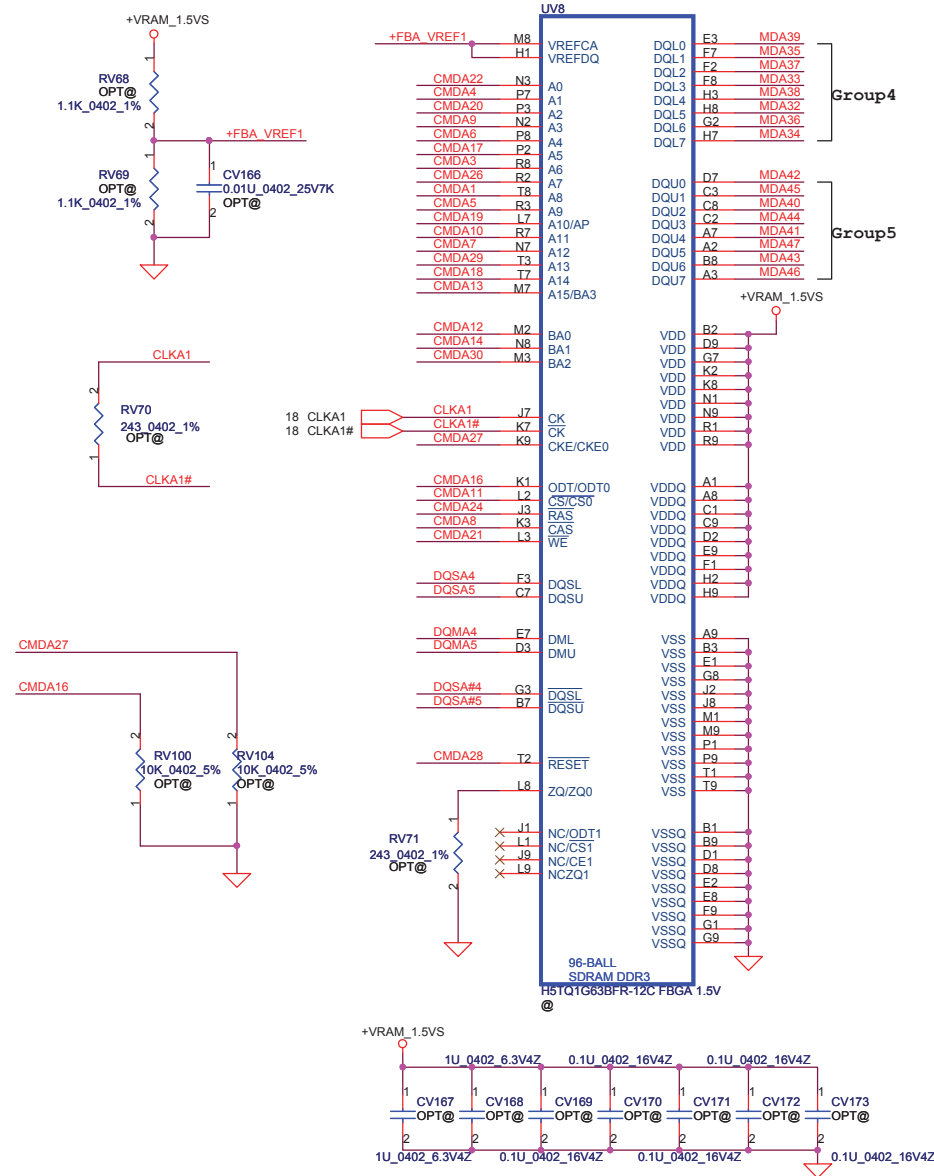
Sheet

20

of

59

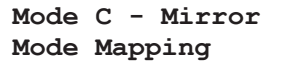
# Memory Partition A - Upper 32 bits



## Mode C - Mirror Mode Mapping

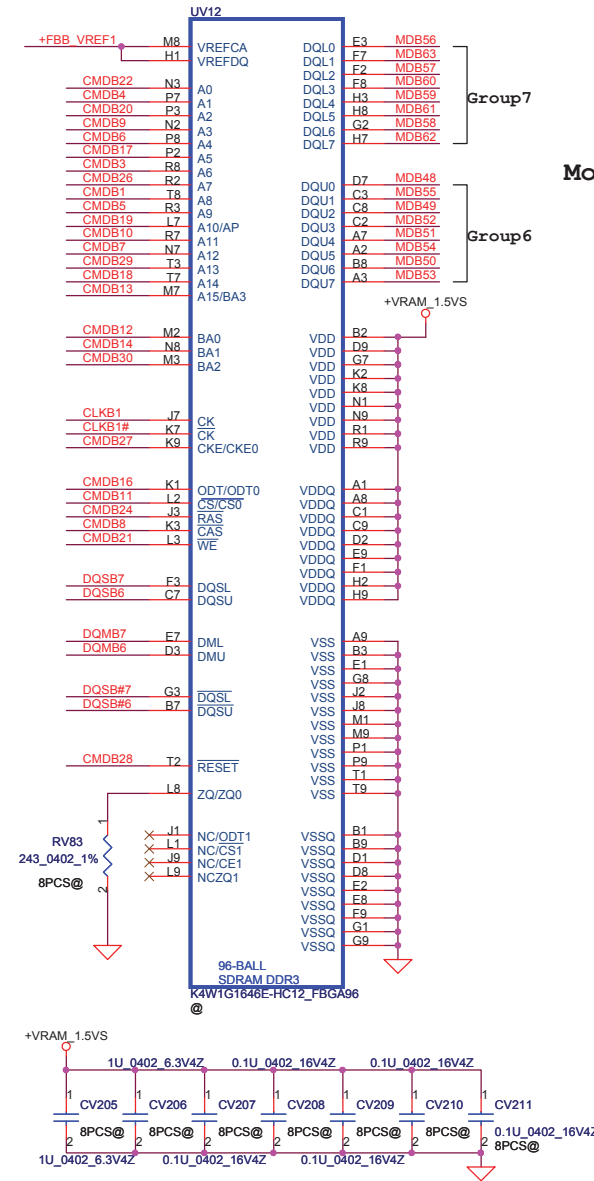
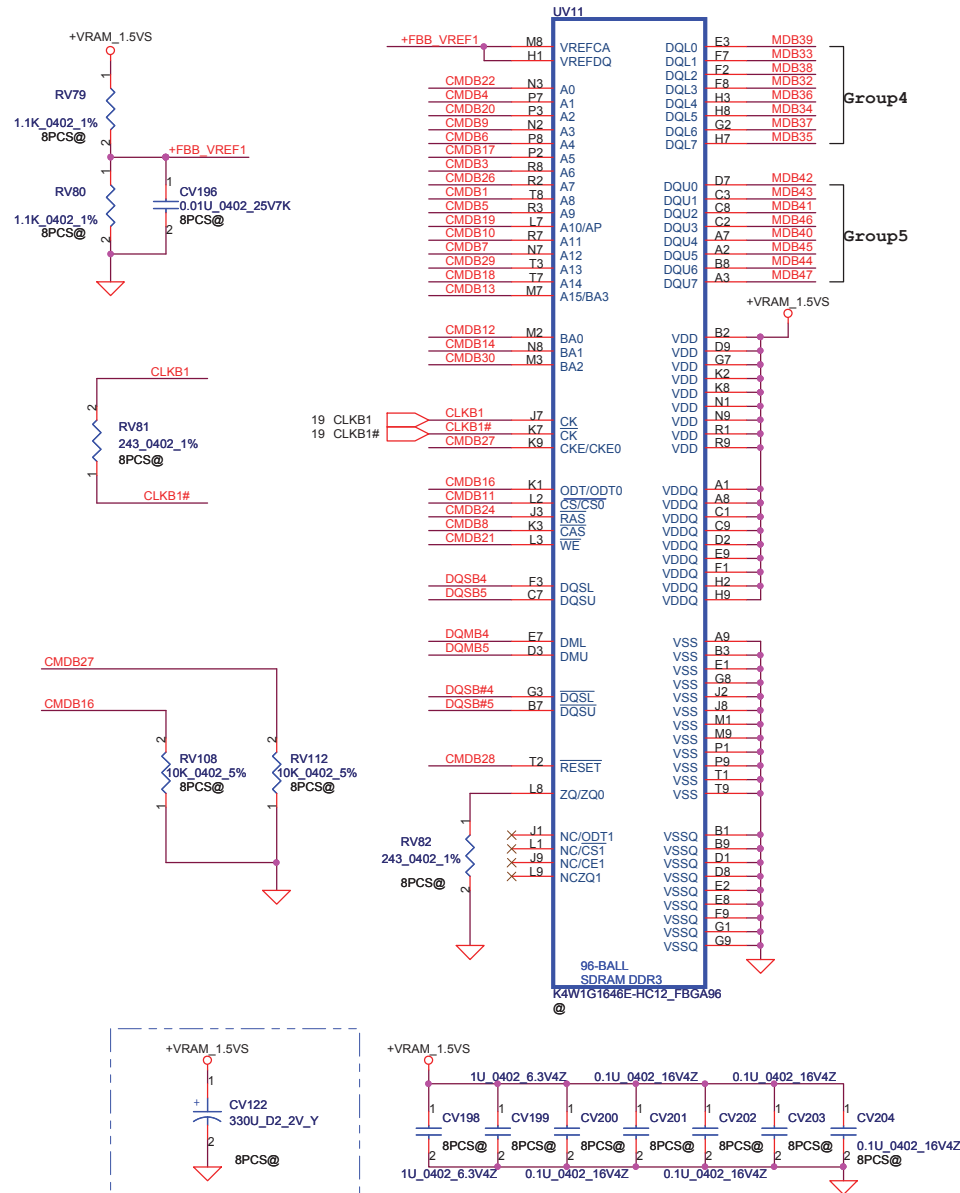
DATA Bus	
Address	0..31 32..63
CMD0	CKE_L
CMD1	A8
CMD2	CS0#_L
CMD3	A7
CMD4	A2
CMD5	A11
CMD6	A5
CMD7	A0
CMD8	CAS#
CMD9	BA1
CMD10	A9
CMD11	CS0#_H
CMD12	BA0
CMD13	BA2
CMD14	A3
CMD15	CS1#_H
CMD16	ODT_H
CMD17	A4
CMD18	A13
CMD19	WE#
CMD20	A1
CMD21	A10
CMD22	A12
CMD23	CS1#_L
CMD24	RAS#
CMD25	ODT_L
CMD26	A6
CMD27	CKE_H
CMD28	RST
CMD29	A14
CMD30	A15

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					NCL60/61 LA-6321P M/B	0.1
				Date:	Wednesday, April 14, 2010	Sheet 21 of 59

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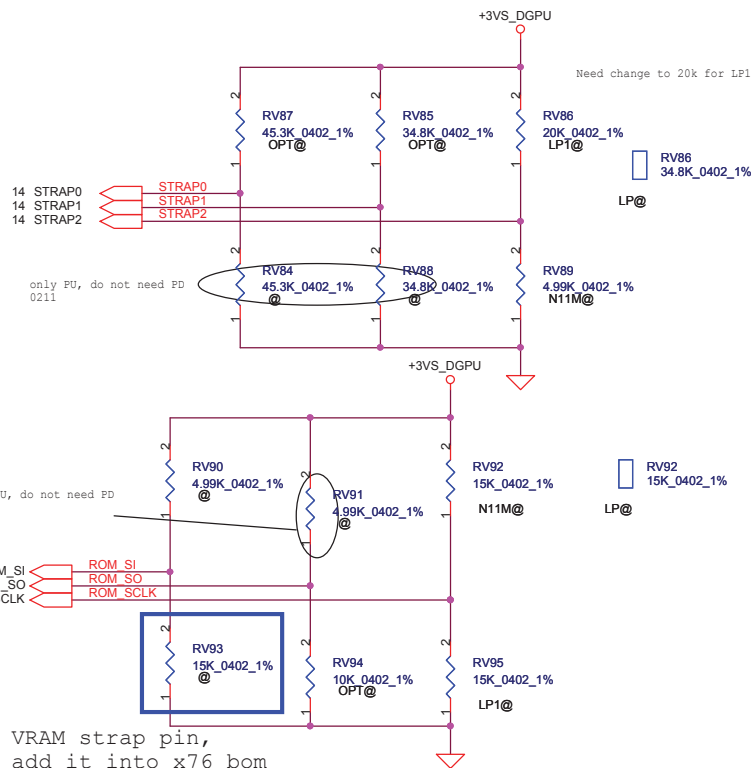
# Memory Partition C - Upper 32 bits



## Mode C - Mirror Mode Mapping

DATA Bus		
Address	0..31	32..63
CMD0	CKE_L	
CMD1	A8	A8
CMD2	CS0#_L	
CMD3	A7	A6
CMD4	A2	A1
CMD5	A11	A9
CMD6	A5	A4
CMD7	A0	A12
CMD8	CAS#	CAS#
CMD9	BA1	A3
CMD10	A9	A11
CMD11		CS0#_H
CMD12	BA0	BA0
CMD13	BA2	A15
CMD14	A3	BA1
CMD15		CS1#_H
CMD16		ODT_H
CMD17	A4	A5
CMD18	A13	A14
CMD19	WE#	A10
CMD20	A1	A2
CMD21	A10	WE#
CMD22	A12	A0
CMD23	CS1#_L	
CMD24	RAS#	RAS#
CMD25	ODT_L	
CMD26	A6	A7
CMD27		CKE_H
CMD28	RST	RST
CMD29	A14	A13
CMD30	A15	BA2

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						Custom	NCL60/61 LA-6321P M/B	0.1
						Date:	Wednesday, April 14, 2010	Sheet 23 of 59



Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS_DGPU	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS_DGPU	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLEN_TERM
ROM_SI	+3VS_DGPU	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	+3VS_DGPU	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	+3VS_DGPU	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	+3VS_DGPU	USER[3]	USER[2]	USER[1]	USER[0]

Resistor Values	Pull-up to +3VS	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

VGA power up sequence



	DeviceID	ROM_SCLK	STRAP2
N11M-GE2		Pull up 15K	Pull down 5K
N11P-LP1		Pull down 15K	Pull up 20K
N11P-LP		TBD	TBD

SUB_VENDOR		XCLK 417	
0	No VBIOS ROM (Default)	0	277MHz (Default)
1	BIOS ROM is present	1	Reserved

FB_0_BAR_SIZE		USER Straps	
0	256MB (Default)	User[3:0]	
1	Reserved	1000-1100	Customer defined

3GIO_PADCFG		PEX_PLL_EN_TERM	
3GIO_PADCFG[3:0]		0	Disable (Default)
1110	Notebook Default	1	Enable

SLOT_CLOCK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SMBUS_ALT_ADDR		VGA_DEVICE	
0	0x9E (Default)	0	3D Device
1	0x9C (Multi-GPU usage)	1	VGA Device (Default)

## ROM SI

Hynix	512M	SA000032400 64MX16 H5TQ1G63BFR-12C	PD 15K
	1G	SA00003VS00 128MX16 H5TQ2G63BFR	PD 35K
Samsung	512M	SA000035700 64Mx16 K4W1G1646E-HC12	PD 20K
	1G	SA00003MQ00 128M16 K4W2G1646B-HC12	PD 45K

## ROM\_SCLK

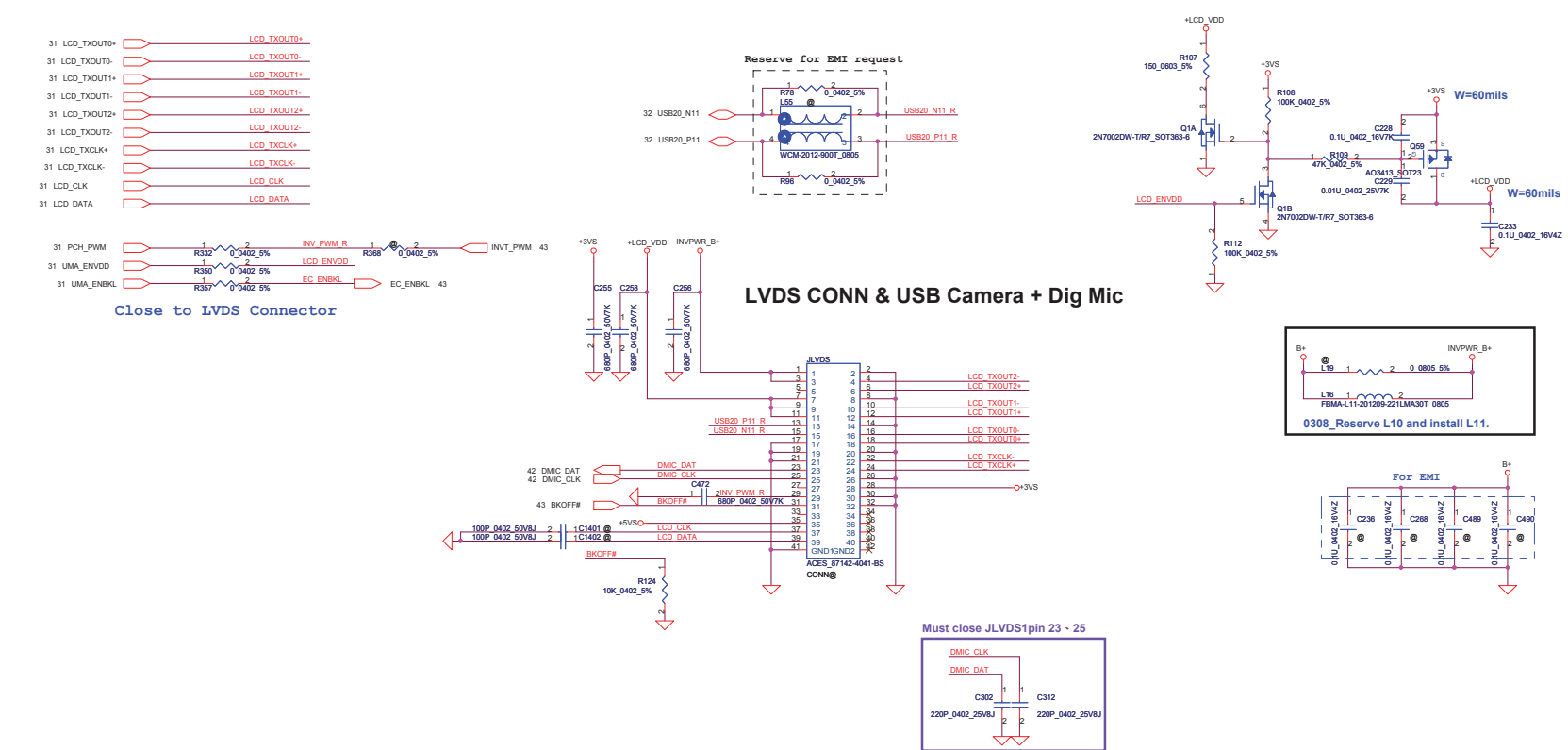
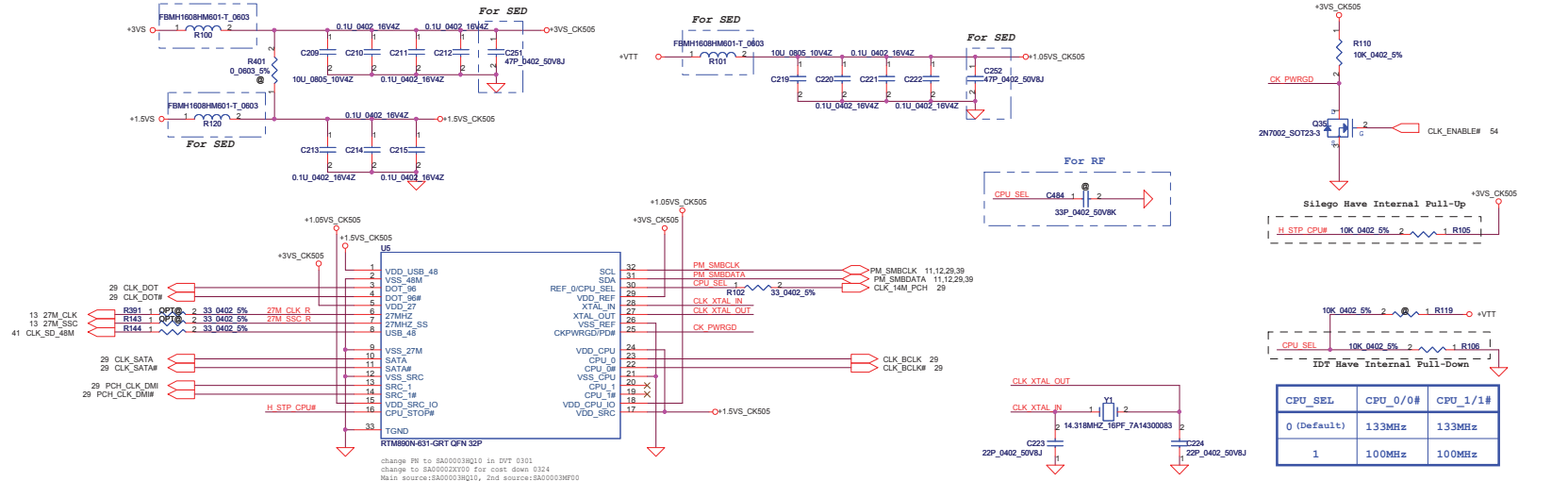
N11M GE2	PU 15K
N11P LP1	PD 15K
N11P LP	PU 15K

## STRAP2

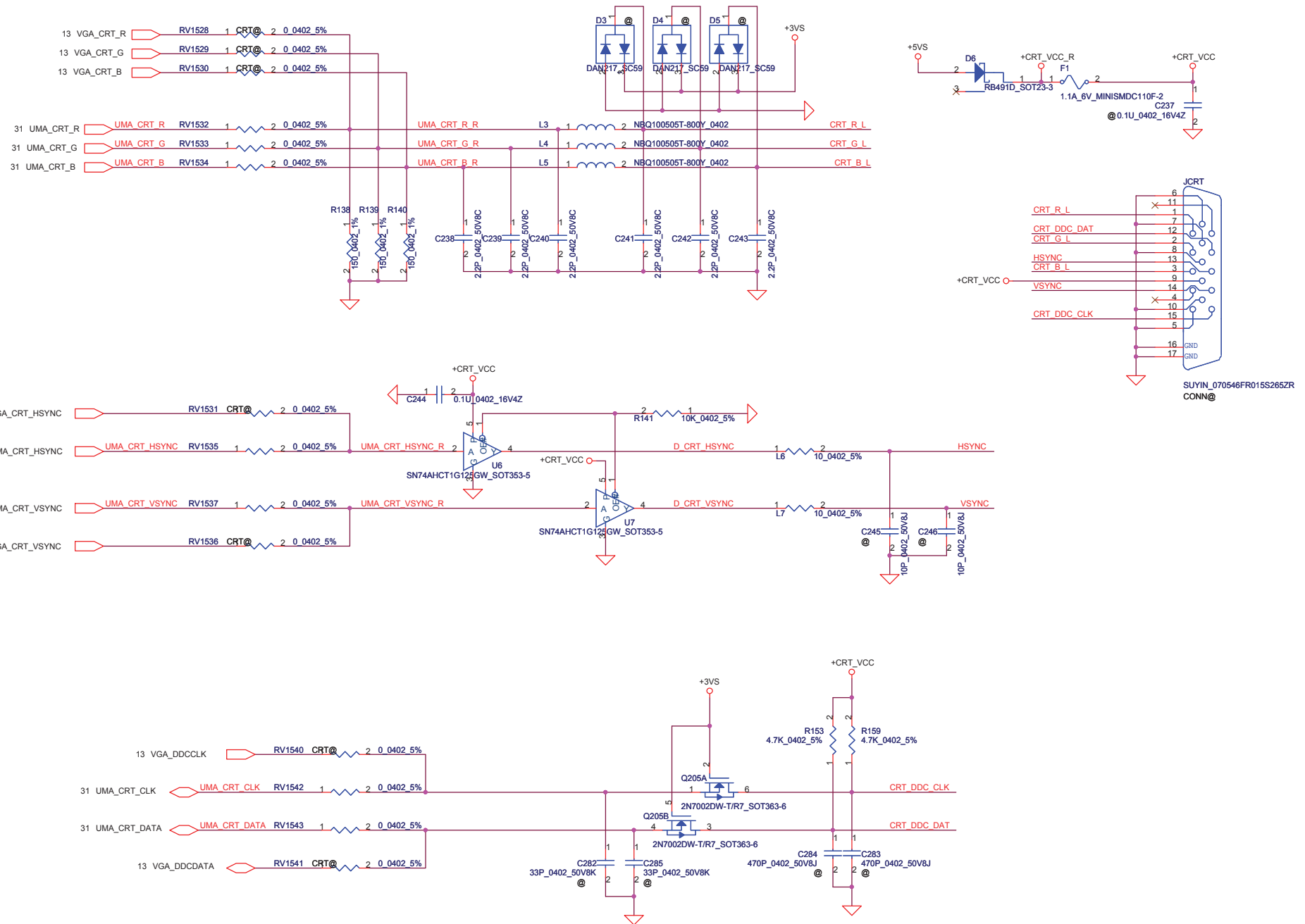
N11M GE2	PD 5K
N11P LP1	PU 20K
N11P LP	PU 35K

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				NCL60/61 LA-6321P M/B			0.1
				Date:	Wednesday, April 14, 2010	Sheet	24 of 59

## Clock Generator

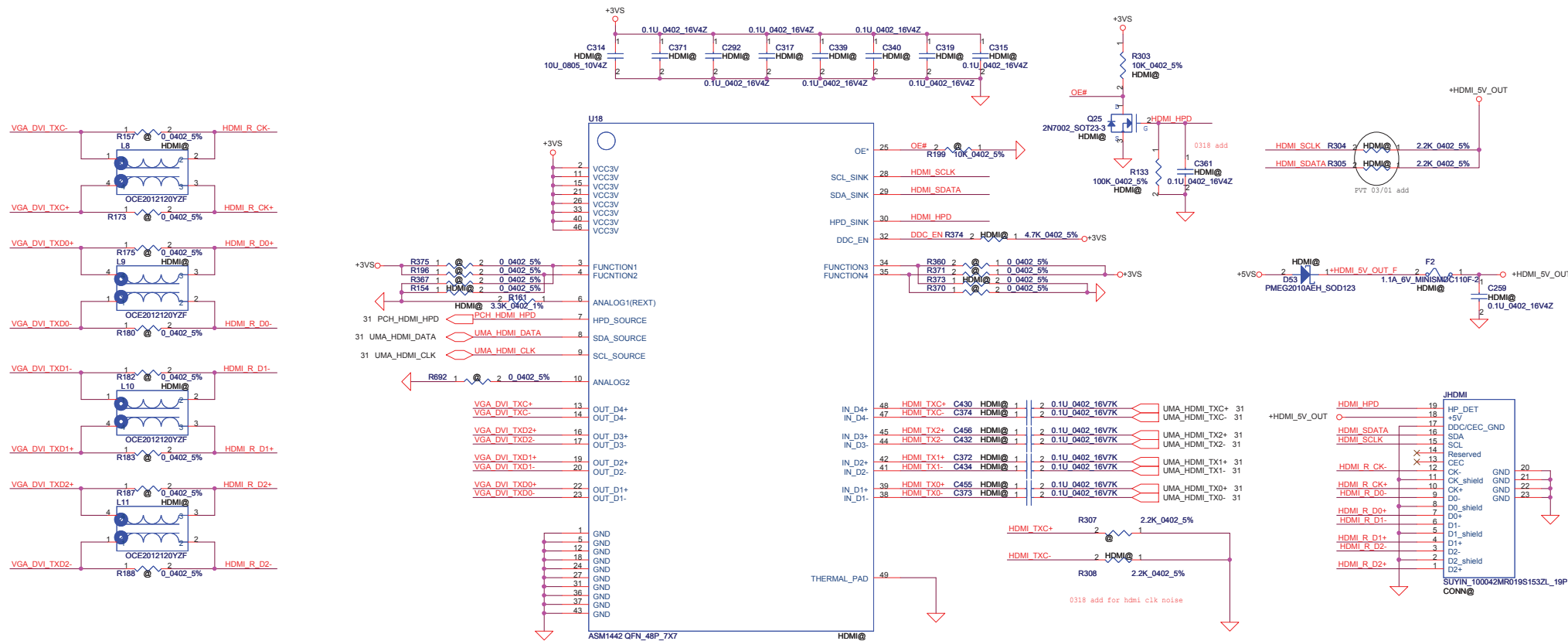


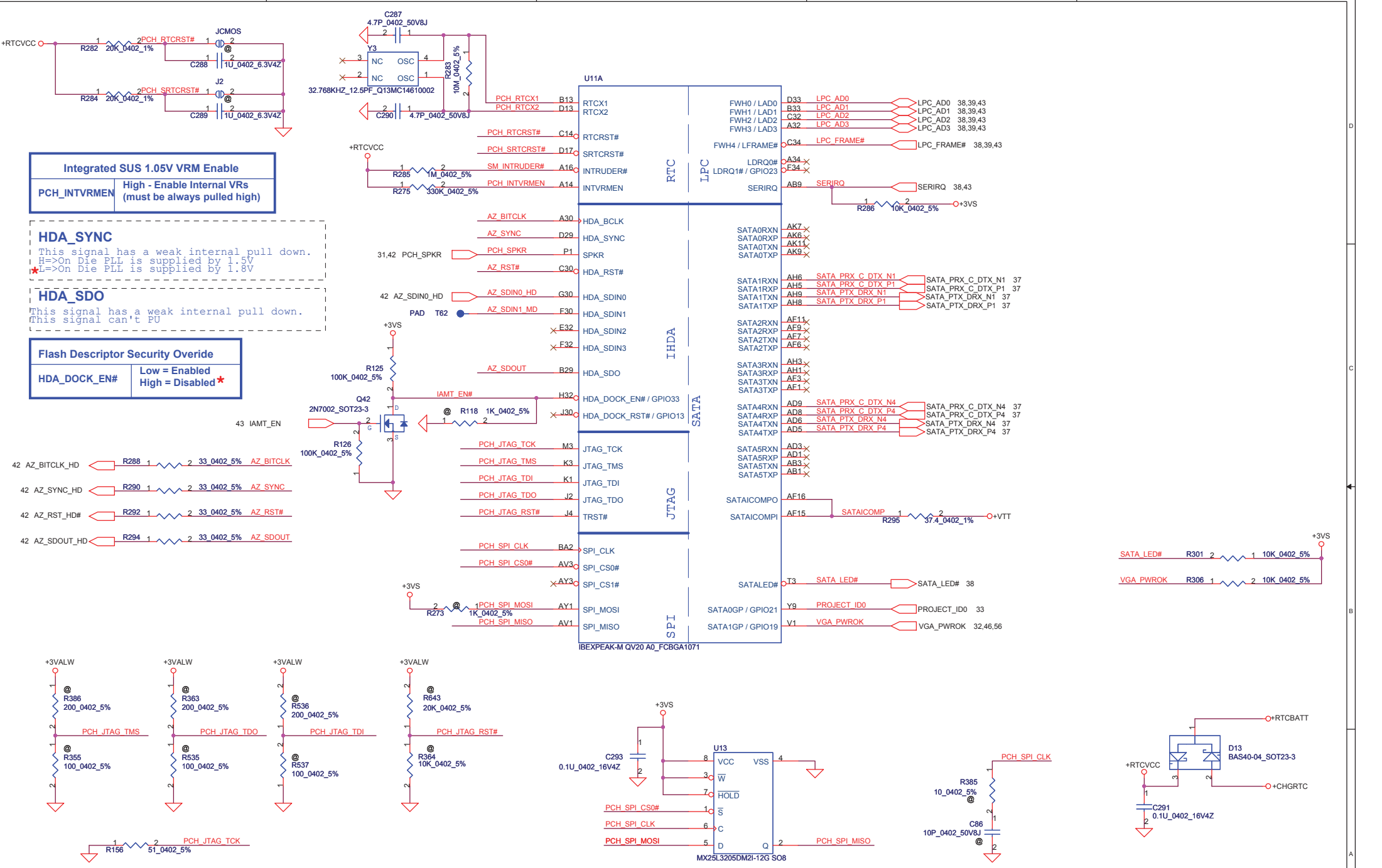
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Sheet Number	Drawing Number		Rev	
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Date	Thursday, 2010/1/23		Date	
	Thursday, 2010/1/23		Date	



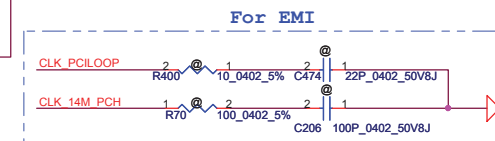
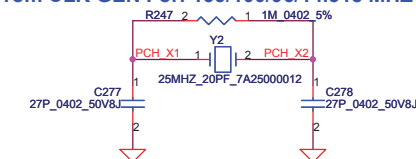
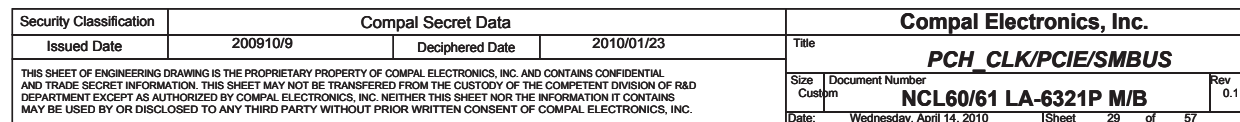
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										CRT	
										NCL60/61 LA-6321P M/B	
										Rev 0.1	
										Date: Wednesday, April 14, 2010	
										Sheet 26 of 57	

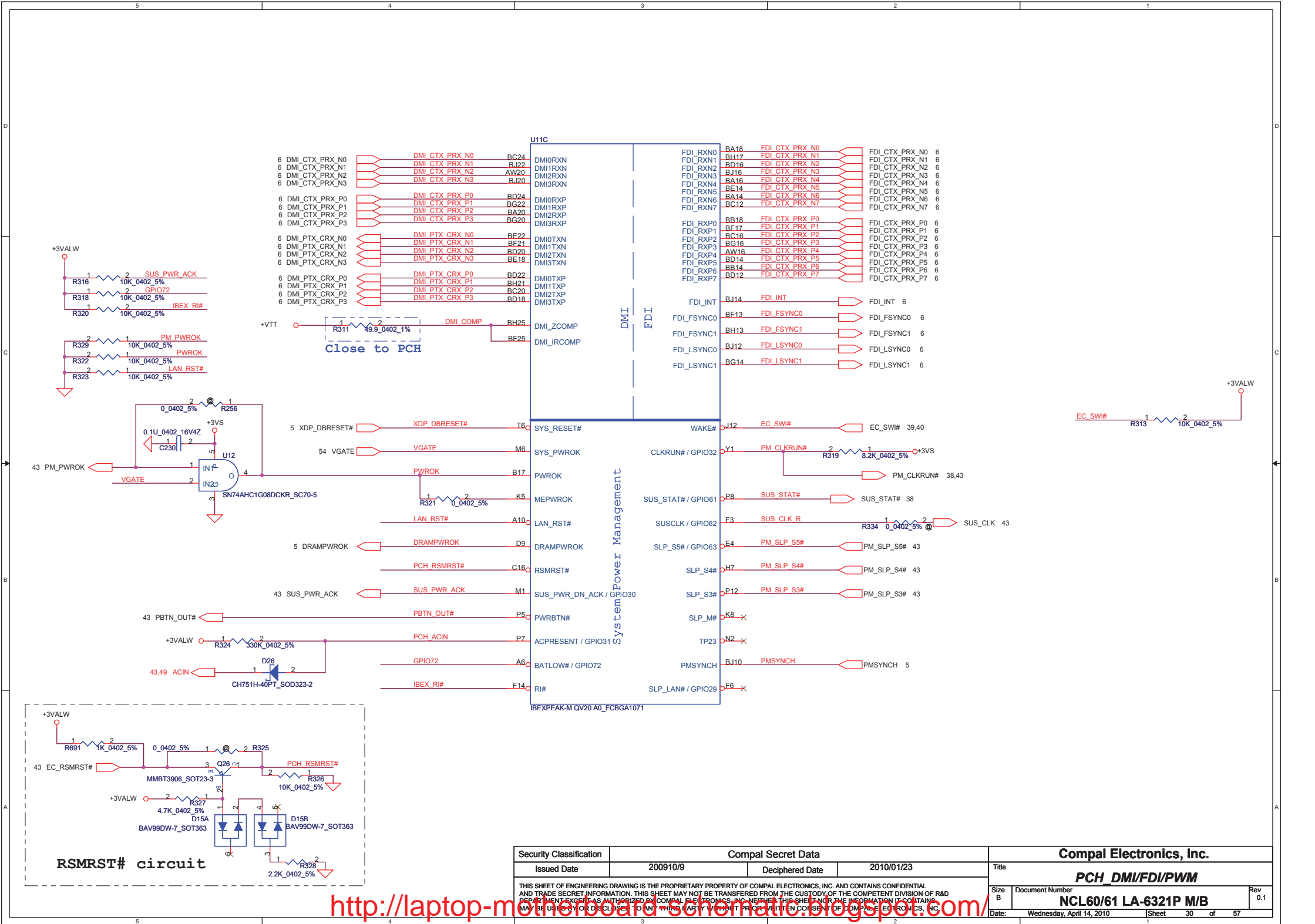
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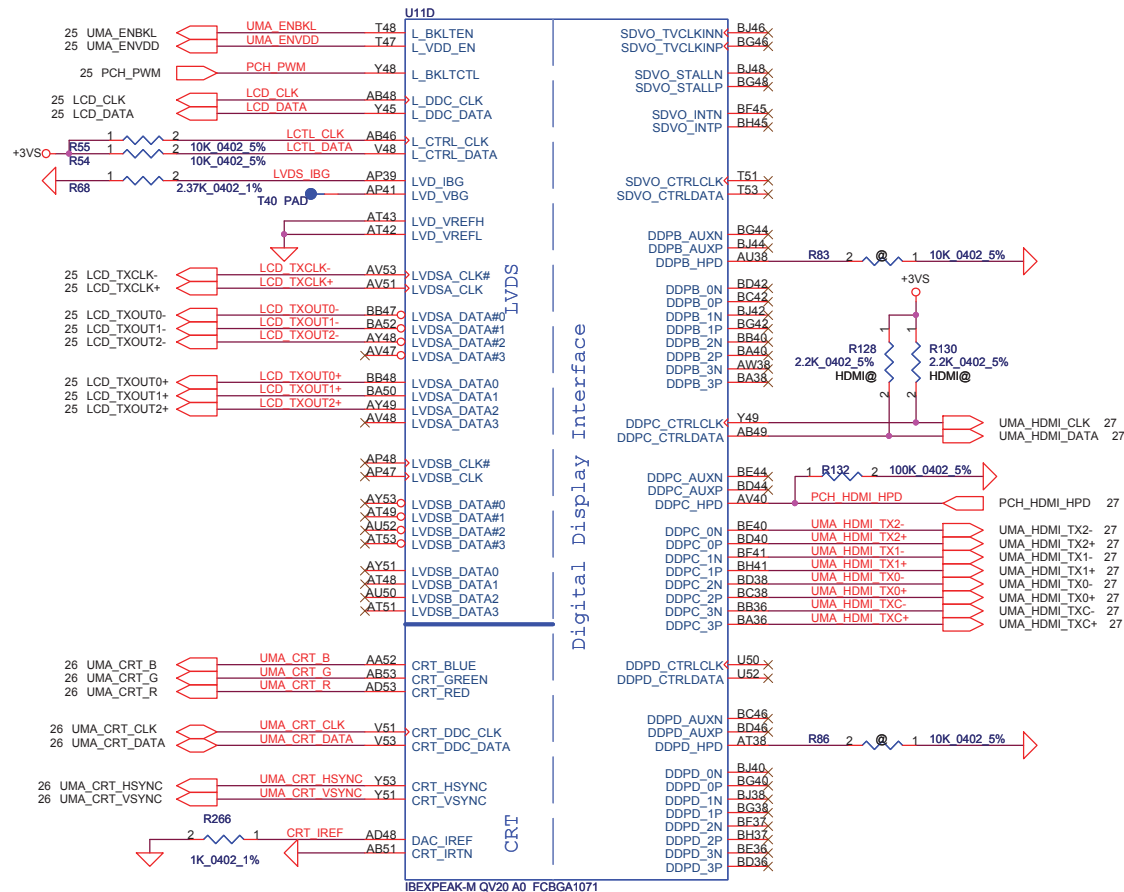
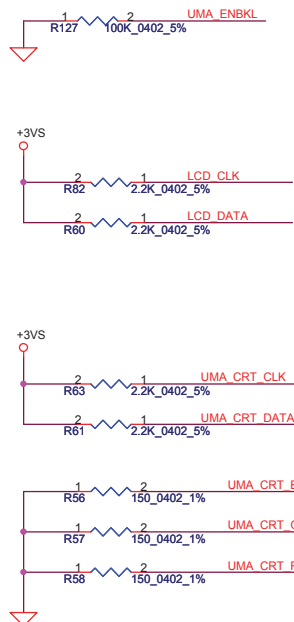




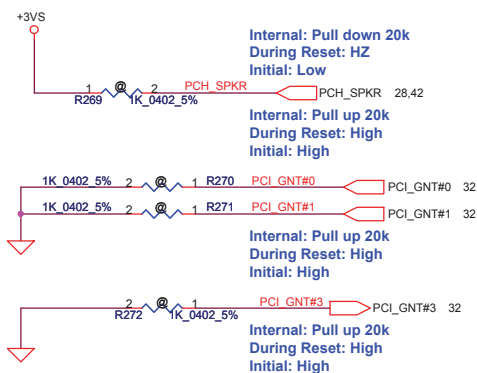
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				NCL60/61 LA-6321P M/B	
				Rev	0.1
Date: Wednesday, April 14, 2010		Sheet 28 of 57			







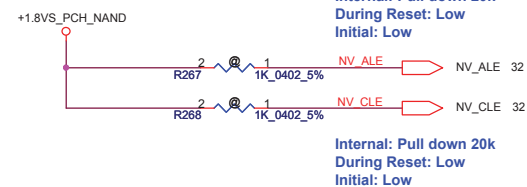
## PCH Strap Pin



NO REBOOT Strap	
PCH_SPKR	Low= Disable High= Enable

Boot BIOS Strap		
PCI_GNT#1	PCI_GNT#0	Boot BIOS Location
0	0	LPC (Default)
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= A16 swap override Disable



Danbury Technology Enabled	
NV_ALE	High = Enabled Low = Disabled (Default)

DMI Termination Voltage	
NV_CLE	Low= Set to Vss (Default) High= Set to Vcc

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				Size	Document Number	Rev	
				Custom	NCL60/61 LA-6321P M/B	0.1	
				Date:	Wednesday, April 14, 2010	Sheet 31 of 57	



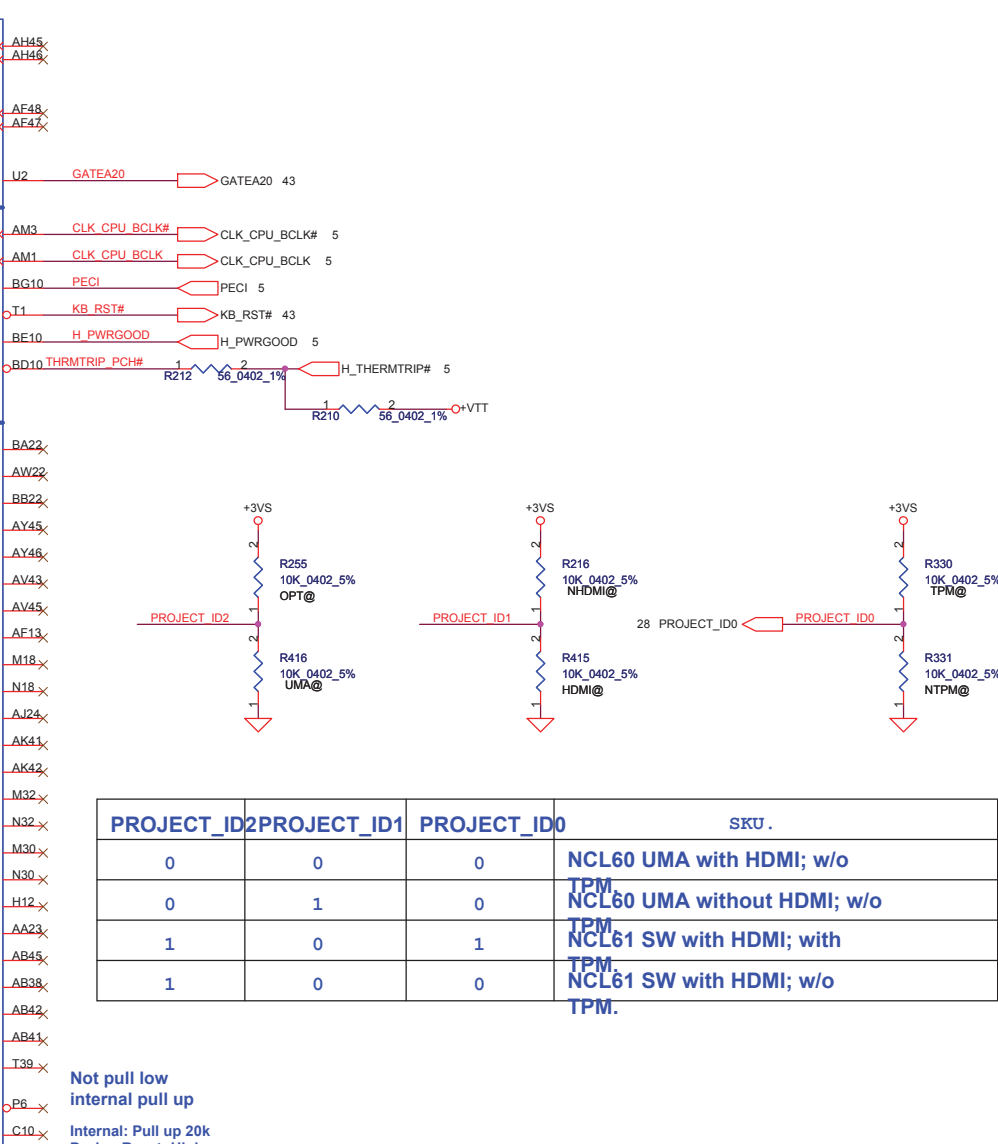
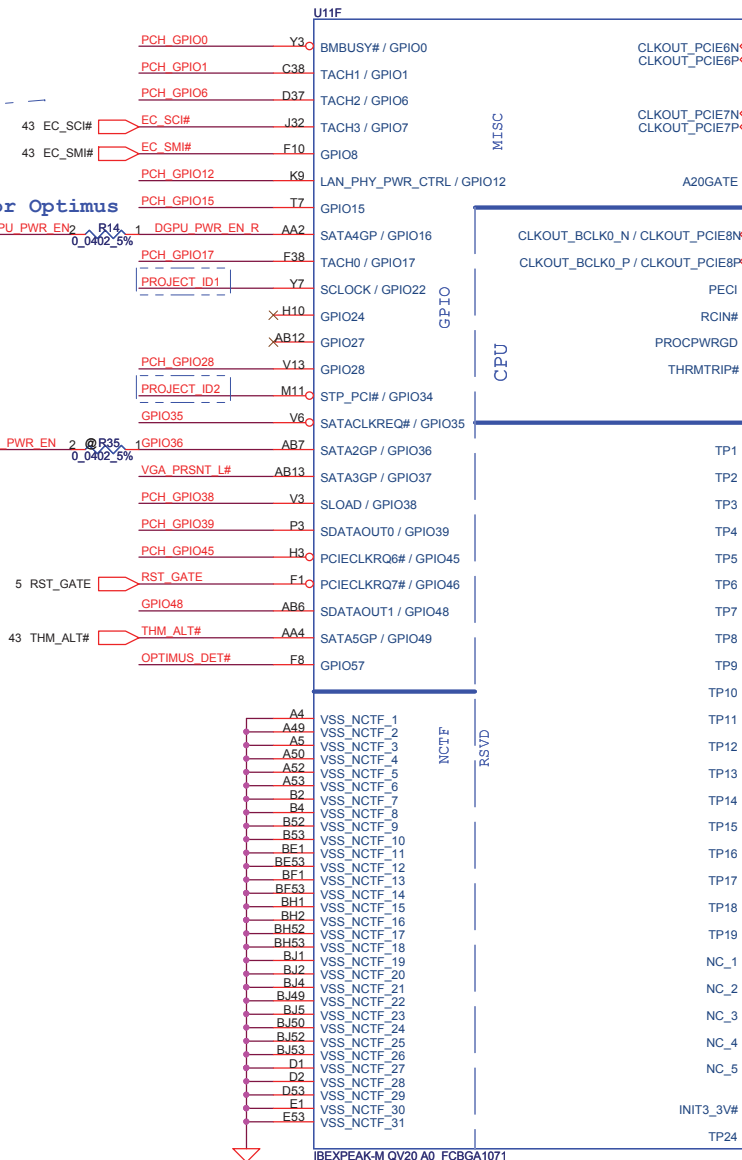
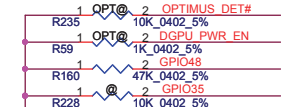
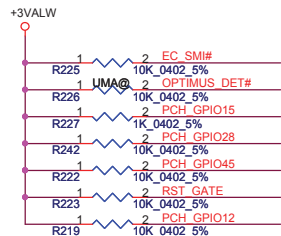
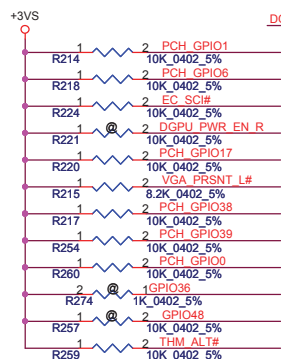
GPIO8  
Not pull down  
Internal: Pull up 20k  
During Reset: High  
Initial: High

GPIO15  
a Strong pull up may be needed  
for GPIO Functionality  
Internal: Pull-down 20k  
During Reset: Low  
Initial: Low

For Optimus

#### On-Die PLL VR

PCH\_GPIO27 High = Enabled (Default)  
Low = Disabled



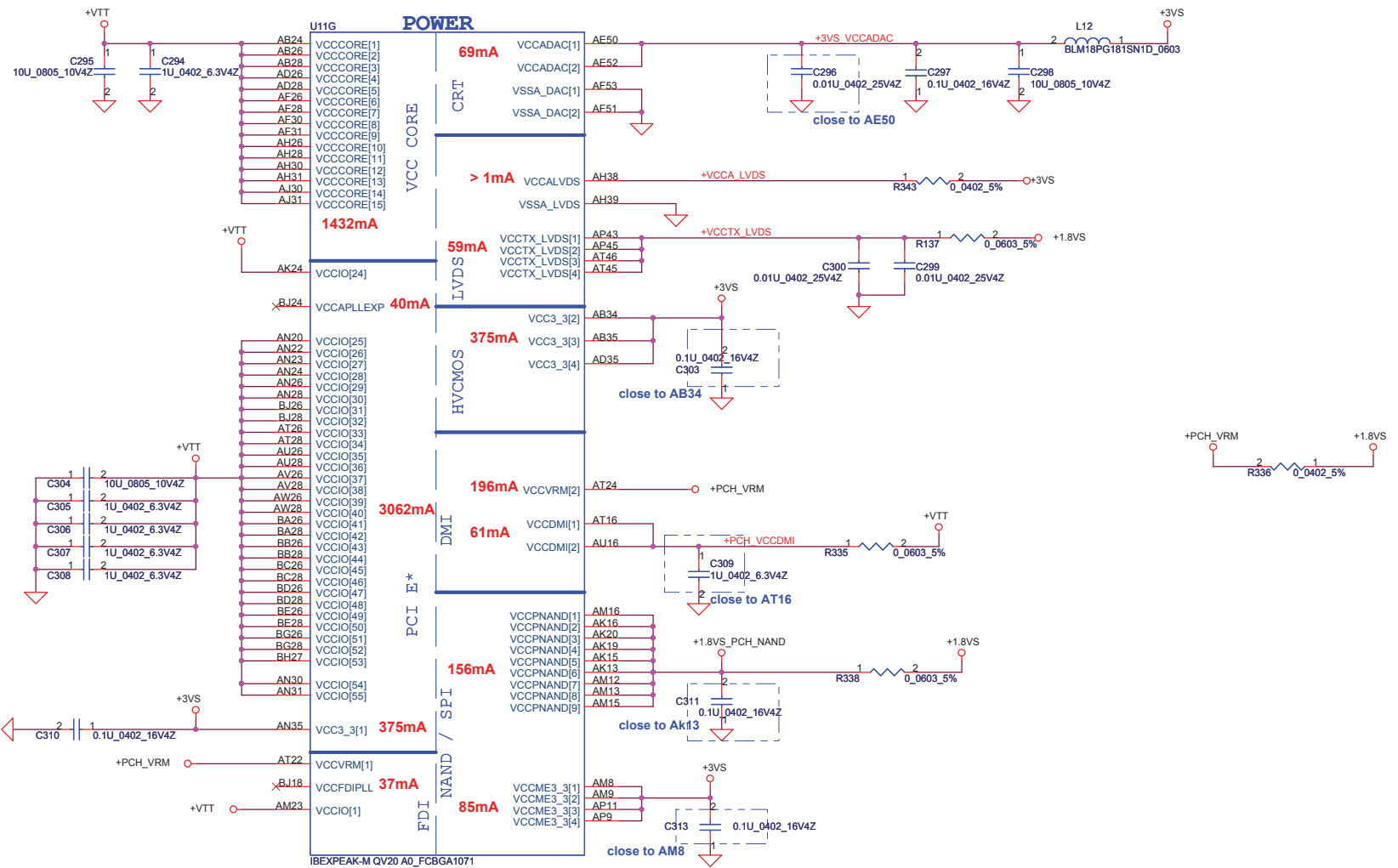
PROJECT_ID2	PROJECT_ID1	PROJECT_ID0	SKU
0	0	0	NCL60 UMA with HDMI; w/o TPM
0	1	0	NCL60 UMA without HDMI; w/o TPM
1	0	1	NCL61 SW with HDMI; with TPM
1	0	0	NCL61 SW with HDMI; w/o TPM

Not pull low  
internal pull up  
Internal: Pull up 20k  
During Reset: High  
Initial: High

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				Size B	Document Number	NCL60/61 LA-6321P M/B		Rev 0.1
				Date:	Wednesday, April 14, 2010	Sheet	33	of

<http://laptop-motherboard.schematic.org/spm.com/>





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				NCL60/61 LA-6321P M/B	
				Date:	Wednesday, March 24, 2010
				Sheet	35 of 57
				Rev	0.1

<http://laptop-motherboard-schematic.blogspot.com/>

AY7	VSS[159]	H49
B11	VSS[160]	H5
B15	VSS[161]	J24
B19	VSS[162]	K11
B23	VSS[163]	K43
B31	VSS[164]	K47
B35	VSS[165]	K7
B39	VSS[166]	L14
B43	VSS[167]	L18
B47	VSS[168]	L2
B7	VSS[169]	L22
BG12	VSS[170]	L32
BB12	VSS[171]	L36
BB16	VSS[172]	L40
BB20	VSS[173]	L52
BB24	VSS[174]	M12
BB30	VSS[175]	M16
BB34	VSS[176]	M20
BB38	VSS[177]	M38
BB42	VSS[178]	M34
BB46	VSS[179]	M38
BB5	VSS[180]	M42
BC10	VSS[181]	M46
BC14	VSS[182]	M49
BC18	VSS[183]	M5
BC2	VSS[184]	M8
BC22	VSS[185]	N24
BC32	VSS[186]	P11
BC36	VSS[187]	AD15
BC40	VSS[188]	P22
BC44	VSS[189]	P30
BC52	VSS[190]	P32
BH9	VSS[191]	P34
BD48	VSS[192]	P42
BD49	VSS[193]	P45
BD5	VSS[194]	P47
BE12	VSS[195]	R2
BE16	VSS[196]	R52
BE20	VSS[197]	T12
BE24	VSS[198]	T41
BE30	VSS[199]	T46
BE34	VSS[200]	T49
BE38	VSS[201]	T5
BE42	VSS[202]	T8
BE46	VSS[203]	U30
BE48	VSS[204]	U31
BE50	VSS[205]	U32
BE6	VSS[206]	U34
BE8	VSS[207]	U38
BF3	VSS[208]	V11
BF49	VSS[209]	P16
BF51	VSS[210]	V19
BG18	VSS[211]	V20
BG24	VSS[212]	V22
BG4	VSS[213]	V30
BG50	VSS[214]	V31
BH11	VSS[215]	V32
BH15	VSS[216]	V34
BH19	VSS[217]	V35
BH23	VSS[218]	V38
BH31	VSS[219]	V43
BH35	VSS[220]	V45
BH39	VSS[221]	V46
BH43	VSS[222]	V47
BH47	VSS[223]	V49
BH7	VSS[224]	V5
C12	VSS[225]	V7
C50	VSS[226]	V8
D51	VSS[227]	W2
E12	VSS[228]	W52
E16	VSS[229]	Y11
E20	VSS[230]	Y12
E24	VSS[231]	Y15
E30	VSS[232]	Y19
E34	VSS[233]	Y23
E38	VSS[234]	Y28
E42	VSS[235]	Y30
E46	VSS[236]	Y31
E48	VSS[237]	Y32
E6	VSS[238]	Y38
E8	VSS[239]	Y43
F49	VSS[240]	Y46
F5	VSS[241]	P49
G10	VSS[242]	Y5
G14	VSS[243]	Y6
G18	VSS[244]	Y8
G2	VSS[245]	P24
G22	VSS[246]	T43
G32	VSS[247]	AD51
G36	VSS[248]	AT8
G40	VSS[249]	AD47
G44	VSS[250]	Y47
G52	VSS[251]	AT12
AF39	VSS[252]	AM6
H16	VSS[253]	AT13
H20	VSS[254]	AM5
H30	VSS[255]	AK45
H34	VSS[256]	AK39
H38	VSS[257]	AV14
H42	VSS[258]	

IBEXPEAK-M QV20 A0\_FCBGA1071

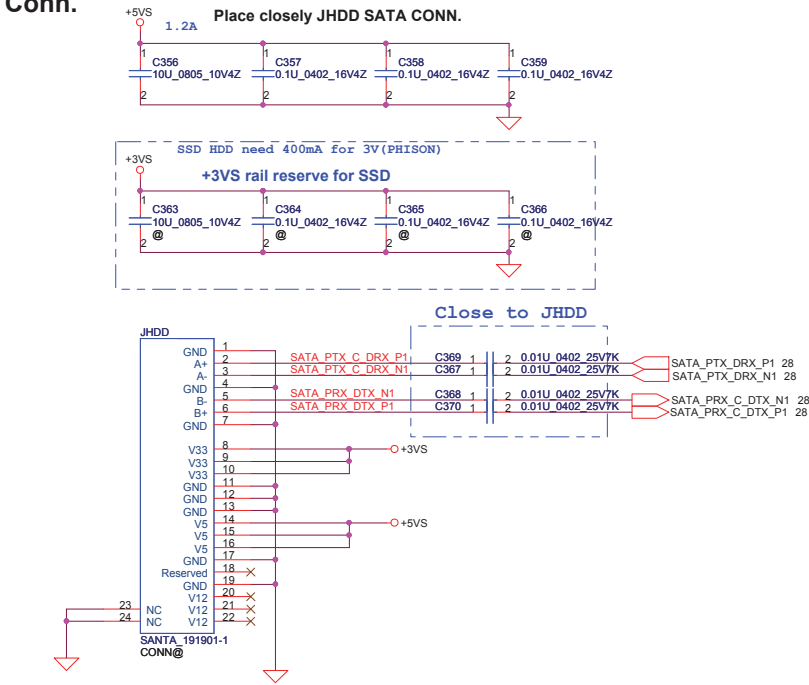
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AA19	VSS[1]	VSS[80]
AA20	VSS[2]	VSS[81]
AA22	VSS[3]	VSS[82]
AM19	VSS[4]	VSS[83]
AA24	VSS[5]	VSS[84]
AA26	VSS[6]	VSS[85]
AA28	VSS[7]	VSS[86]
AA30	VSS[8]	VSS[87]
AA31	VSS[9]	VSS[88]
AA32	VSS[10]	VSS[89]
AB11	VSS[11]	VSS[90]
AB15	VSS[12]	VSS[91]
AB23	VSS[13]	VSS[92]
AB30	VSS[14]	VSS[93]
AB31	VSS[15]	VSS[94]
AB32	VSS[16]	VSS[95]
AB39	VSS[17]	VSS[96]
AB43	VSS[18]	VSS[97]
AB47	VSS[19]	VSS[98]
AB5	VSS[20]	VSS[99]
AB8	VSS[21]	VSS[100]
AC2	VSS[22]	VSS[101]
AC52	VSS[23]	VSS[102]
AD11	VSS[24]	VSS[103]
AD12	VSS[25]	VSS[104]
AD16	VSS[26]	VSS[105]
AD23	VSS[27]	VSS[106]
AD30	VSS[28]	VSS[107]
AD31	VSS[29]	VSS[108]
AD32	VSS[30]	VSS[109]
AD34	VSS[31]	VSS[110]
AU22	VSS[32]	VSS[111]
AD42	VSS[33]	VSS[112]
AD46	VSS[34]	VSS[113]
AD49	VSS[35]	VSS[114]
AD7	VSS[36]	VSS[115]
AE2	VSS[37]	VSS[116]
AE4	VSS[38]	VSS[117]
AF12	VSS[39]	VSS[118]
Y13	VSS[40]	VSS[119]
AH49	VSS[41]	VSS[120]
AU4	VSS[42]	VSS[121]
AF35	VSS[43]	VSS[122]
AP13	VSS[44]	VSS[123]
AN34	VSS[45]	VSS[124]
AF45	VSS[46]	VSS[125]
AF46	VSS[47]	VSS[126]
AF49	VSS[48]	VSS[127]
AF5	VSS[49]	VSS[128]
AG2	VSS[50]	VSS[129]
AG52	VSS[51]	VSS[130]
AH11	VSS[52]	VSS[131]
AH15	VSS[53]	VSS[132]
AH16	VSS[54]	VSS[133]
AH24	VSS[55]	VSS[134]
AH32	VSS[56]	VSS[135]
AV18	VSS[57]	VSS[136]
VSS[58]	VSS[58]	VSS[137]
AH43	VSS[59]	VSS[138]
AH47	VSS[60]	VSS[139]
AH7	VSS[61]	VSS[140]
AJ19	VSS[62]	VSS[141]
AJ2	VSS[63]	VSS[142]
AJ20	VSS[64]	VSS[143]
AJ22	VSS[65]	VSS[144]
AJ23	VSS[66]	VSS[145]
AJ26	VSS[67]	VSS[146]
AJ28	VSS[68]	VSS[147]
AJ32	VSS[69]	VSS[148]
AJ34	VSS[70]	VSS[149]
AT5	VSS[71]	VSS[150]
AJ4	VSS[72]	VSS[151]
AK12	VSS[73]	VSS[152]
AM41	VSS[74]	VSS[153]
AN19	VSS[75]	VSS[154]
AK26	VSS[76]	VSS[155]
AK22	VSS[77]	VSS[156]
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AK28	VSS[79]	VSS[158]

IBEXPEAK-M QV20 A0\_FCBGA1071

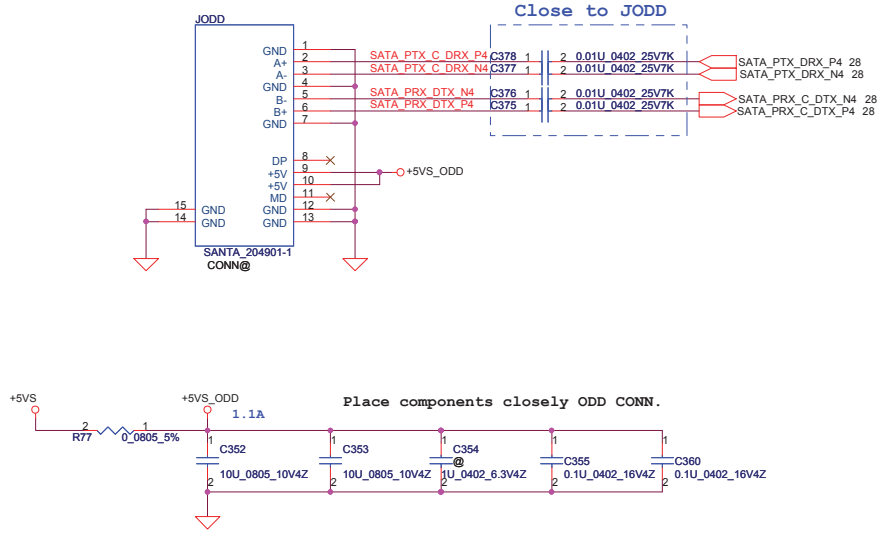
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Date:	Wednesday, March 24, 2010	Sheet	36	of	57

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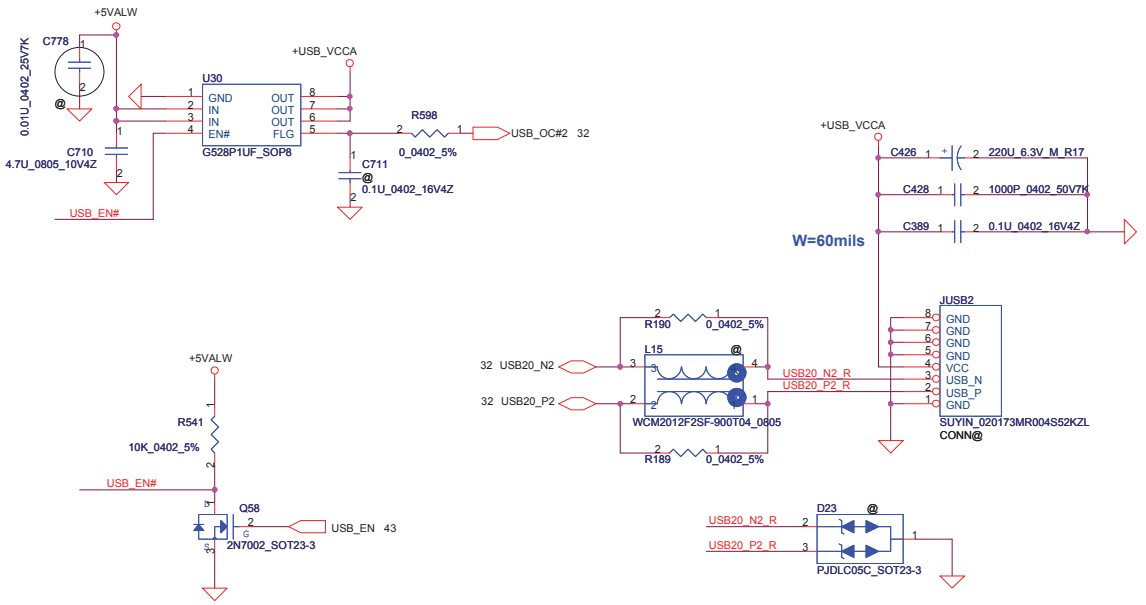
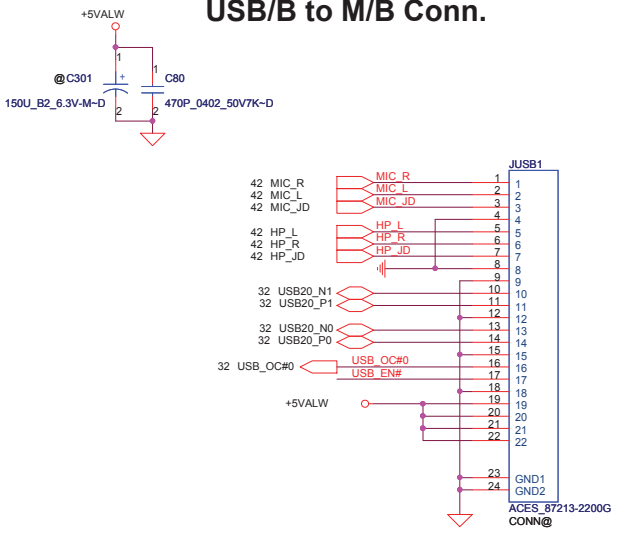
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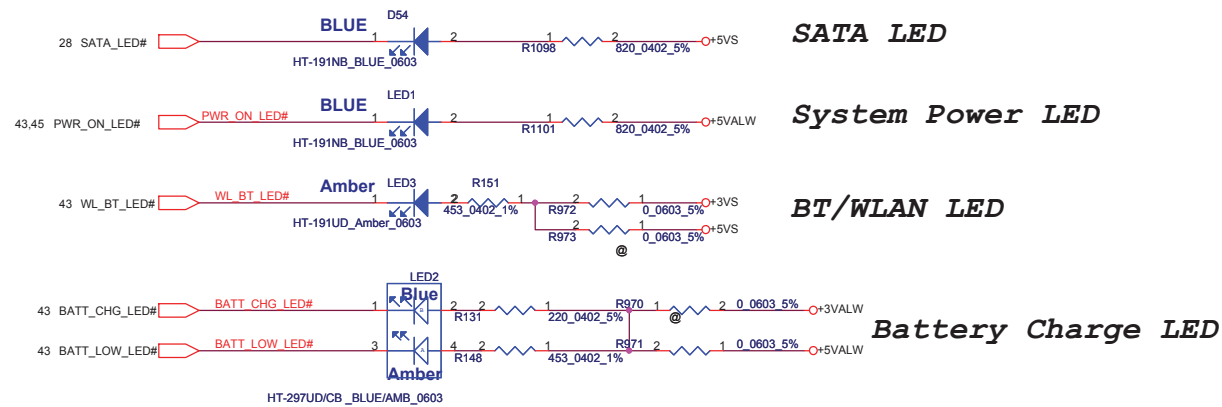
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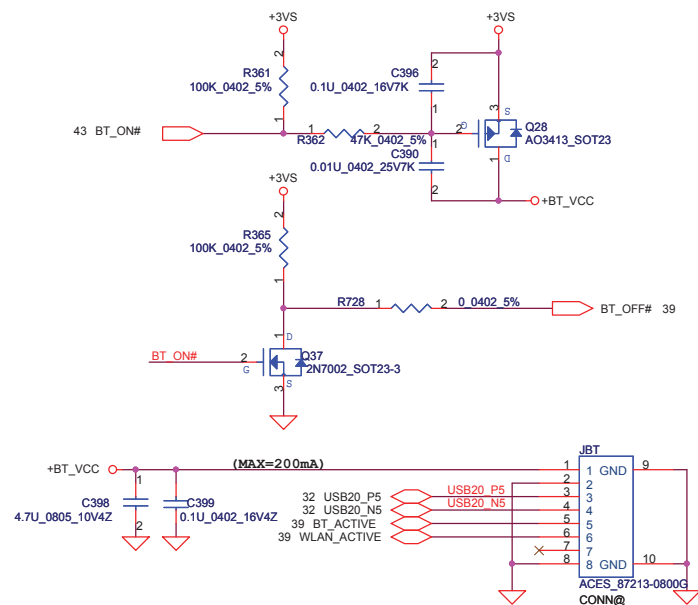
USB/B to M/B Conn.



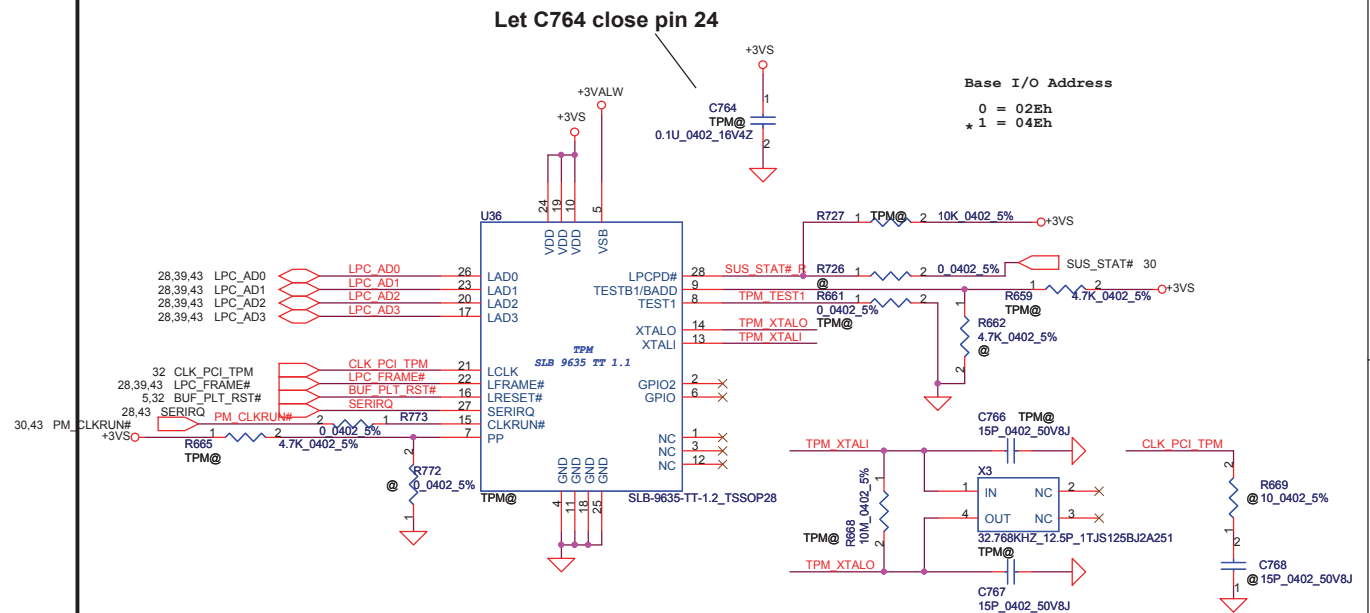
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Issued Date	200910/9	Deciphered Date	2010/01/23	Title	
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Size	Document Number	NCL60/61 LA-6321P M/B		Rev	0.1
Date	Wednesday, April 14, 2010	Sheet	37 of 57		



## BlueTooth Interface

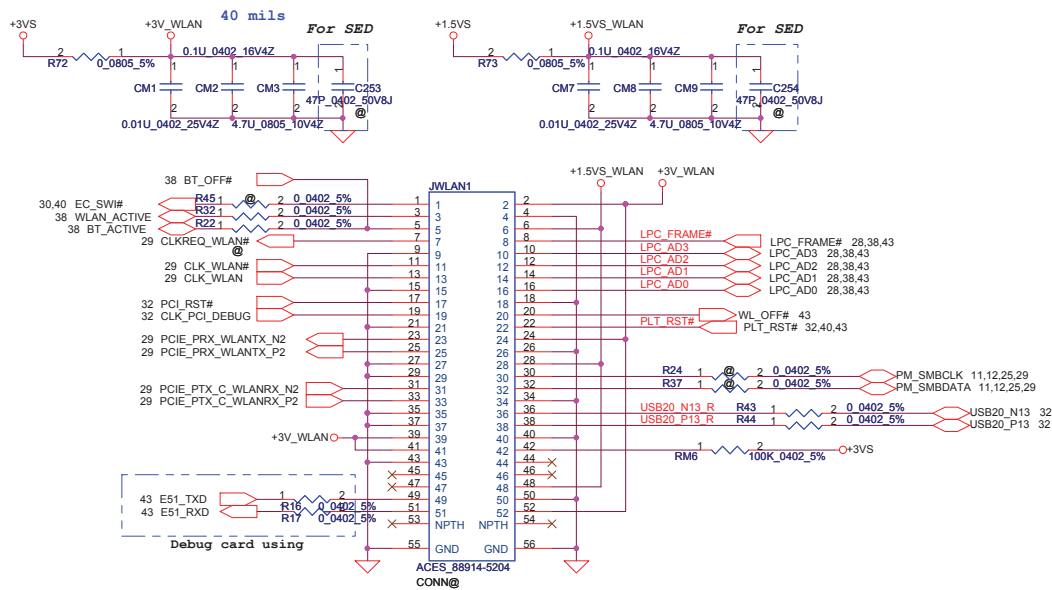


## TPM 1.2



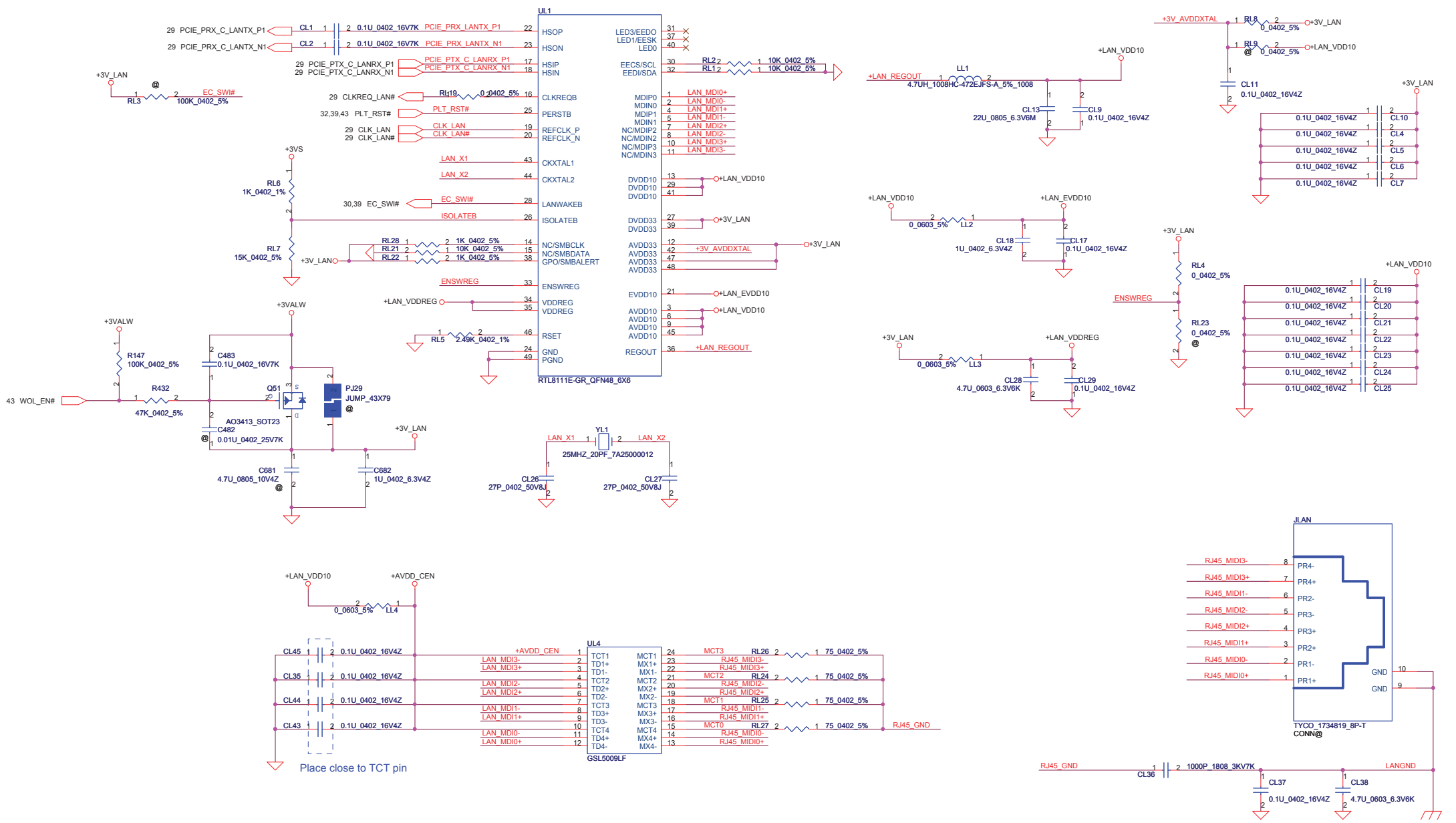
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				Rev	
				NCL60/61 LA-6321P M/B	
				Date:	Wednesday, April 14, 2010
				Sheet	38 of 57

# Slot 1 Half PCIe Mini Card-WLAN

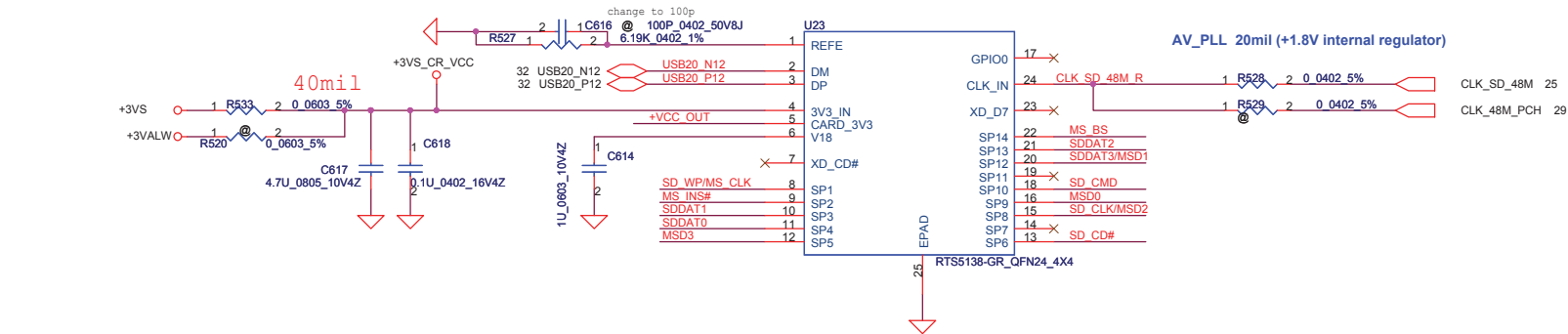


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Size	Document Number	NCL60/61 LA-6321P M/B		Rev
Date:	Wednesday, April 14, 2010	Sheet	39	of 57

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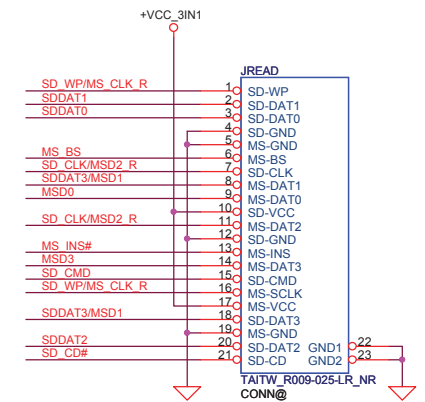
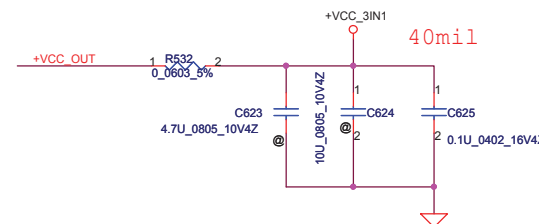
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				Custom	<b>NCL60/61 LA-6321P M/B</b>	0.1
Date: Wednesday, April 14, 2010		Sheet 40 of 57				



# SD,MMC,MS muti-function pin define

MDIO PIN Name	SD Card PIN Name	MMC Card PIN Name	MS Card PIN Name
SP1	SP1		SP1
SP2			
SP3			
SP4			
SP5			
SP6			
SP7			
SP8			
SP9			
SP10			
SP11			
SP12			
SP13			
SP14			
SP15			
SP16			
SP17			
SP18			
SP19			

SD CLK/MSD2 1 R538 2 0.0402 5% SD CLK/MSD2 R  
SD WP/MS\_CLK 1 R539 2 0.0402 5% SD WP/MS\_CLK R

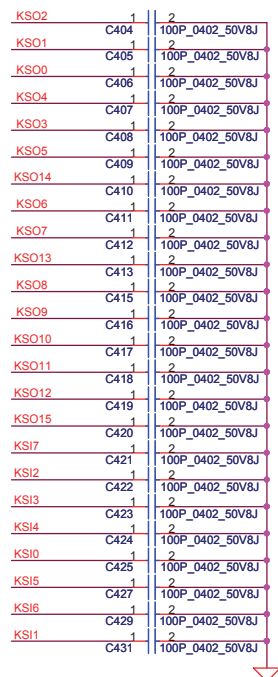
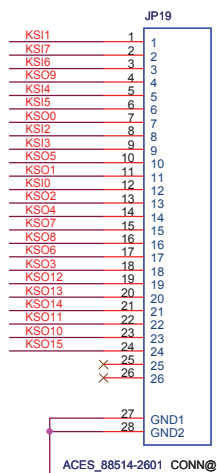
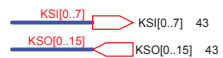
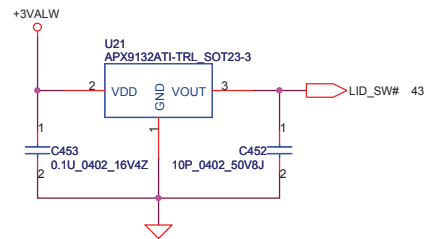
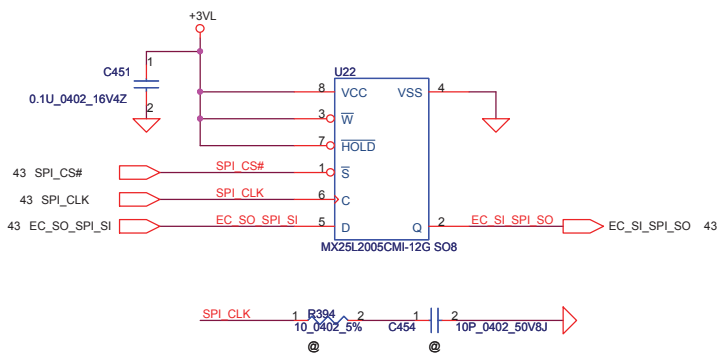


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Size	Custom	Document Number	NCL60/61 LA-6321P M/B		Rev 0.1
Date:	Thursday, April 15, 2010	Sheet	41	of	59

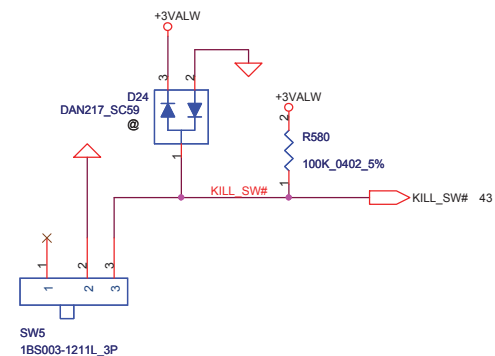
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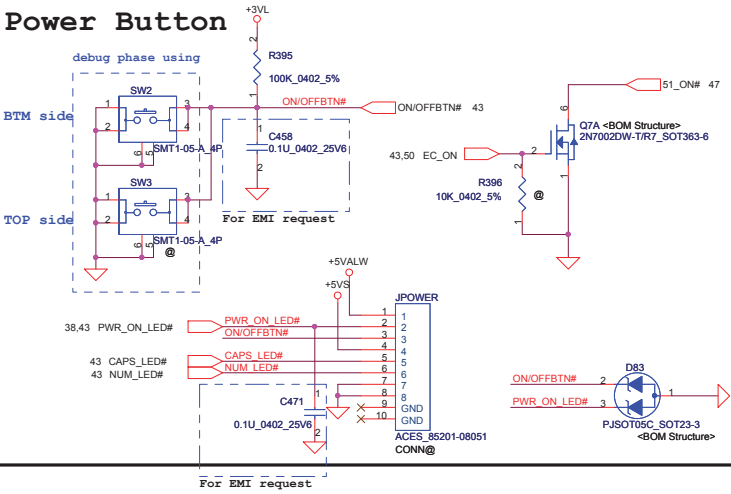


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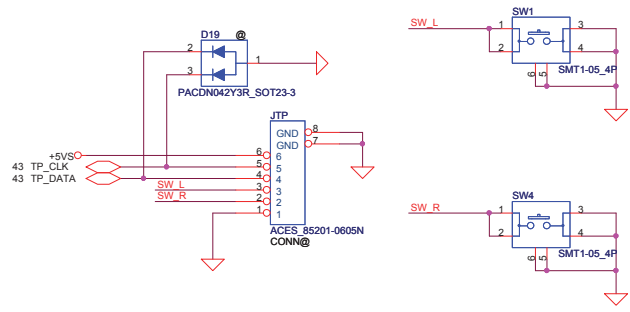


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								Size	Document Number			Rev
									NCL60/61 LA-6321P M/B			0.1
								Date:	Wednesday, April 14, 2010		Sheet	44

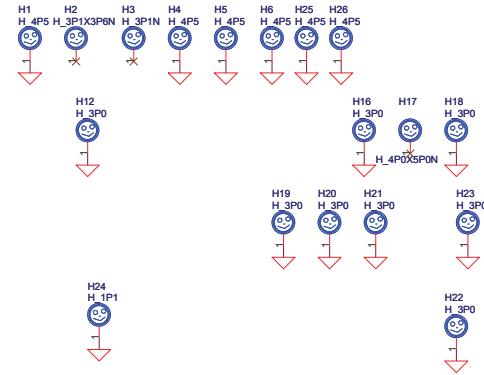
Power Button



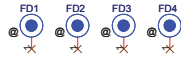
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Screw Hole



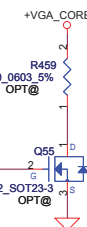
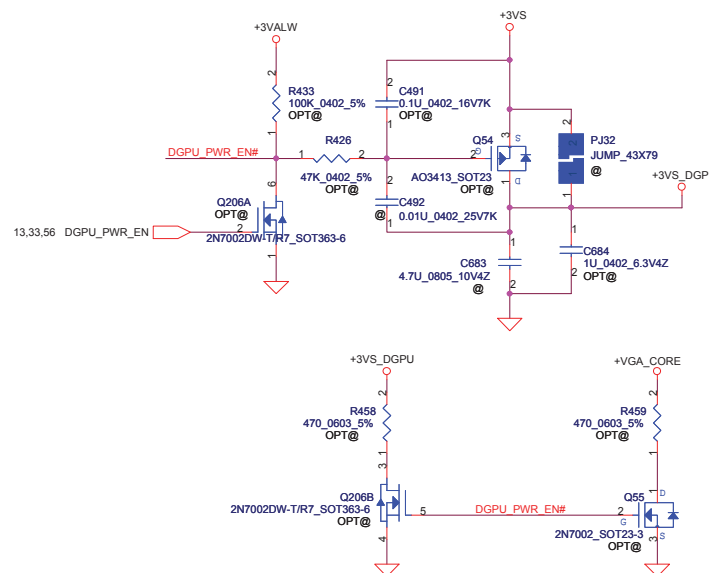
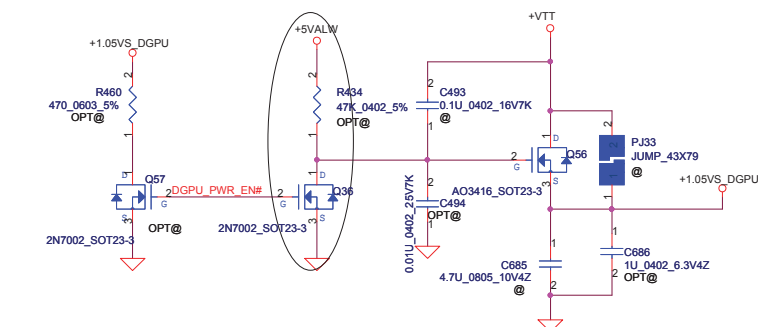
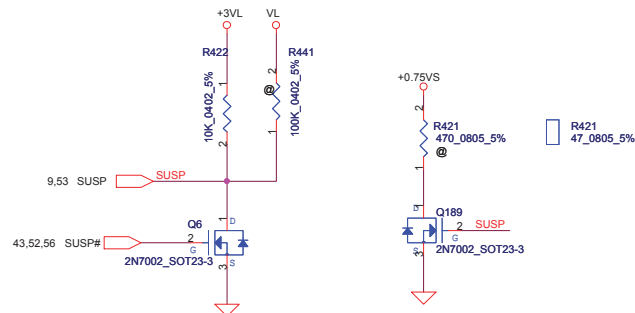
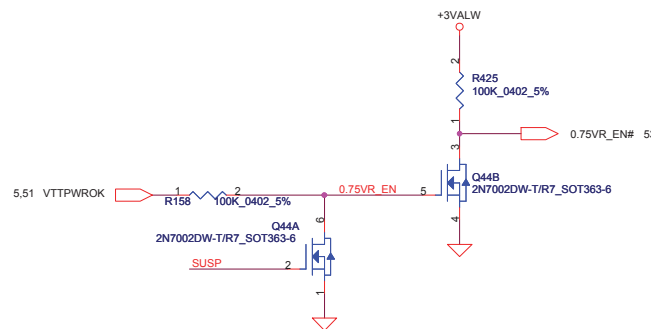
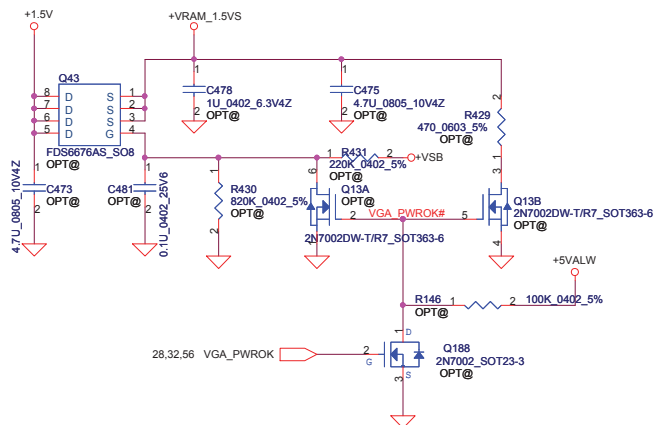
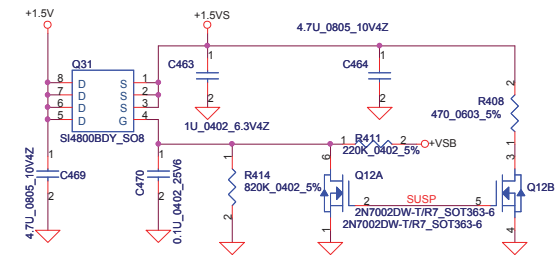
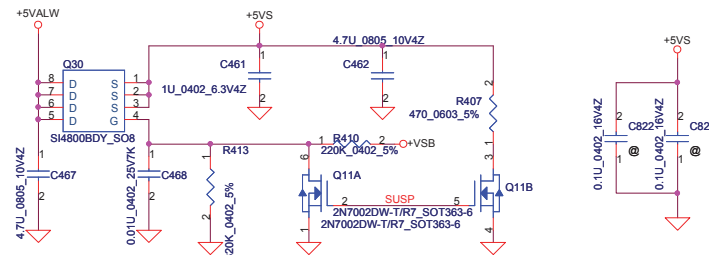
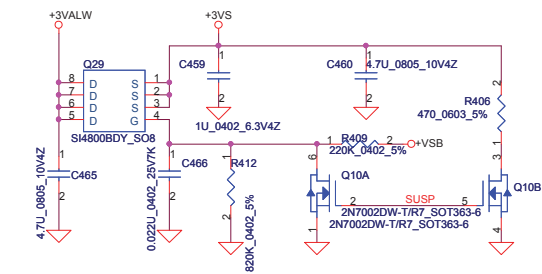
PCB Fedical Mark PAD



ISPD

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				Date	Wednesday, April 14, 2010
				Sheet	45 of 57
				Rev	0.1

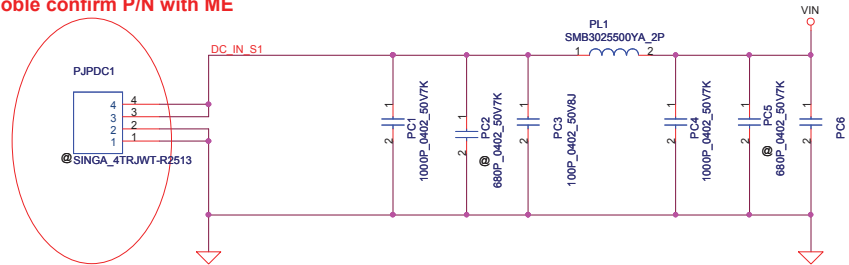


Change to N MOS at DVT and add R434, Q36

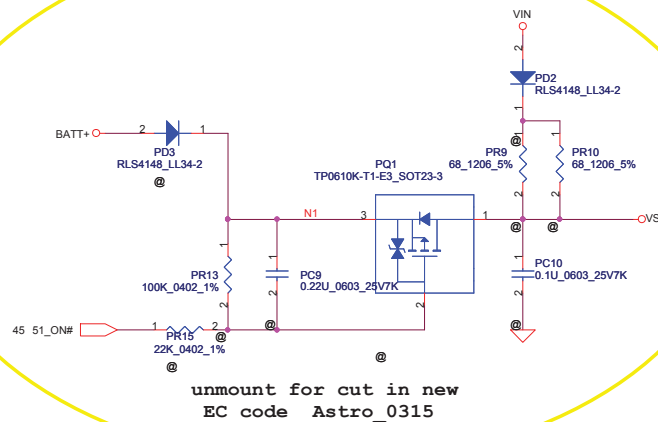
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Date: Monday, April 19, 2010				Sheet 46 of 57	

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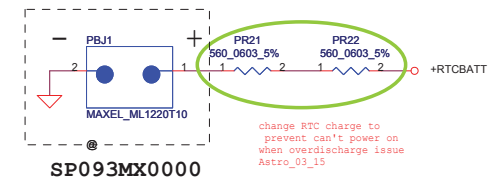
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need dogle confirm P/N with ME



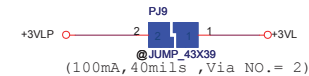
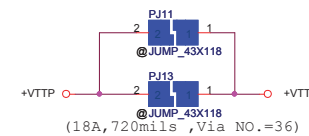
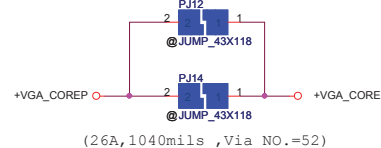
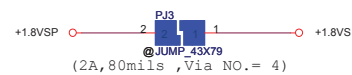
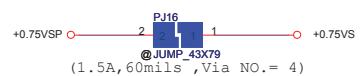
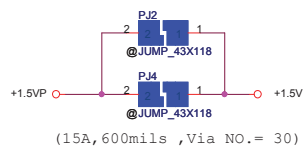
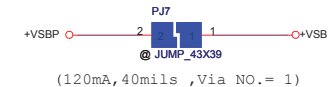
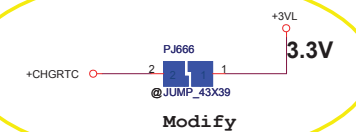
Modify the VIN\_DET, Pre-charge, RTC\_charge



RTC Battery



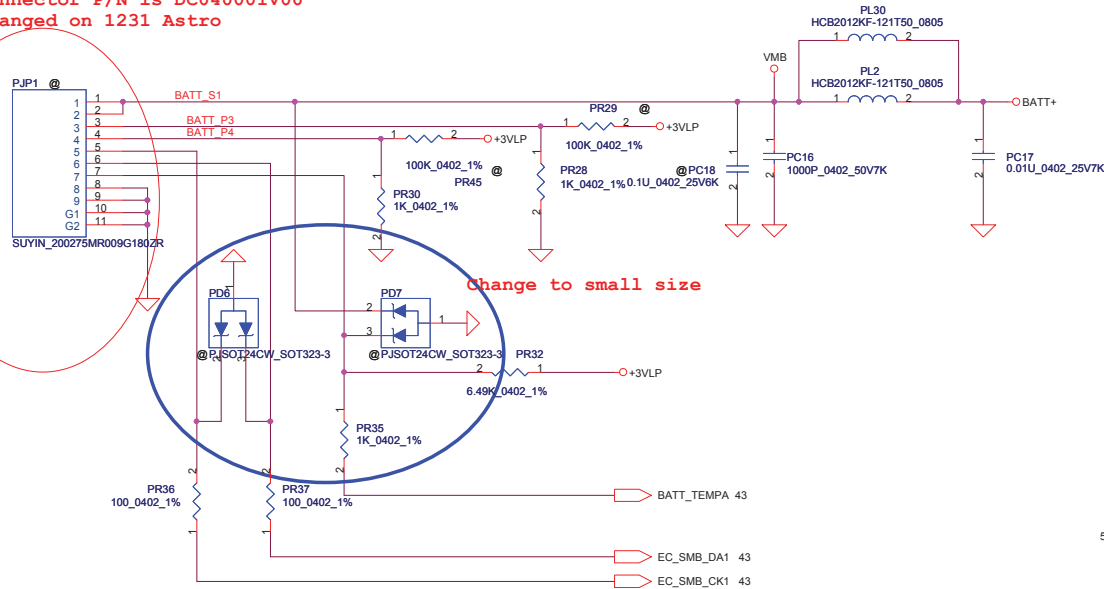
SP093MX0000



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					NCL61 LA-6321P M/B	0.1
				Date:	Wednesday, April 14, 2010	Sheet 47 of 59

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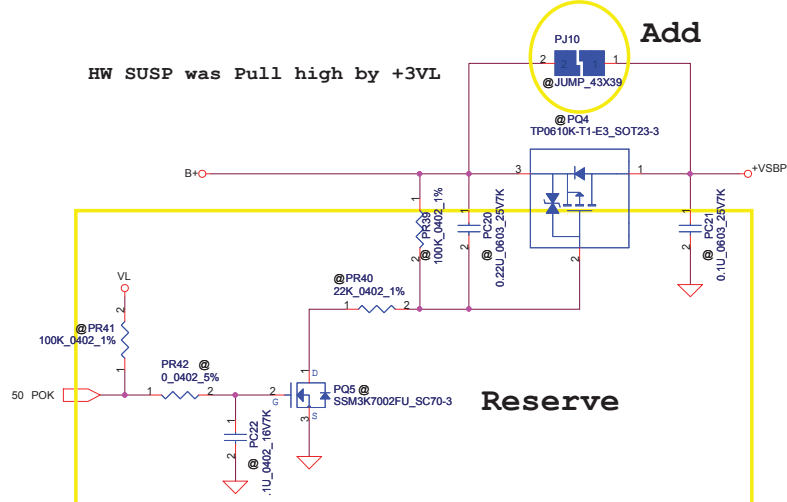
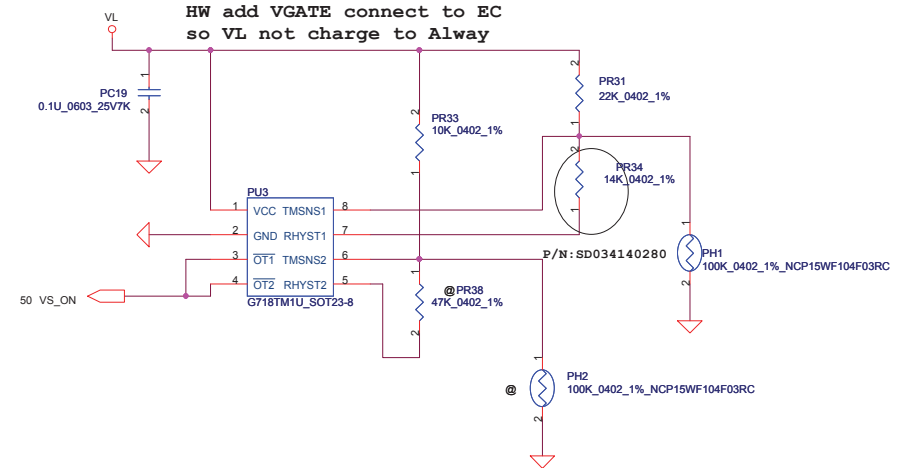
need confirm: ME give us battery  
connector P/N is DC040001V00  
changed on 1231 Astro



Rset = 3 \* Rtmh  
Rhyst = (Rset \* Rtm1) / (3 \* Rtm1 - Rset)  
Rtmh at 92C = 7.3092K, Rtm1 at 70C = 15.423K  
Rset = 3 \* 7.3092K = 21.9276K ==> 22K  
Rhyst = (21.9276K \* 15.423K) / (3 \* 15.423K - 21.9276K) = 13.98K ==> 14K  
change temprature setting Astro1231

PH1 under CPU botten side :  
CPU thermal protection at 92 degree C  
Recovery at 70 degree C

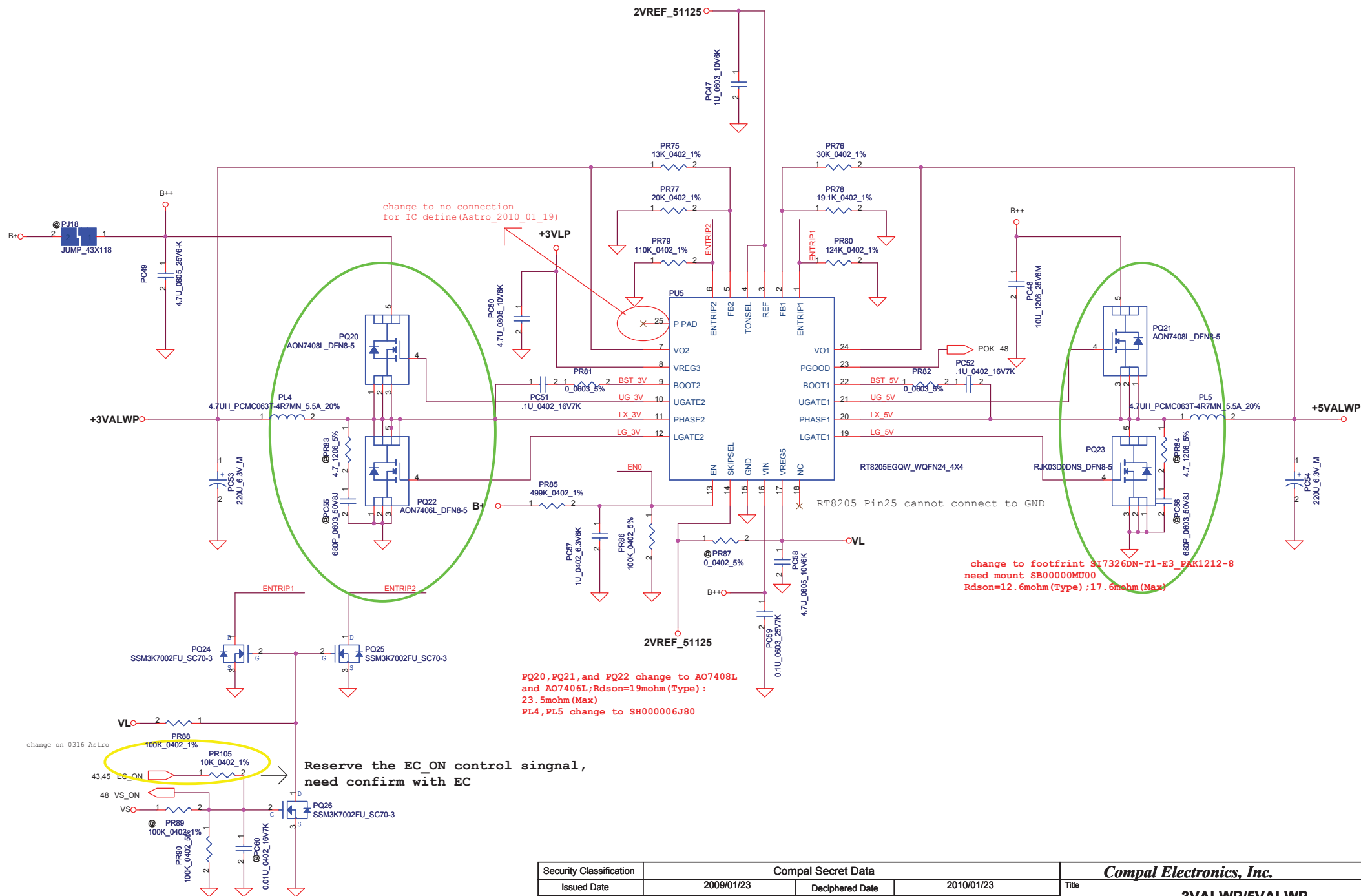
PH2 near main Battery CONN : Reserve  
BAT. thermal protection at 90 degree C  
Recovery at 53 degree C



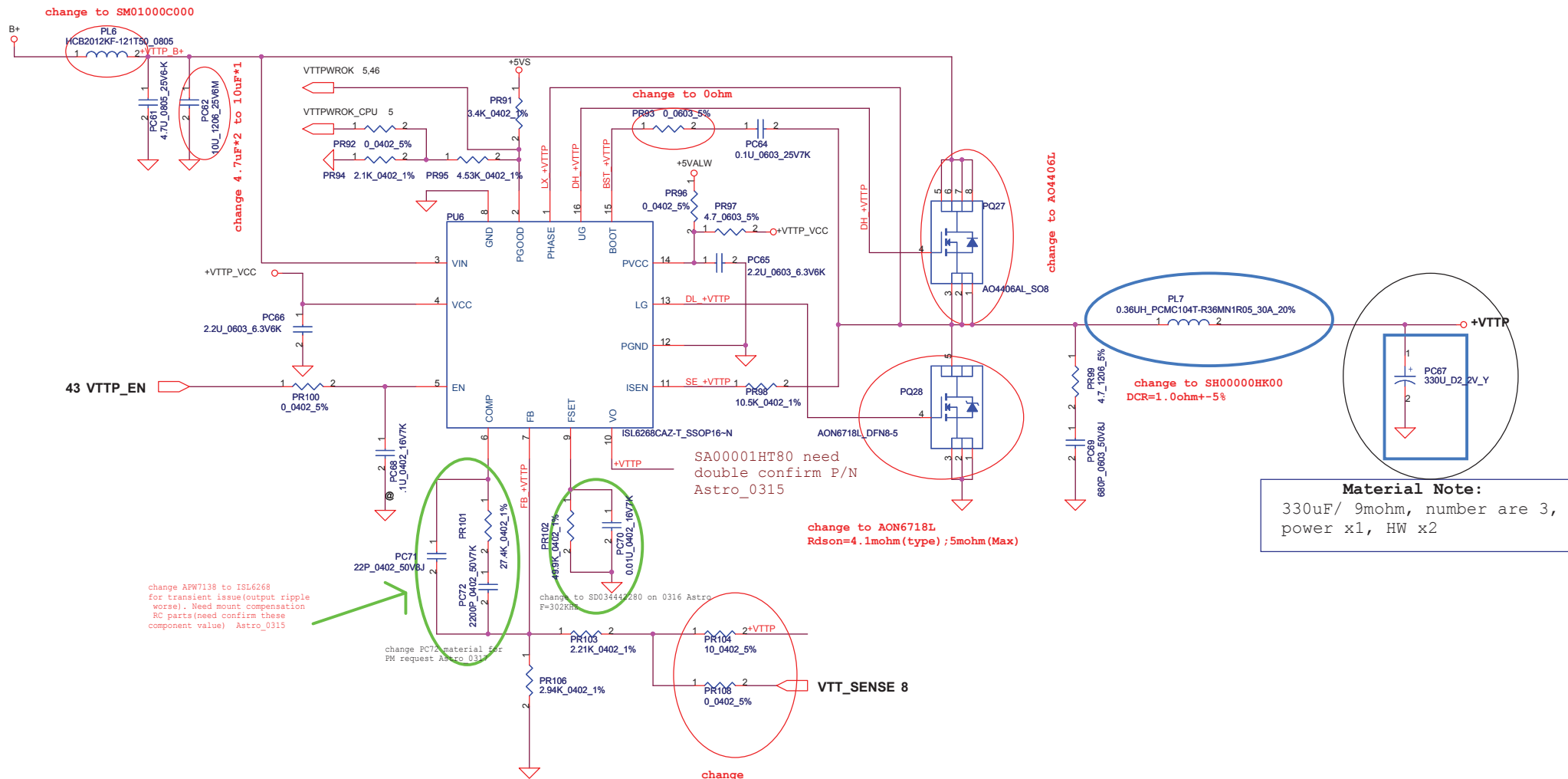
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				Document Number
				NCL61 LA-6321P M/B
				Rev
				0.1
Date: Wednesday, April 14, 2010		Sheet 48 of 59		

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Issued Date	2009/01/23	Deciphered Date	2010/01/23	Title	
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				Rev	0.1
				Date:	Monday, April 19, 2010
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				Date:	Monday, April 19, 2010	Sheet 51 of 59

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