

Compal Confidential

Model Name : Q3ZMC

File Name : LA-8481P

# Compal Confidential

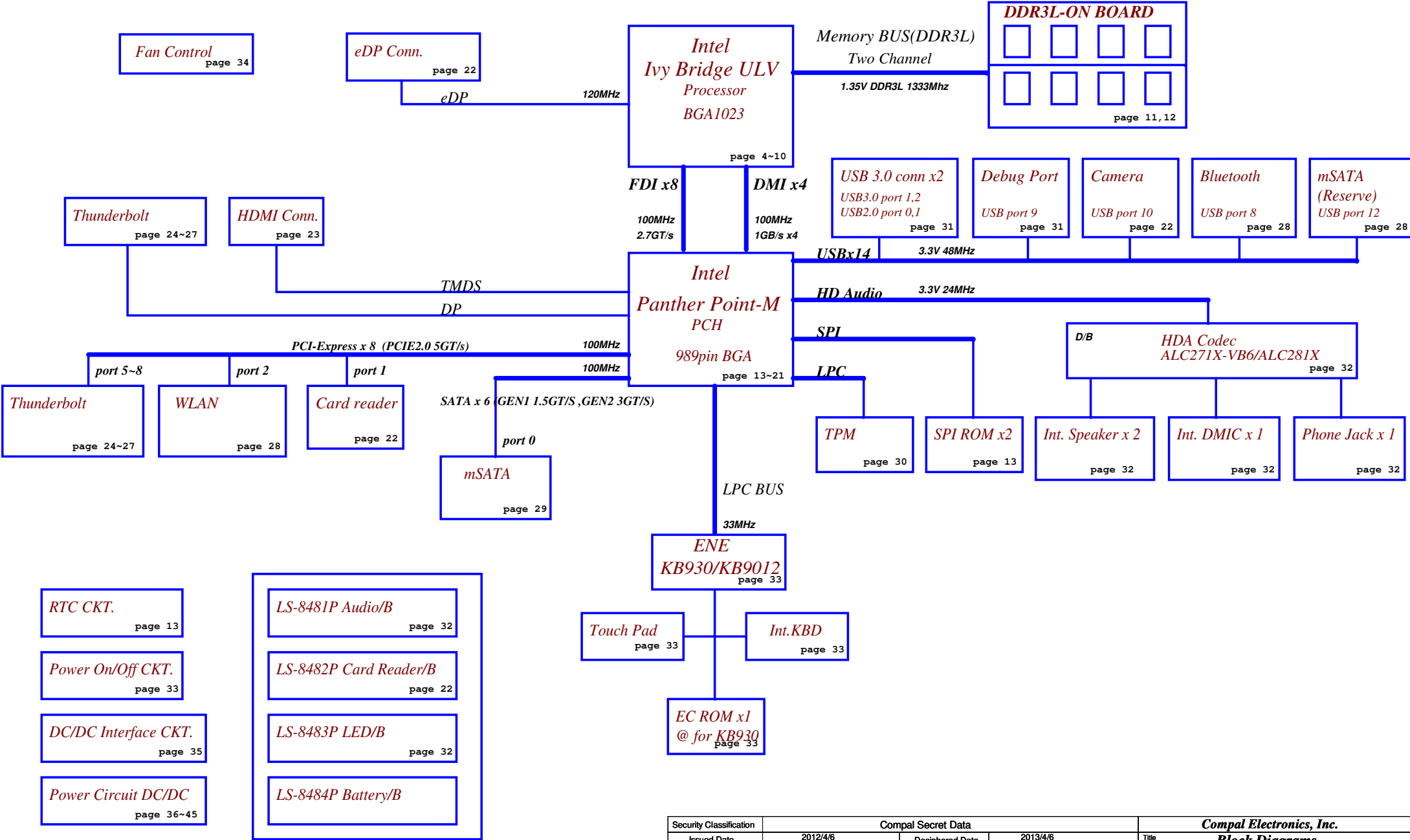
## Q3ZMC UMA M/B Schematics Document

Intel Ivy/Sandy Bridge SFF BGA 1023p Processor  
/Panther Point 989p PCH  
/ DDR3L Memory Down \*8

2012-04-11

REV : 1 . 0 (MP SMT)

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Issued Date	2012/4/6	Deciphered Date	2013/4/6	Title	Cover Page
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+CPU_CORE	Core voltage for CPU	ON	ON	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+1.05VS_VTT	+1.05VS_VTTP to +1.05VS_VTT switched power rail for CPU	ON	OFF	OFF
+1.05VS_PCH	+1.05VS_VTT to +1.05VS_PCH power for PCH	ON	OFF	OFF
+1.35V	+1.35VP to +1.35V power rail for DDR3L	ON	ON	OFF
+1.35VS	+1.35V to +1.35VS switched power rail	ON	OFF	OFF
+0.675VS	+0.675VSP to +0.675VS switched power rail for DDR3L terminator	ON	OFF	OFF
+1.5VS	+1.5VSP to +1.5VS power rail for PCH	ON	OFF	OFF
+1.8VS	+3VALW to 1.8VS switched power rail for PCH	ON	OFF	OFF
+3VALW	+3VALWP to +3VALW always on power rail	ON	ON	ON*
+3VALW_PCH	+3VALW to +3VALW_PCH power rail for PCH (Short Resistor)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW always on power rail	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+RTCVCC	RTC power	ON	ON	ON
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.				

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b		

EC SM Bus2 address

PCH SM Bus address

Device	Address
ChannelA	A0 1010 000X
ChannelB	A4 1010 010X

BOM Config  
4319HNBOL01:UMA@/DDR3L@/eDP@/USB3.0@/9012@/TB@/IVB@/HM77@/DS3@/TXM@/TPM@/128@/  
4319HNBOL02:UMA@/DDR3L@/eDP@/USB3.0@/9012@/TB@/IVB@/HM77@/DS3@/TXM@/TPM@

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.10.2
1	0.3 DVT:unknown MCU+MKS Motor,With TB IC
2	0.4 PVT1:PADAUK MCU+MKS Motor,Without TB IC
3	0.4 PVT2:PADAUK MCU+MKS Motor,With TB IC
4	1.0
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
Unpop	@
Connector	CONN@
UMA	UMA@
CPU	IVB@
PCH	HM77@
DDR3	DDR3@
DDR3L	DDR3L@
On Board DRAM	X76@
128bit RAM	128@
eDP	eDP@
LVDS	LVDS@
USB2.0 Conn	USB2.0@
USB3.0 Conn	USB3.0@
Thunderbolt	TB@
KB930	930@
KB9012	9012@
Normal S3	S3@
Deep S3	DS3@
TPM+TCM	TXM@
TPM	TPM@
TCM	TCM@

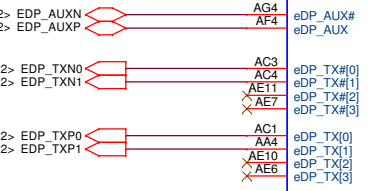
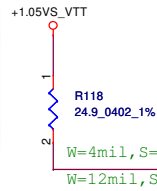
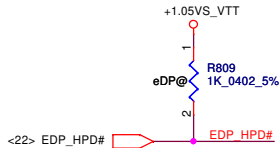
USB Port Table

USB 2.0	USB 1.1	Port	2 External USB Port
EHCI1	UHCI0	0	USB port (Rear side 3.0)
		1	USB port (Rear side 3.0)
		2	
	UHCI1	3	
		4	
		5	
EHCI2	UHCI2	6	
		7	
		8	
	UHCI3	9	Debug Port
		10	Camera
		11	
	UHCI4	12	mSATA(Reserve)
		13	BlueTooth

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eDP\_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms, even if disable eDP function...

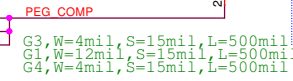
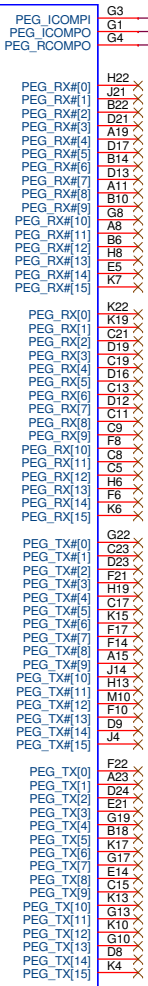
Add eDP circuit



IVY-BRIDGE\_BGA1023  
1VB@

ULV type P/N:  
1.SA00005B000:S IC AV8063801057400 QBP7 K0 1.7G BGA  
2.SA00005AZ30:S IC AV8063801057401 QBTP K0 1.5G BGA

PCI EXPRESS -- GRAPHICS

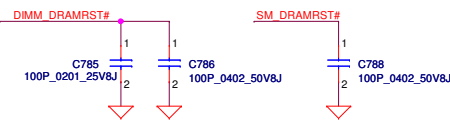
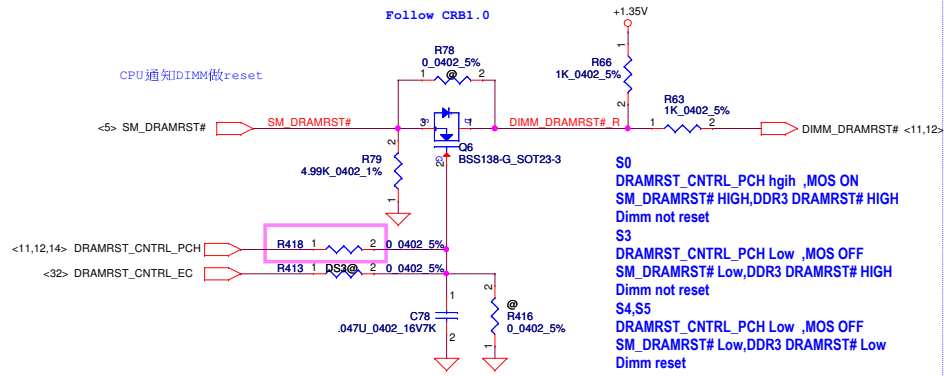
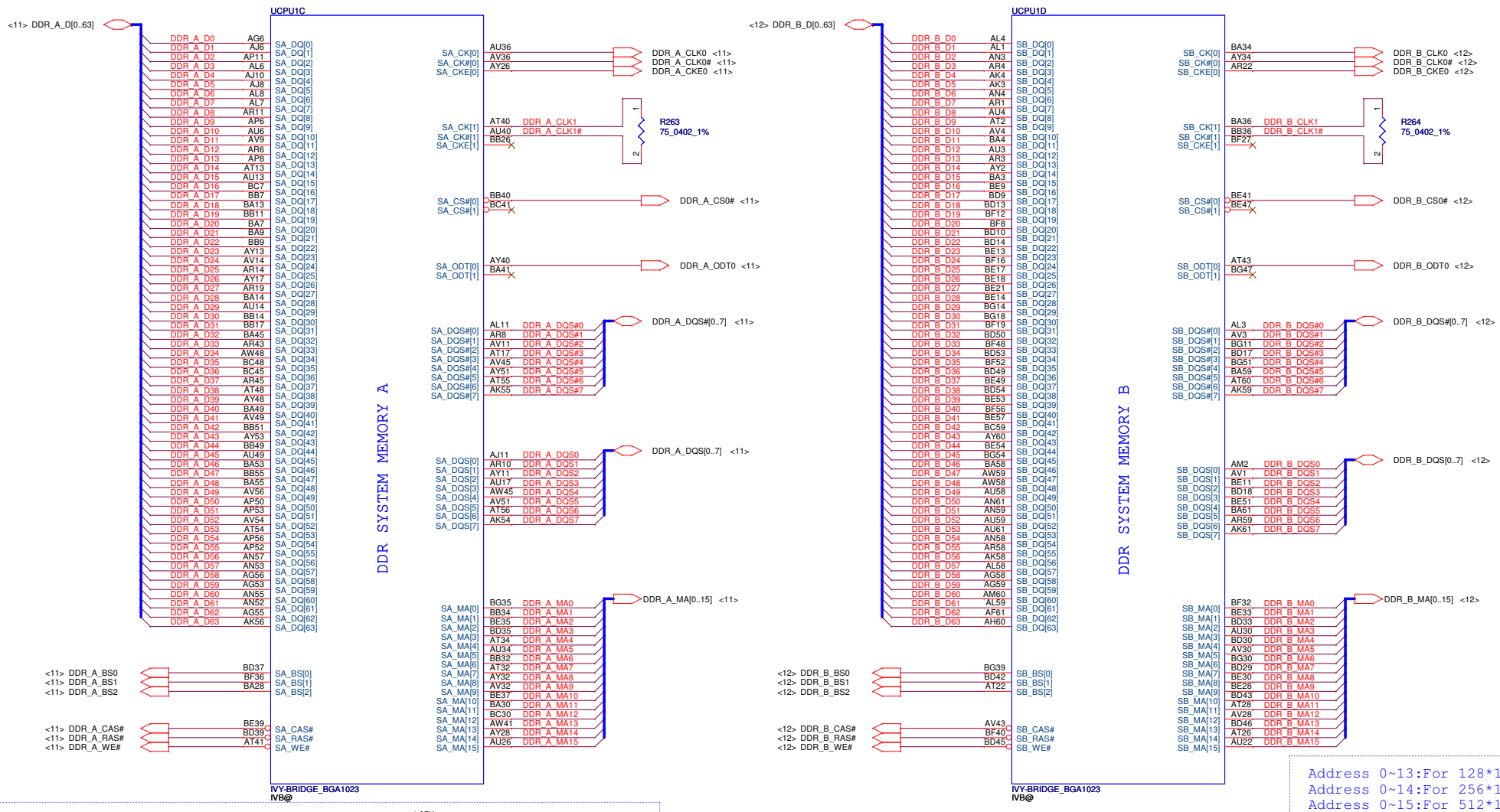


PEG\_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms  
PEG\_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms

UMA only=>PEG NC

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				Size		Document Number		Rev	
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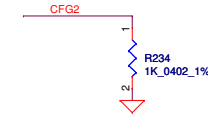


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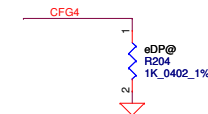
## CFG Straps for Processor

PEG Static Lane Reversal - CFG2 is for the 16x

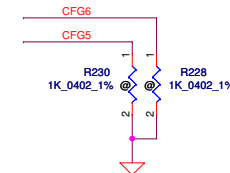
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition ★ 0: Lane Reversed
------	--



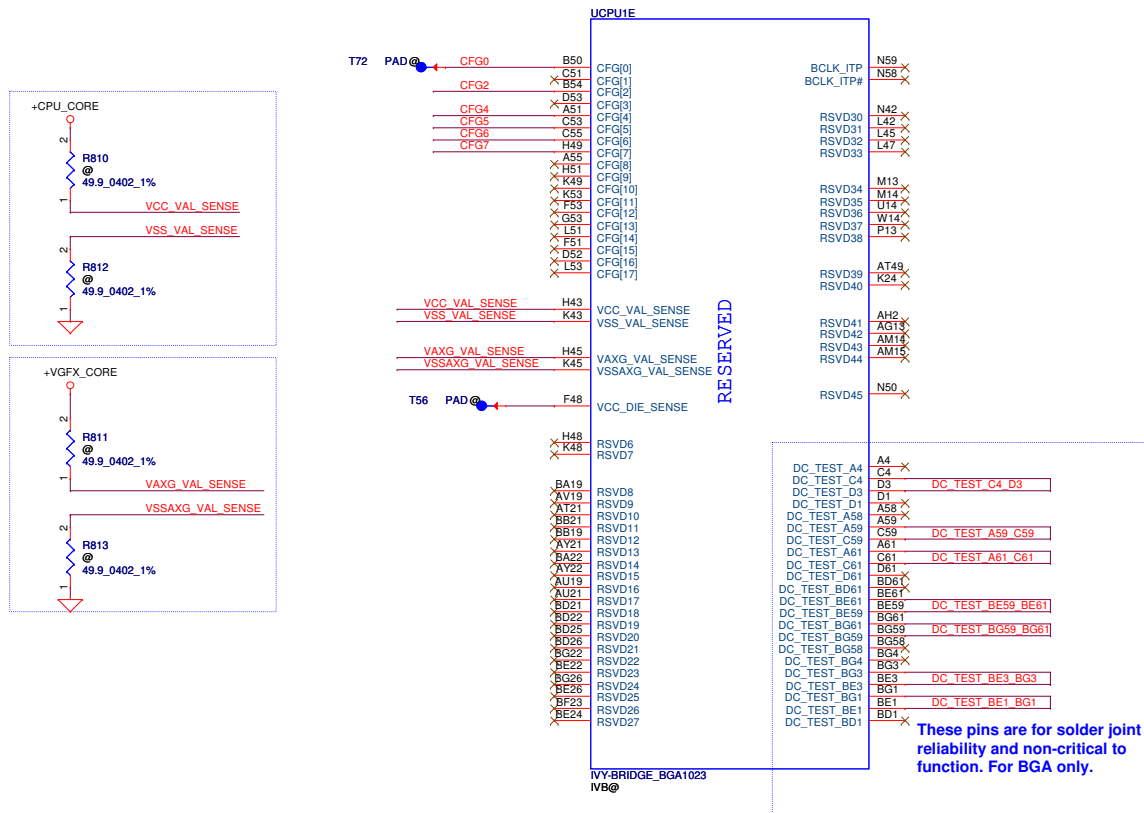
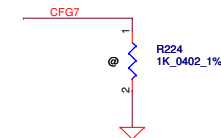
eDP enable	★ 1: Disable 0: Enable
------------	---------------------------



PCIE Port Bifurcation Straps	★ 11: (Default) 1x16 PCI Express 10: 2x8 PCI Express 01: Reserved 00: 1x8,2x4 PCI Express
------------------------------	--



PEG DEFER TRAINING	CRB1.0 P.12
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



ULV SC/DC 33A

+CPU\_CORE

A26  
A29  
A31  
A34  
A35  
A38  
A39  
A42  
A44  
C26  
C27  
C32  
C34  
C37  
C38  
C42  
D27  
D32  
D34  
D37  
D39  
D42  
E28  
E32  
E34  
E37  
E38  
F28  
F32  
F34  
F37  
F38  
F42  
G42  
H25  
H28  
H32  
H34  
H38  
H39  
H40  
J26  
J28  
J32  
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J38  
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J42  
K26  
K27  
K29  
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K42  
L28  
L33  
L36  
L40  
N26  
N30  
N34  
N38

VOC[1]  
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VOC[75]  
VOC[76]

## 8.5A

330uF 1+1  
10uF (0603) \*5  
1uF (0201) \*16

330uF 1  
10uF (0603) \*5  
1uF (0201) \*10

Check List R1.5  
VIDALERT#: 75ohm  $\pm 5\%$  pull-up to VCCIO close to IMVP7  
VIDSCLK: 55ohm  $\pm 5\%$  pull-up to VCCIO close to IMVP7  
VIDSOUT: 130ohm  $\pm 5\%$  pull-up to VCCIO close to CPU  
130ohm  $\pm 5\%$  pull-up to VCCIO close to IMVP7

**Check List R1.5**  
VCCSENSE:100ohm  $\pm 1\%$  pull-up to VCC near processor.  
VSSSENSE:100ohm  $\pm 1\%$  pull-down to GND near processor.

Place the PU,PD resistors close to CPU

Should change to connect from power circuit & layout differential with VCCIO SENSE.

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INTEL Recommend VAXG  
2\*330uF,5\*22uF(0805),6\*10uF(0603),6\*1uF(0402)  
PD 0.9

Check List R1.5  
VCCAXG\_SENSE:100ohm  $\pm$ 5% pull-up to VCC near processor.  
VSSAXG\_SENSE:100ohm  $\pm$ 5% pull-down to GND near processor.

INTEL Recommend VCCPLL  
1\*330uF,2\*1uF(0402)  
PD 0.9

INTEL Recommend VCCSA  
1\*330uF,5\*10uF(0603) ,5\*1uF(0402)  
PD0.9

ULV SC/DC GT1: 18A  
GT2: 33A

## POWER

GRAPHICS

DDR3 - 1.5V RAILS

QUIET RAILS

SENSE LINES

VCCSA VID Lines

SA\_DIMM\_VREFDQ  
SB\_DIMM\_VREFDQ  
For Future CPU M3 support,  
Sandy bridge not support M3,  
Check list1.0 & CRB say can NC

+V\_SM\_VREF should  
have 20 mil trace width

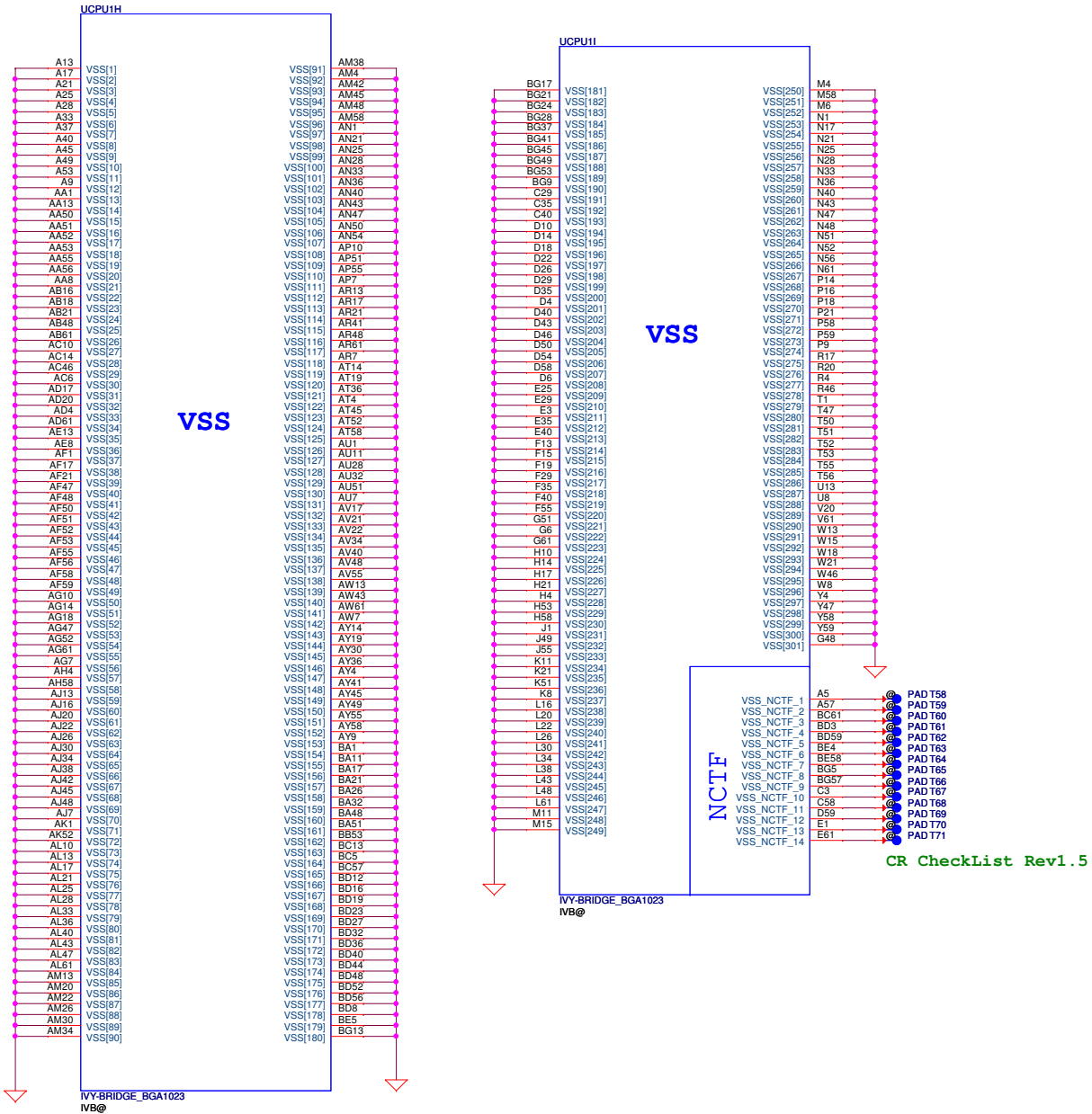
INTEL Recommend VDDQ  
1\*330uF,8\*10uF(0603) ,10\*1uF(0402)  
PD0.9

Short for +1.35VS to +1.35V\_CPU\_VDDQ

Place BOT OUT Conn

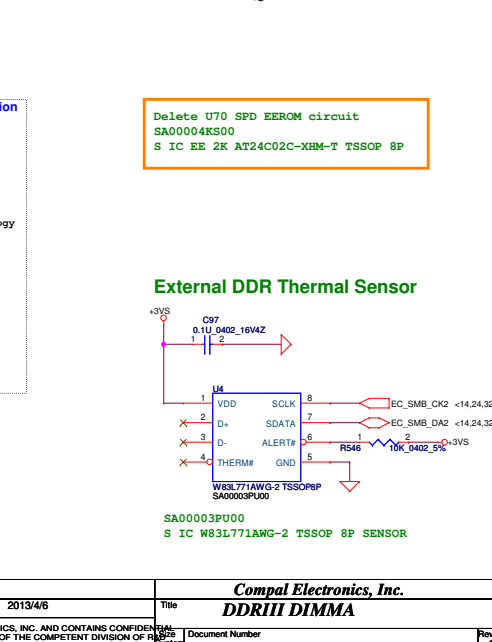
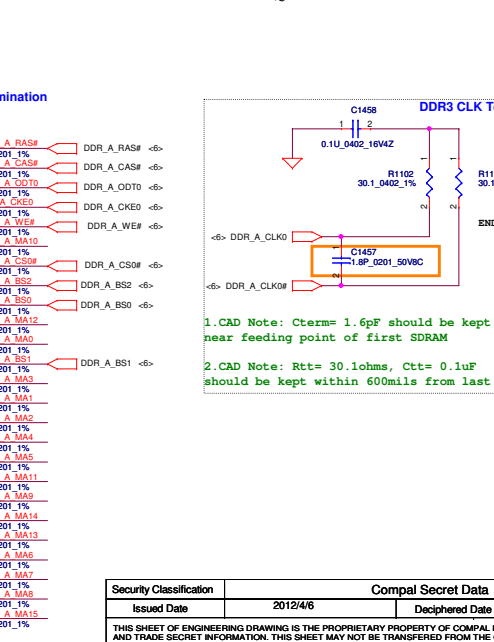
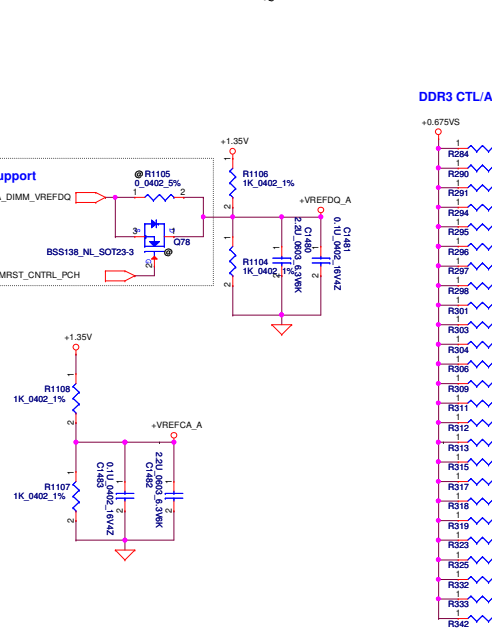
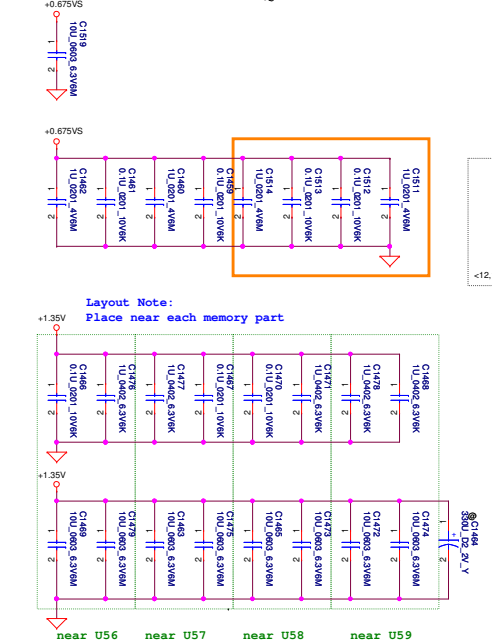
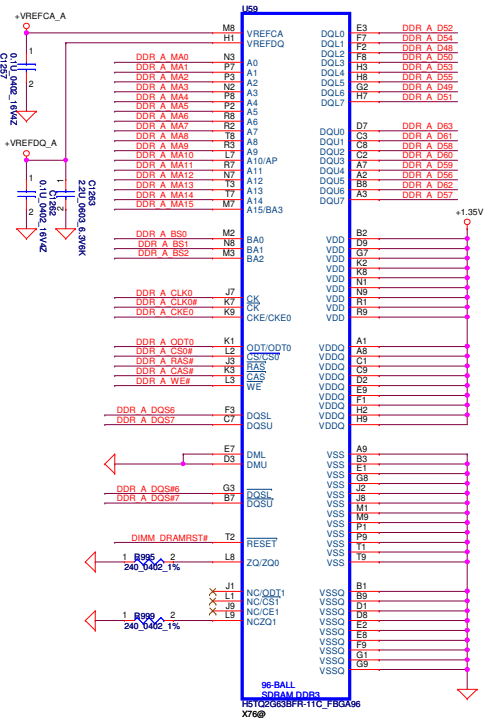
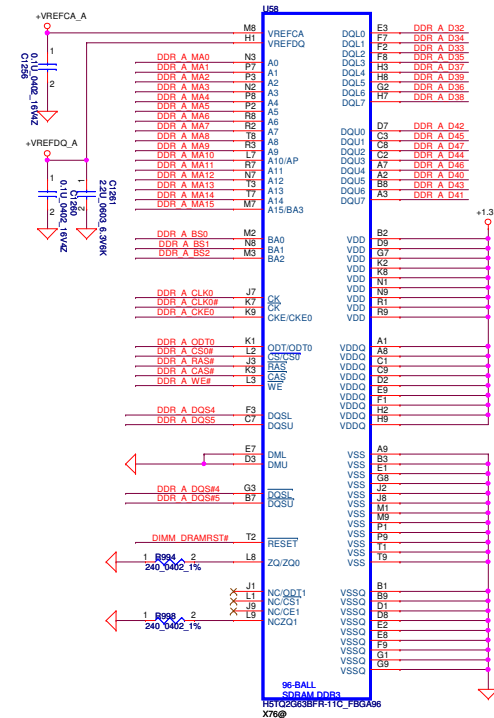
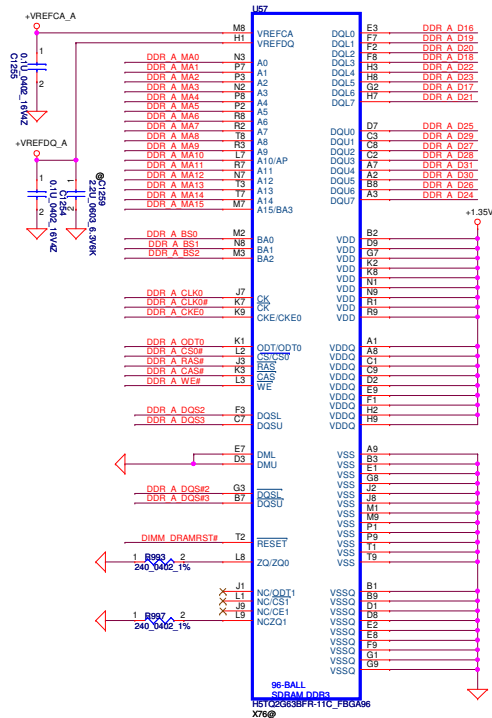
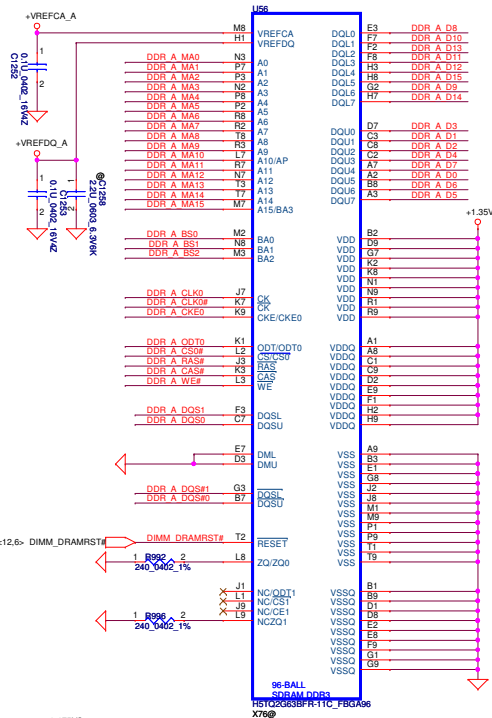
VCCSA\_VID  
For 2012 future CPU  
VCCSA voltage select

VCCSA					
VID0	VID1	Vout	SNB	IVB	ULV
0	0	0.9V	V	V	V
0	1	0.8V	V	V	V
		0.85V			
1	0	0.725V	X	V	V
1	1	0.675V	X	V	V

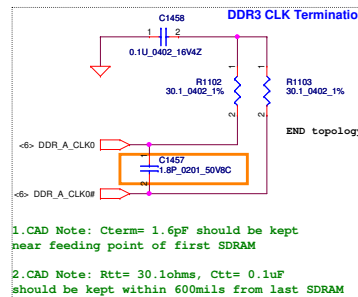
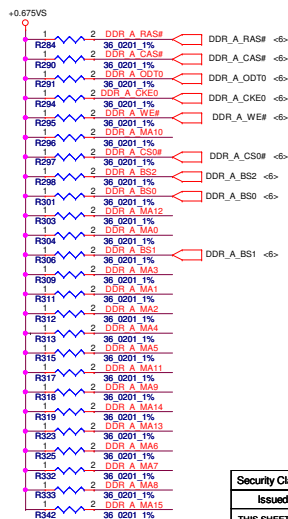


# Channel A

<6> DDR\_A\_MA0[0..15]   
 <6> DDR\_A\_DQS#0[0..7]   
 <6> DDR\_A\_DQS#0[0..7]   
 <6> DDR\_A\_DQ0[0..63] 

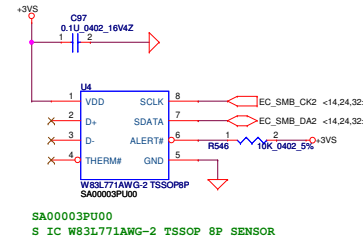


## DDR3 CTL/ADD Termination



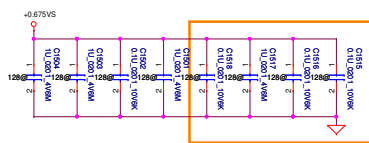
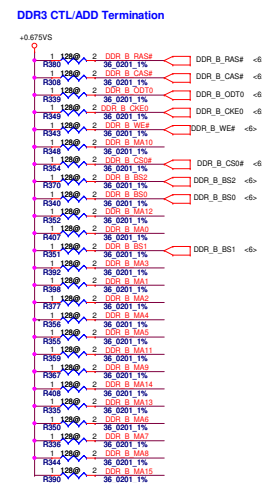
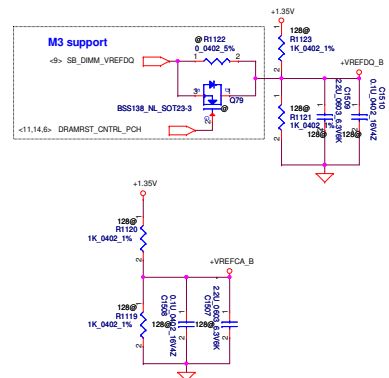
Delete U70 SPD EEROM circuit  
 SA00004KS00  
 S IC EE 2K AT24C02C-XHM-T TSSOP 8P

## External DDR Thermal Sensor



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DDR\_B\_DQS#[0..7] <6>  
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 DDR\_B\_D[0..63] <6>  
 DDR\_B\_MA[0..15] <6>

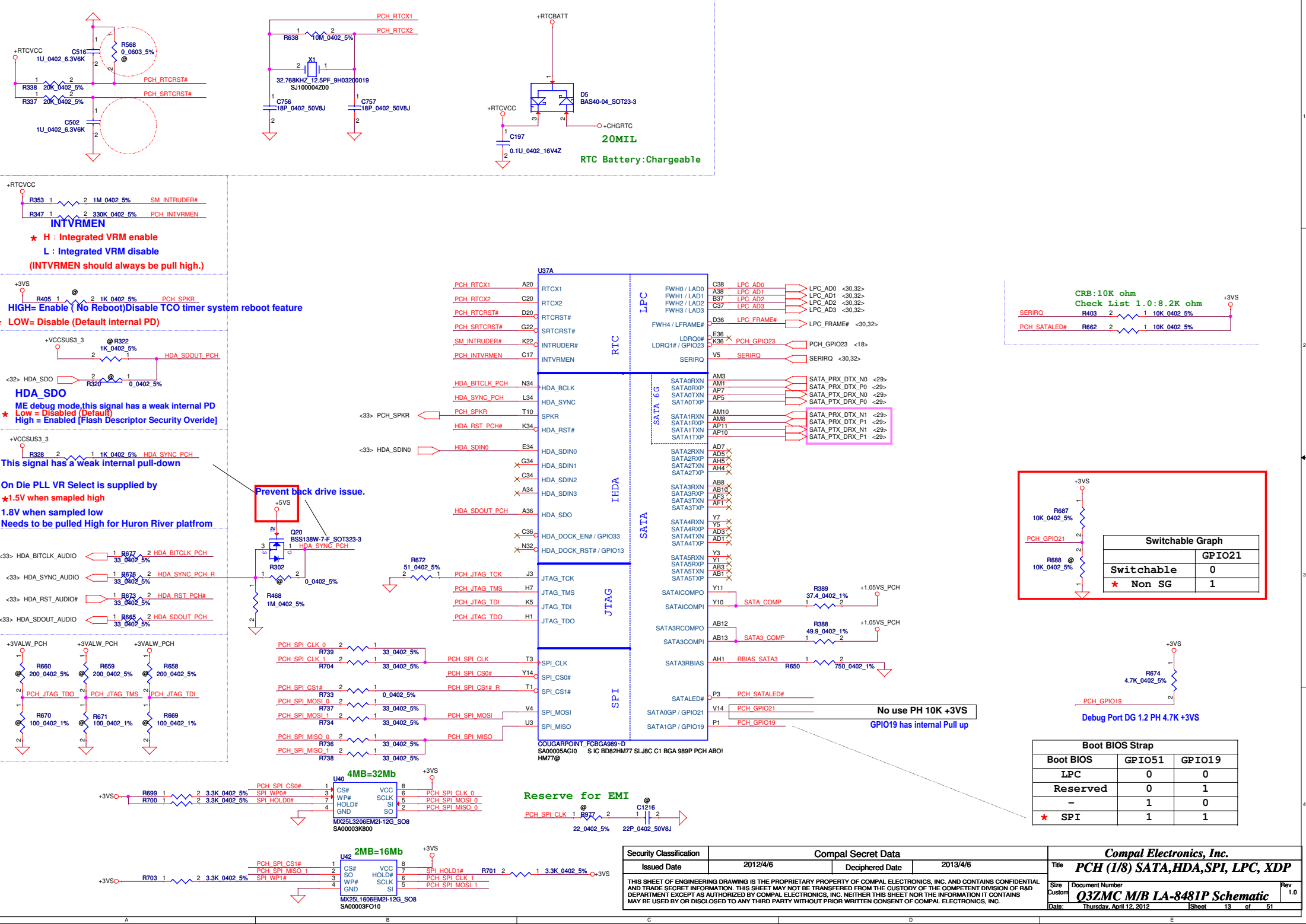
[illegible]

The diagram illustrates a DDR3 clock termination circuit. It features a differential signal path with two main signal lines, `DDR_B_CLK0` and `DDR_B_CLK0#`, which are connected to a pair of termination resistors (R117 and R118) in parallel with a capacitor (C106). The resistors are labeled `30.1_0402_1%`. The capacitor is labeled `C106 1.6P_0301_50VDC`. The circuit is terminated to a common ground plane, which is also connected to a `128Ω` resistor. The signal lines are labeled `128Ω` and `30.1_0402_1%`. The diagram is titled `DDR3 CLK Termination` and includes a note: `END topology`.

1. CAD Note: Cterm = 1.6pF should be kept near feeding point of first SDRAM

2. CAD Note: Rtt = 30.1ohms, Ctt = 0.1uF should be kept within 600mils from last SDRAM

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			Date	Q3ZMC M/B 1A-8481P Scheme
			Drawn	Thursday, April 16, 2015
			Steel	12
				91



+RTCVCC

R353 1 2 1M 0402 5% SM\_INTRUDER#

R347 1 2 330K 0402 5% PCH\_INTRVREN

**INTVYRMEN**

★ H : Integrated VRM enable

L : Integrated VRM disable

(INTVYRMEN should always be pull high.)

+3VS

R405 1 2 1K 0402 5% PCH\_SPKR

**HIGH= Enable ( No Reboot)Disable TCO timer system reboot feature**

★ **LOW= Disable (Default internal PD)**

+VCCSUS3\_3

R322 1 2 1K 0402 5% HDA\_SDOUT\_PCH

<32> HDA\_SDO

**HDA\_SDO**

ME debug mode this signal has a weak internal PD

★ **Low = Disabled (Default)**

**High = Enabled (Flash Descriptor Security Override)**

+VCCSUS3\_3

R328 2 1 1K 0402 5% HDA\_SYNC\_PCH

**This signal has a weak internal pull-down**

On Die PLL VR Select is supplied by

★ **1.5V when sampled high**

**1.8V when sampled low**

**Needs to be pulled High for Huron River platform**

+3VALW\_PCH

R660 200 0402 5%

PCH\_JTAG\_TDO

R670 100 0402 1%

+3VALW\_PCH

R659 200 0402 5%

PCH\_JTAG\_TMS

R671 100 0402 1%

+3VALW\_PCH

R658 200 0402 5%

PCH\_JTAG\_TDI

R669 100 0402 1%

<33> HDA\_BITCLK\_AUDIO

R677 33 0402 5%

HDA\_BITCLK\_PCH

<33> HDA\_SYNC\_AUDIO

R676 33 0402 5%

HDA\_SYNC\_PCH\_R

<33> HDA\_RST\_AUDIO#

R673 33 0402 5%

HDA\_RST\_PCH#

<33> HDA\_SDOUT\_AUDIO

R665 33 0402 5%

HDA\_SDOUT\_PCH

4MB=32Mb

U40

CS# VCC 8 PCH\_SPI\_CLK\_0

SO SCLK 7 PCH\_SPI\_MISO\_1

WP# HOLD# 5 PCH\_SPI\_CLK\_1

GND SI 2 PCH\_SPI\_MISO\_0

MX25L3206EM2I-12G\_S08

SA00003K800

4MB=16Mb

U42

CS# VCC 8 PCH\_SPI\_CLK\_0

SO SCLK 7 PCH\_SPI\_MISO\_1

WP# HOLD# 5 PCH\_SPI\_CLK\_1

GND SI 2 PCH\_SPI\_MISO\_0

MX25L1606EM2I-12G\_S08

SA00003F010

Reserve for EMI

R707 22 0402 5%

22P 0402 50V8J

CRB:10K ohm

Check List 1.0:8.2K ohm

SERIRQ

R403 2 1 10K 0402 5%

PCH\_SATALED#

R662 2 1 10K 0402 5%

+3VS

Switchable Graph

Switchable	GPIO21
0	0
★ Non SG	1

+3VS

R687 10K 0402 5%

PCH\_GPIO21

R688 10K 0402 5%

+3VS

R674 4.7K 0402 5%

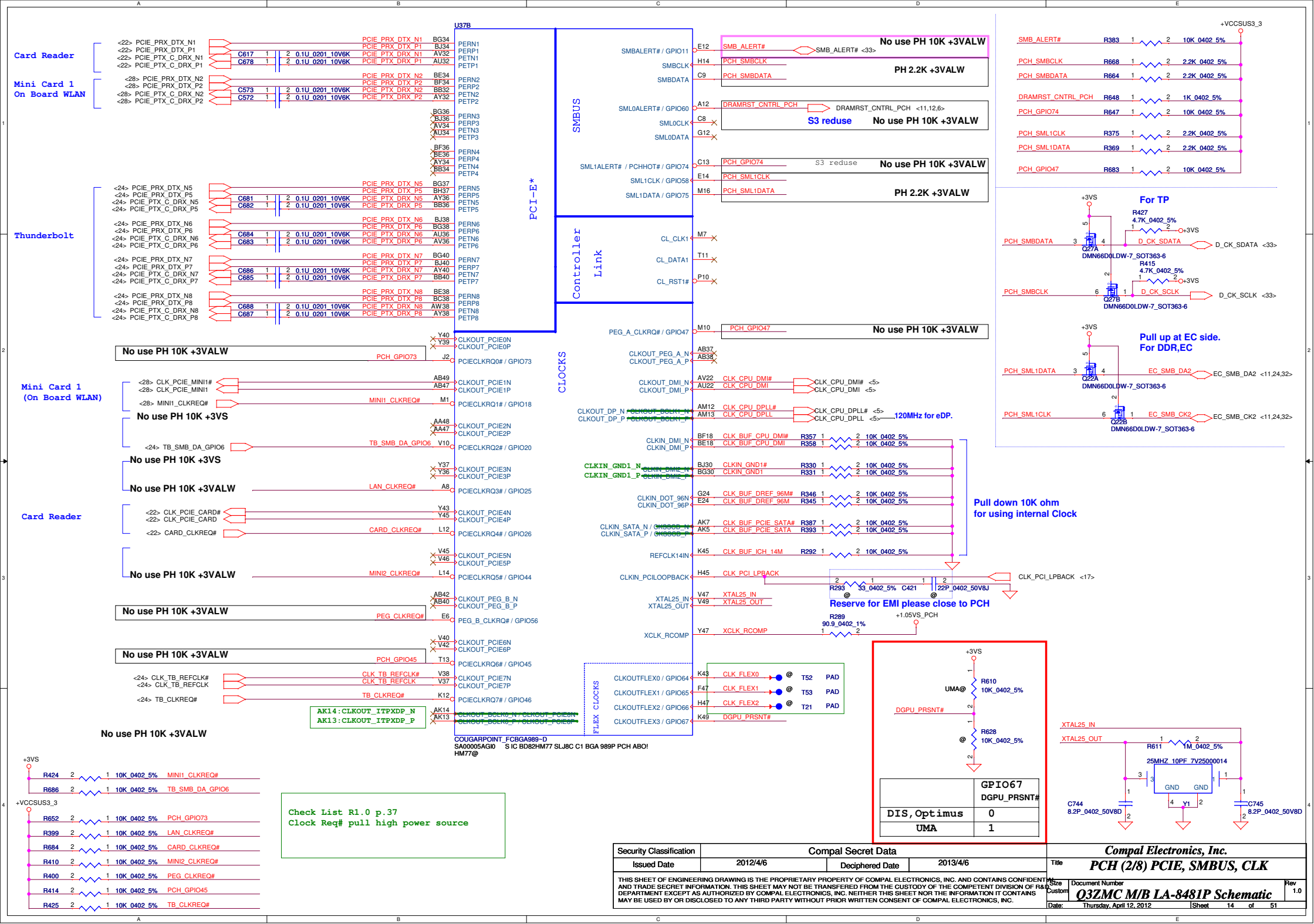
PCH\_GPIO19

Debug Port DG 1.2 PH 4.7K +3VS

Boot BIOS Strap

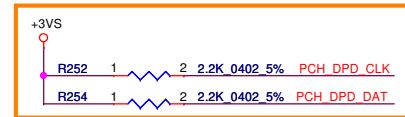
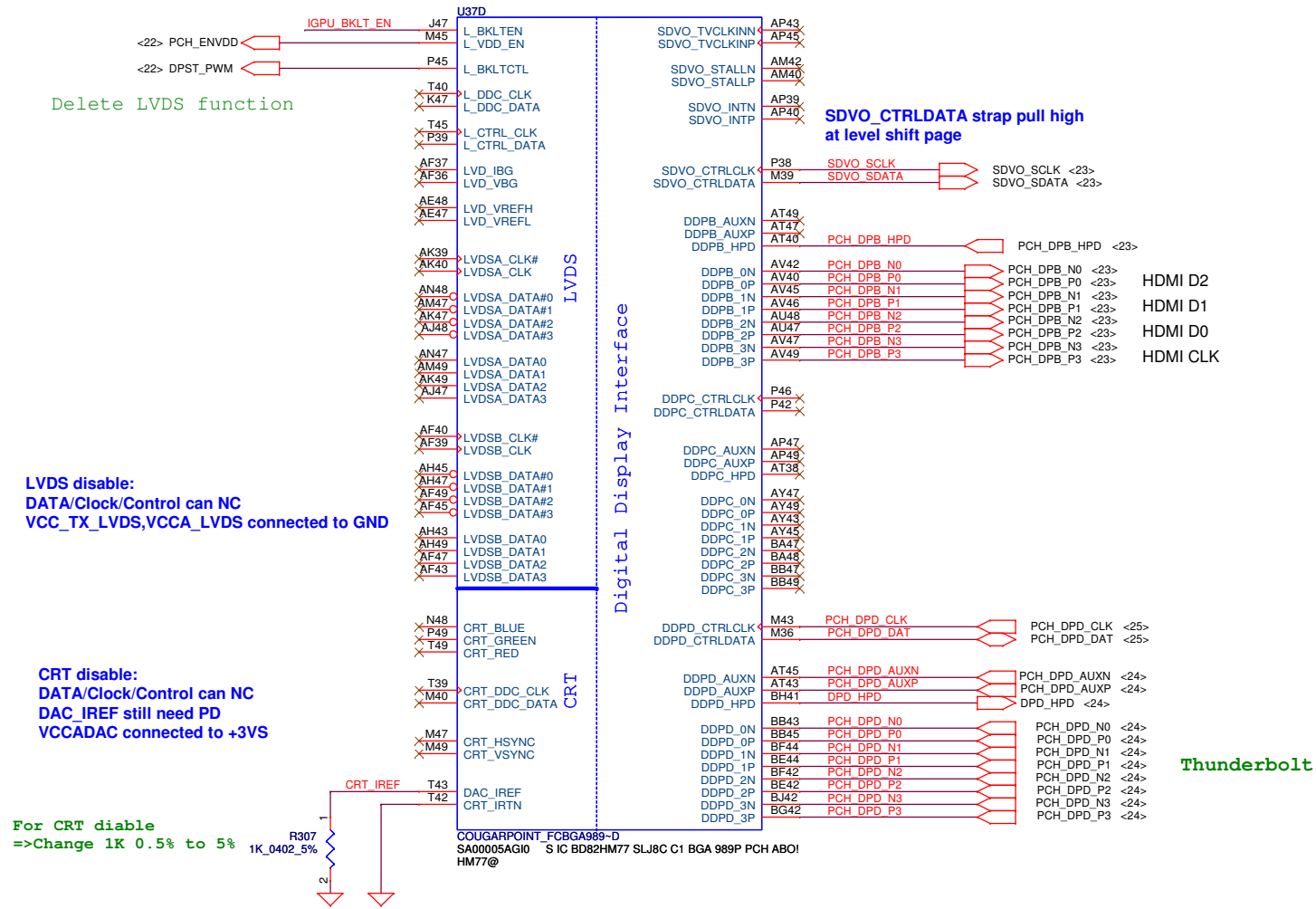
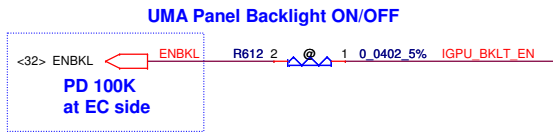
Boot BIOS	GPIO51	GPIO19
LPC	0	0
Reserved	0	1
-	1	0
★ SPI	1	1

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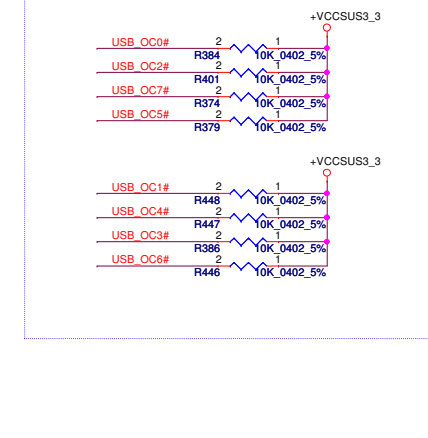






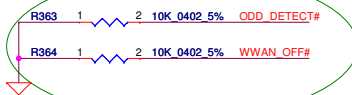
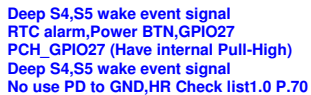
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Size	Document Number	Rev	Date: Thursday, April 12, 2012		
Custom	Q3ZMC M/B LA-8481P Schematic	1.0	Sheet	16	of 51





This signal has a weak internal pull up

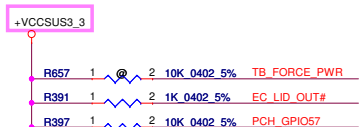
- \* H : On-Die PLL voltage regulator enable
- L : On-Die PLL Voltage Regulator disable



1. Used as for Mechanical Presence detect -  
Use a weak external pull-up (150K-200k Ohms) to Vcc3\_3  
or use 10K external pull-up that is enabled only  
after PLTRST# de-assertion.

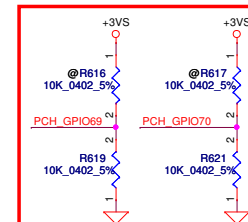
2.Used as GP Input (Pin HW default) -  
Ensure GPI is not driven high during strap sampling window

3.Unused as GPIO or SATA\*GP -  
Use 8.2K-10K pull-down to ground.

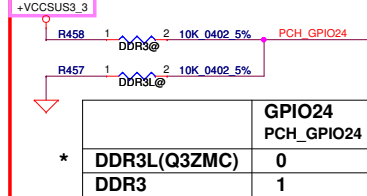
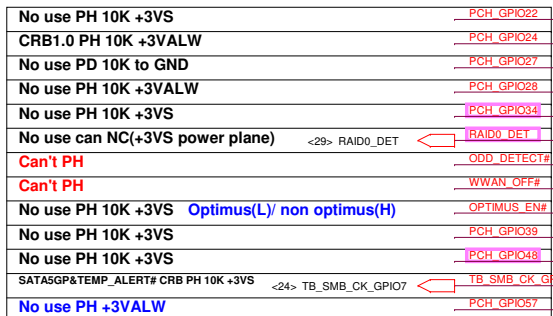


**GPIO24 Unmultiplexed**  
**NOTE:** GPIO24 configuration register bits are not cleared by CF9h reset event.  
**CRB1.0 PH10K to +3VALW**

For eDP only,  
不判斷eDP or LVDS



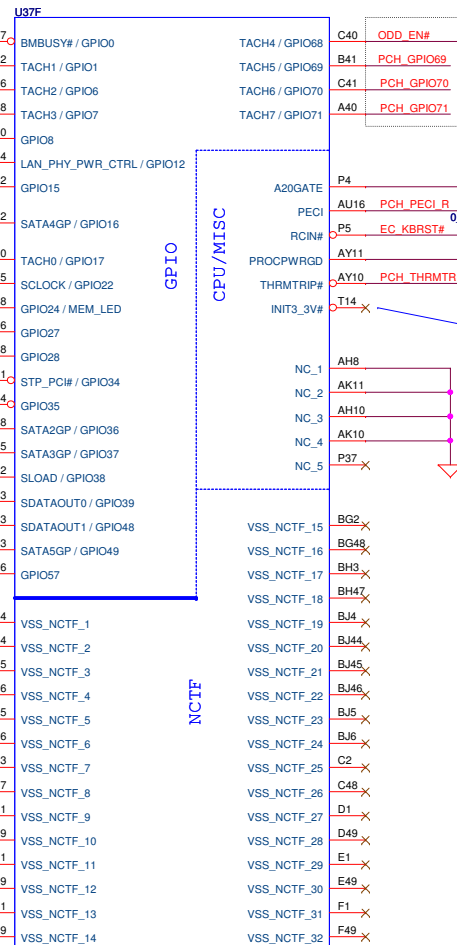
Project ID	GPIO69	GPIO70
* x	0	0
x	0	1
x	1	0
x	1	1



```

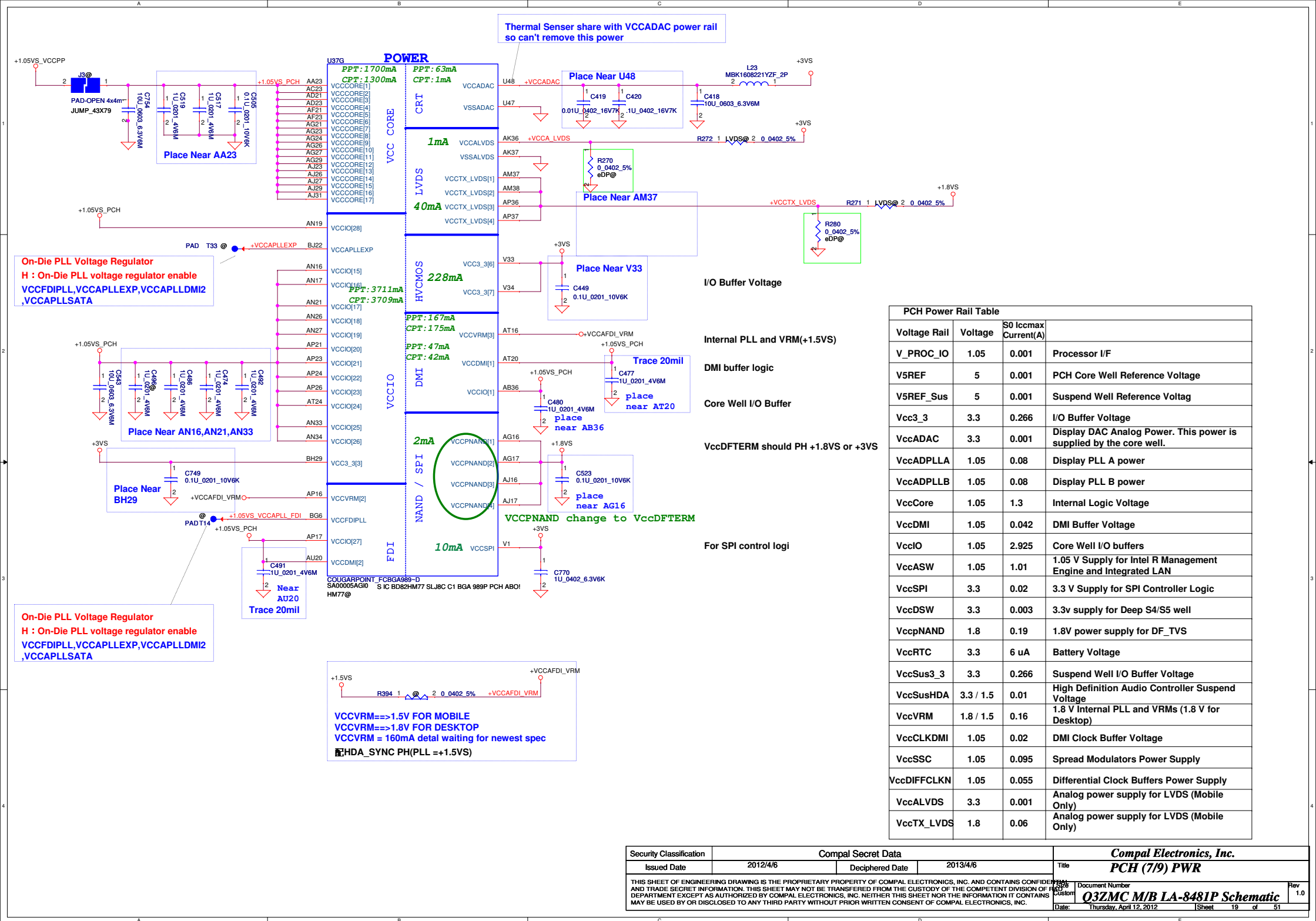
GPIO36/GPIO37 inStrap functionality
that requires internal pull down to be sampled at rising PWROK.
When used as SATA2GP/SATA3GP for mechanical presence detect
-use an external pull up 150K-200K ohm to Vcc3_3
When used as GP input
-ensure GP is not driven high during strap sampling window
When Unused as GPIO or SATA*GP
-use 8.2K-10K pull-down
check list page 47

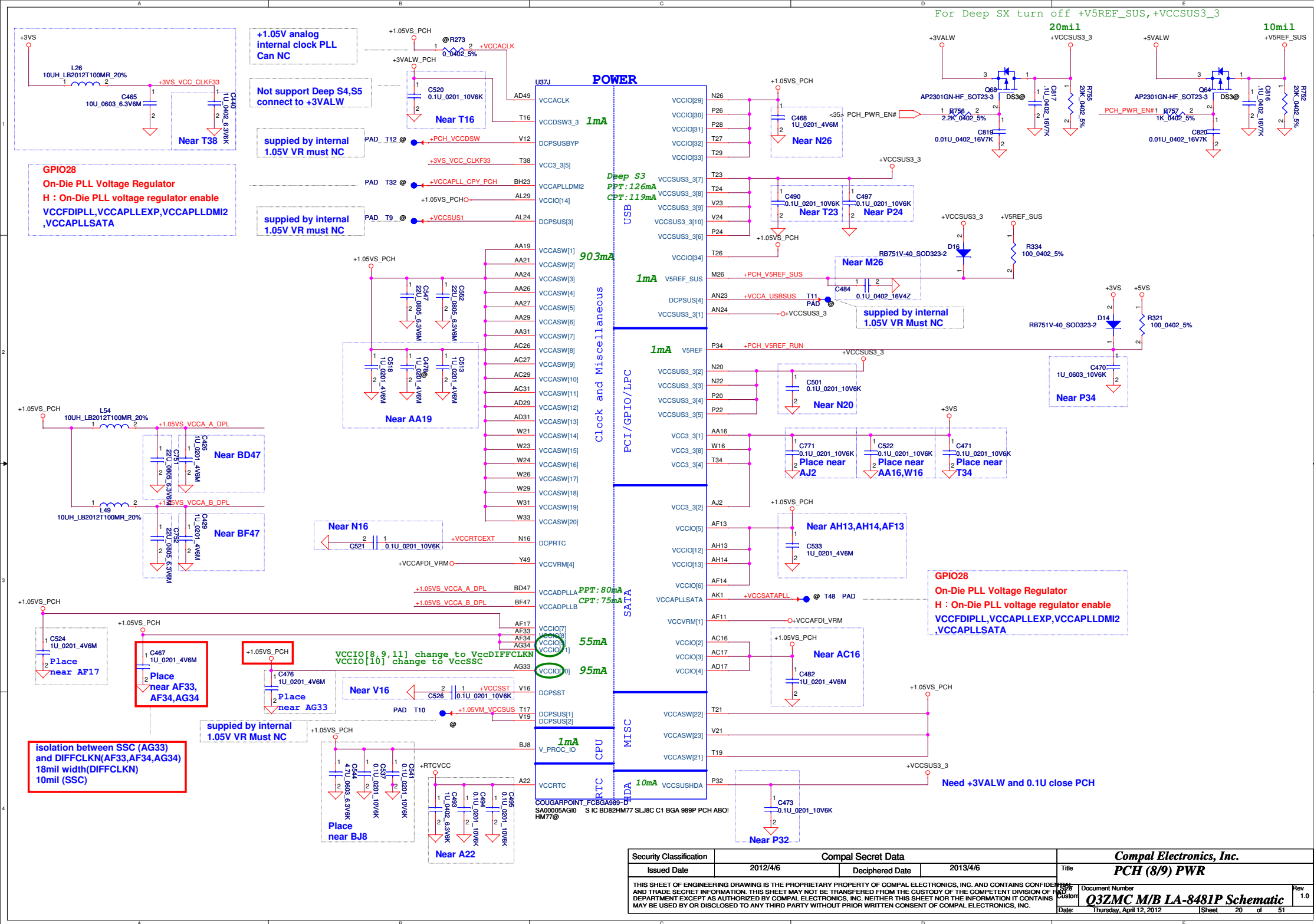
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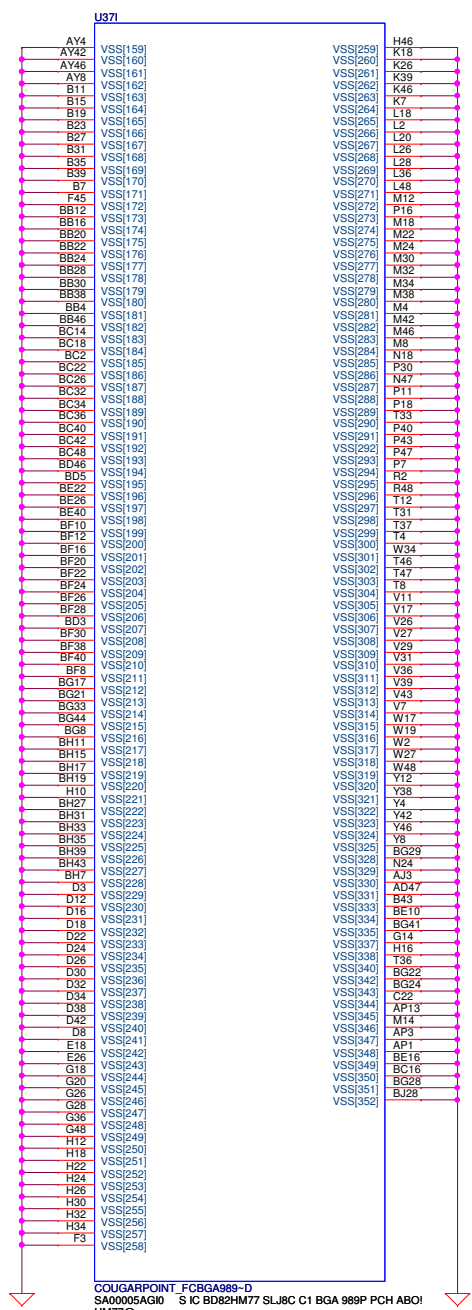
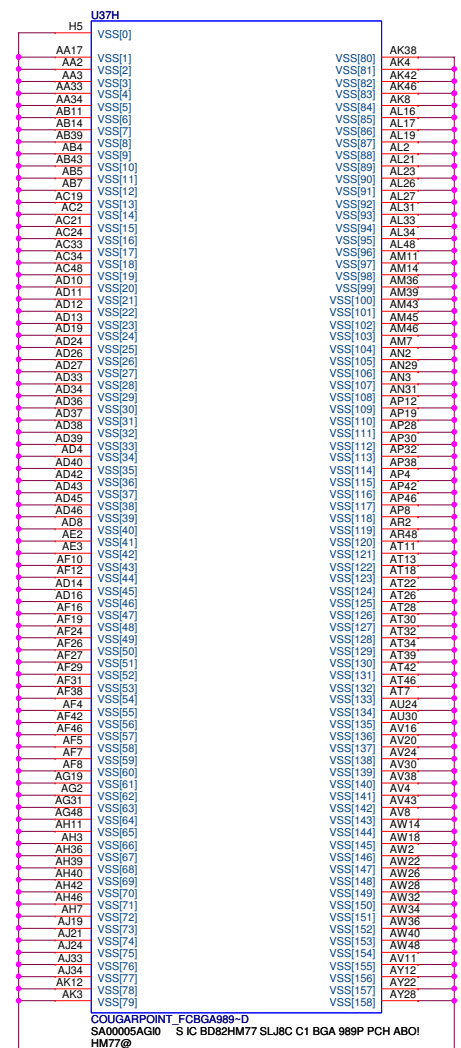


Remove NCTF test point  
2011/9/23

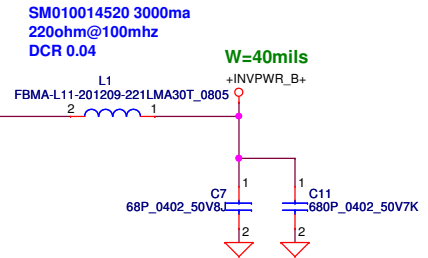
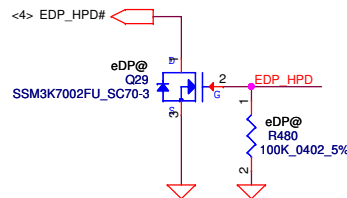
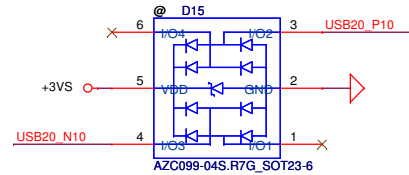
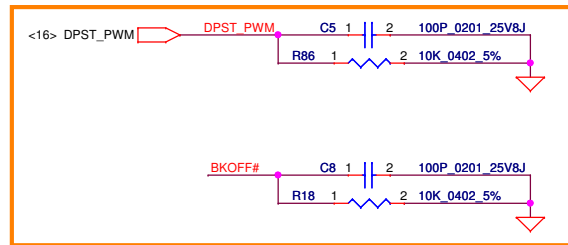
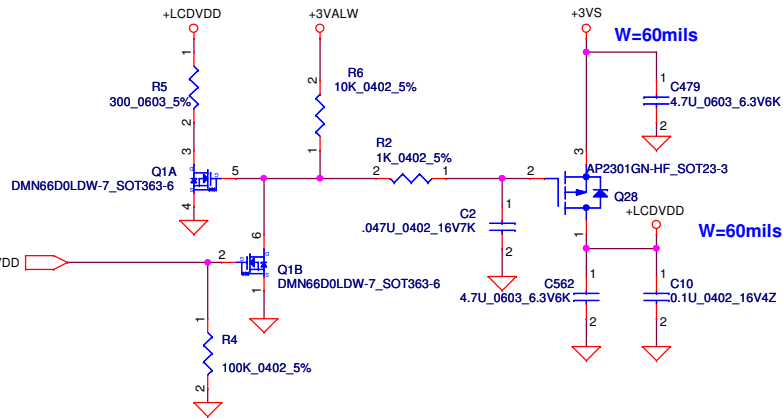
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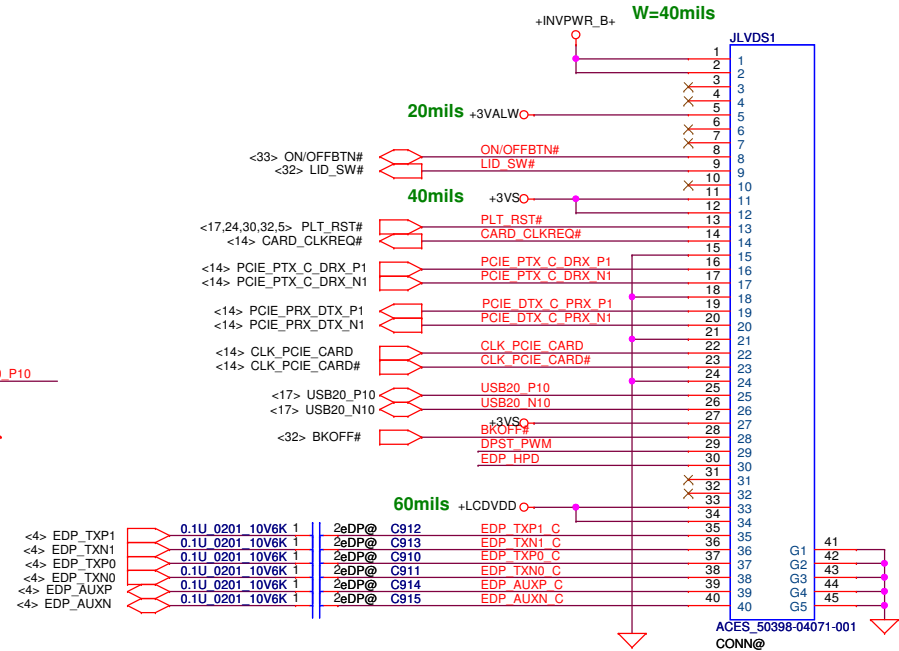




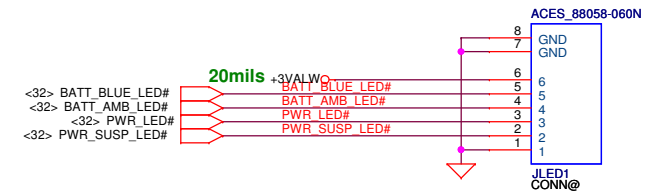
# Panel POWER CIRCUIT



## eDP panel + Card Reader Conn.

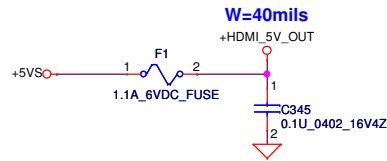


## To LED/B Conn.

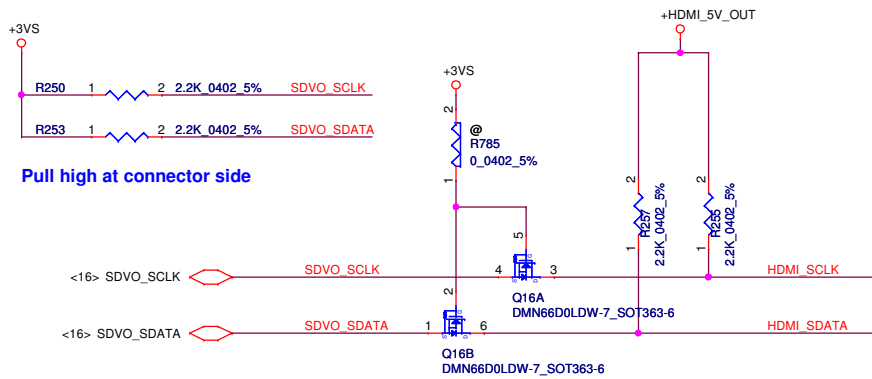


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					Customer Q3ZMC M/B LA-8481P Schematic
					Rev 1.0
					Date: Thursday, April 12, 2012
					Sheet 22 of 51

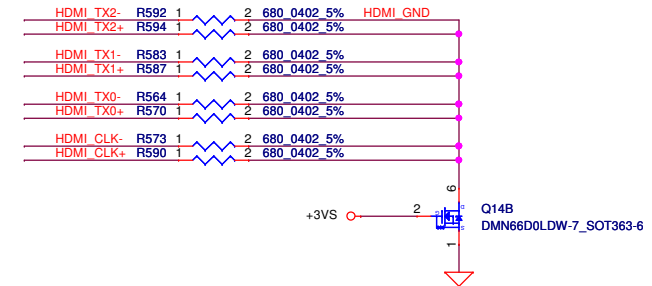
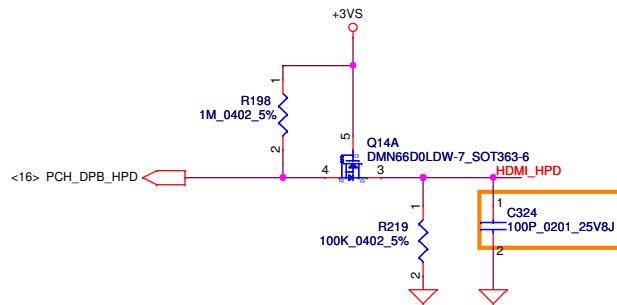




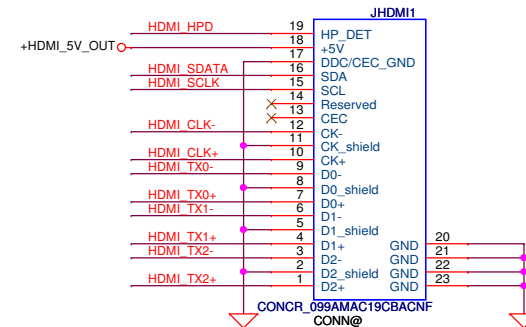
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<16> PCH_DPB_P0	C281	2	1	.1U_0402_16V7K	HDMI TX2+
<16> PCH_DPB_N1	C283	2	1	.1U_0402_16V7K	HDMI TX1-
<16> PCH_DPB_P1	C282	2	1	.1U_0402_16V7K	HDMI TX1+
<16> PCH_DPB_N2	C287	2	1	.1U_0402_16V7K	HDMI TX0-
<16> PCH_DPB_P2	C286	2	1	.1U_0402_16V7K	HDMI TX0+
<16> PCH_DPB_N3	C285	2	1	.1U_0402_16V7K	HDMI CLK-
<16> PCH_DPB_P3	C284	2	1	.1U_0402_16V7K	HDMI CLK+



**Place close to JHDMI1**



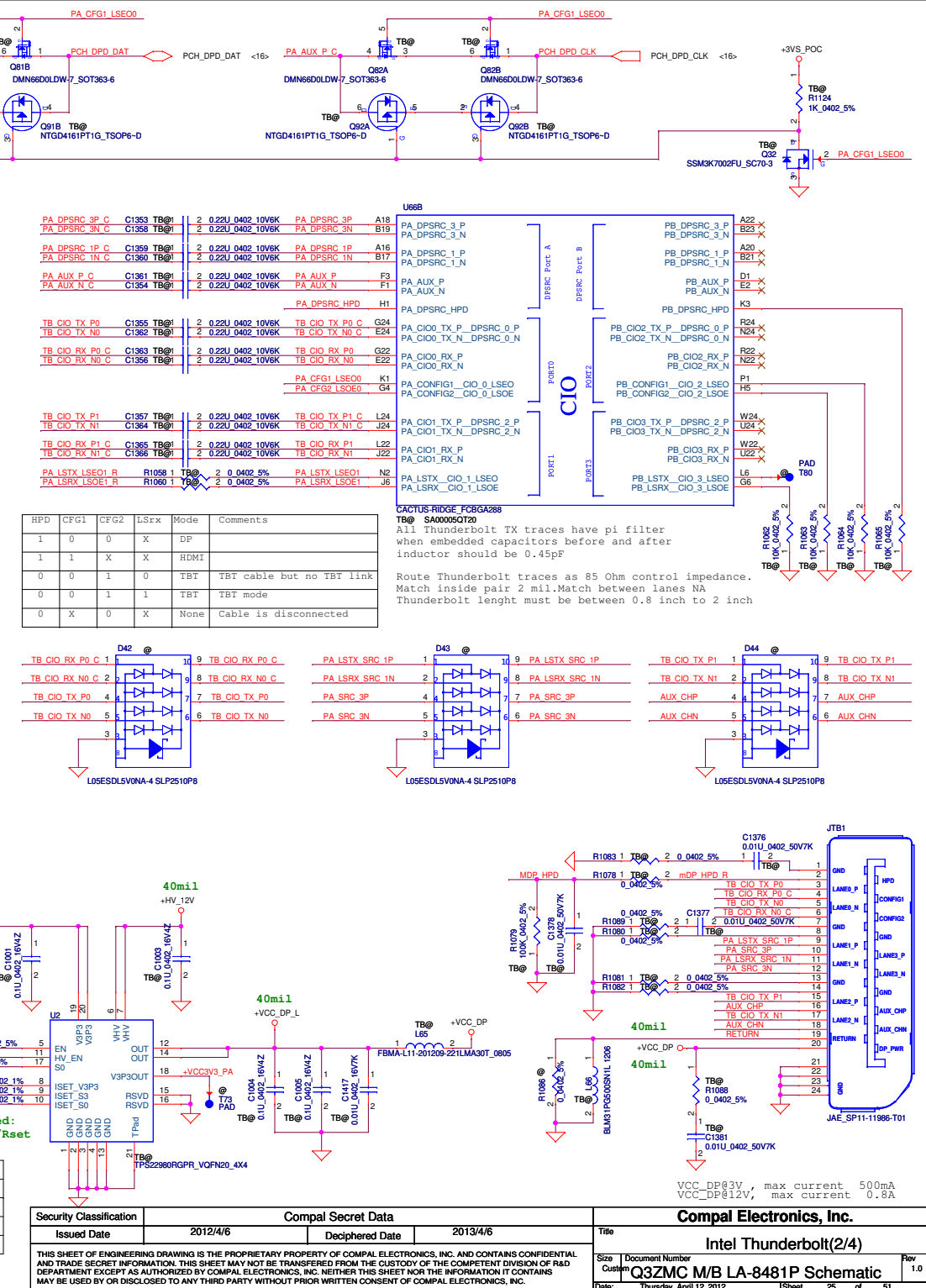
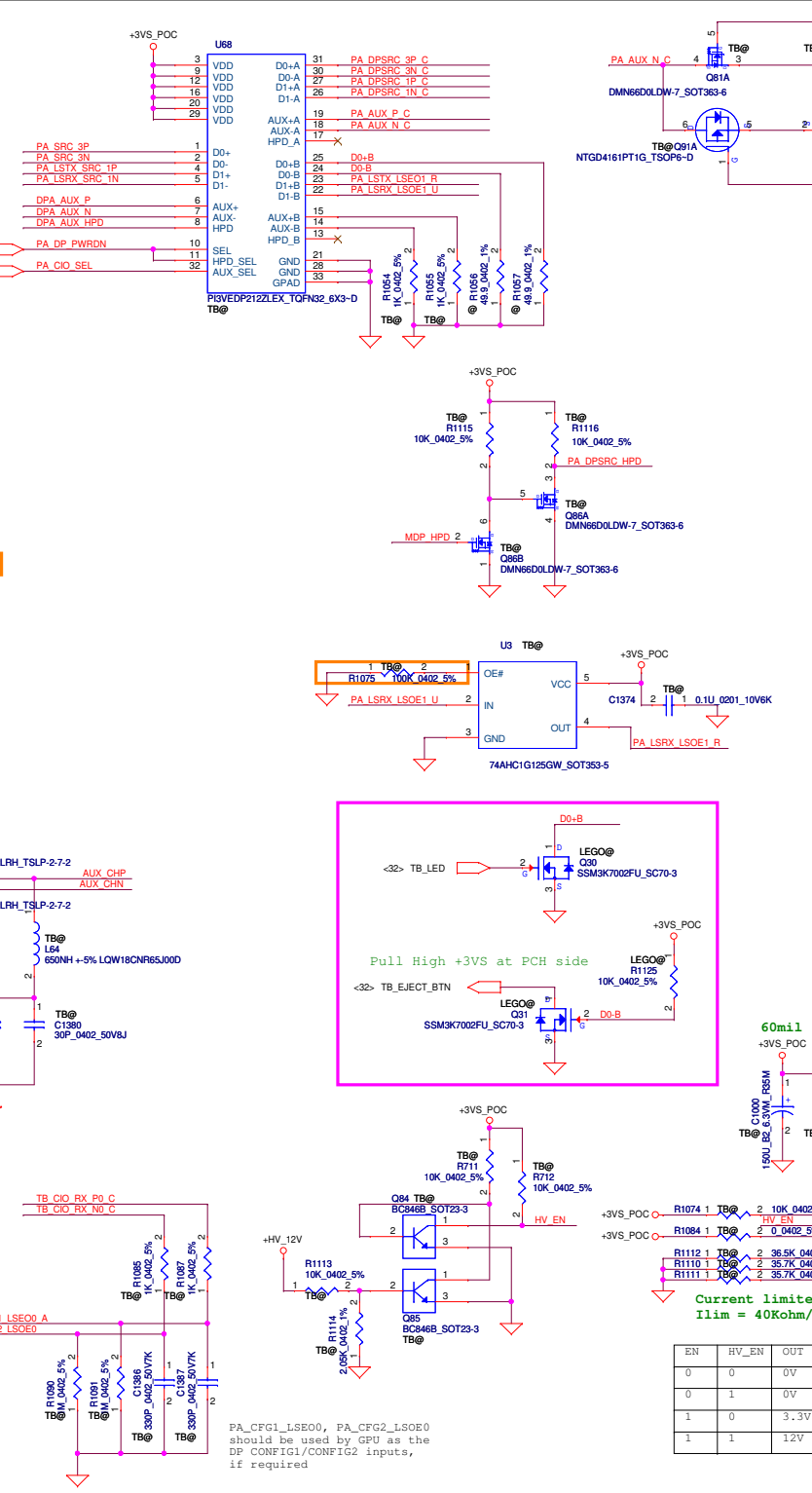
### HDMI connector

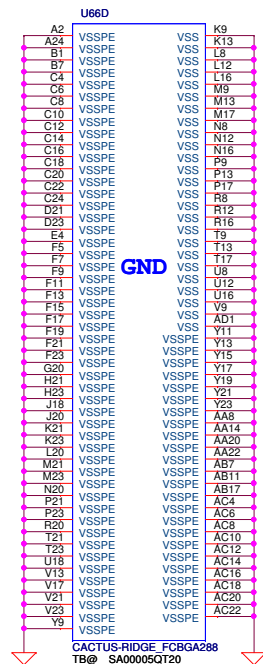


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				Date:	Thursday, April 12, 2012	Sheet 23 of 51

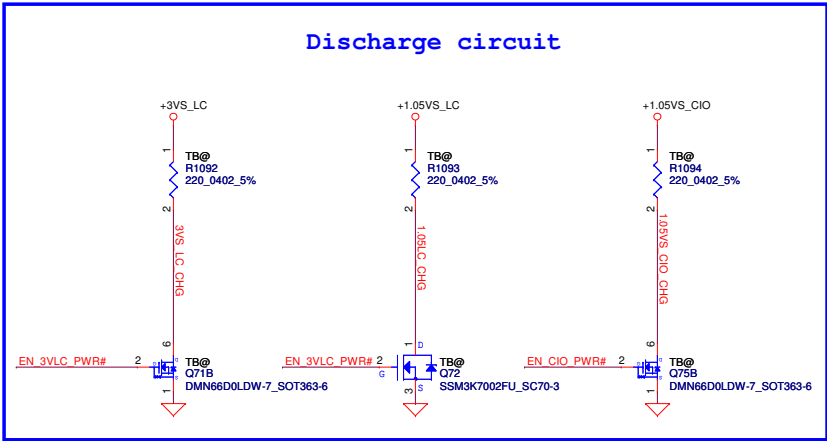
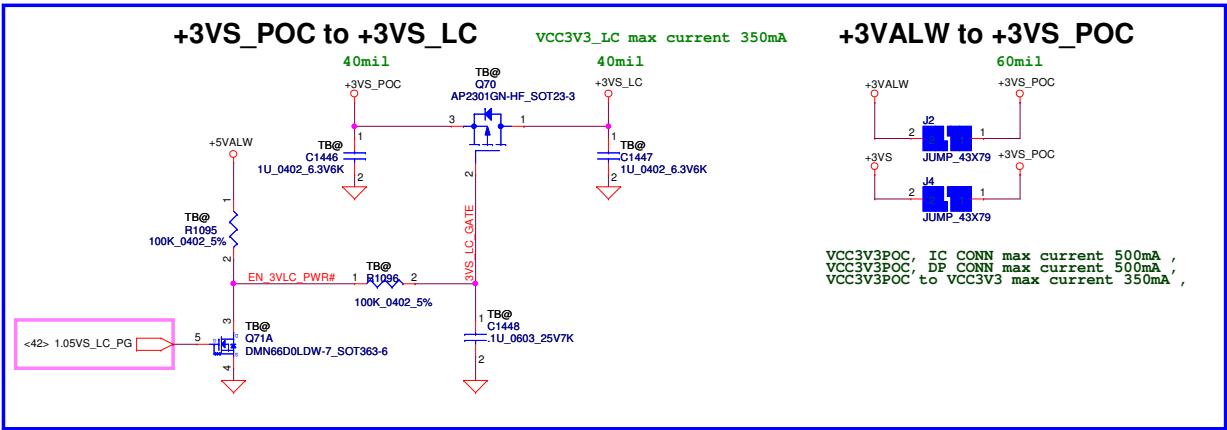




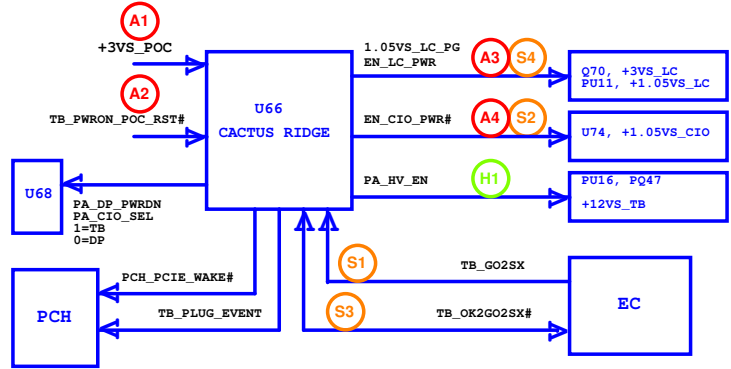
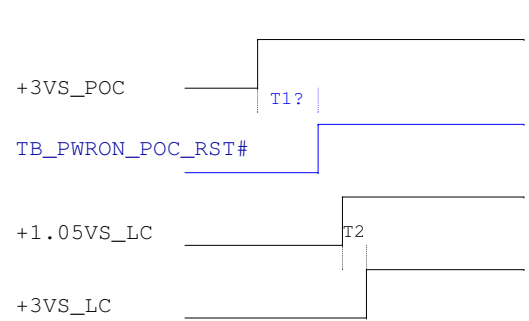
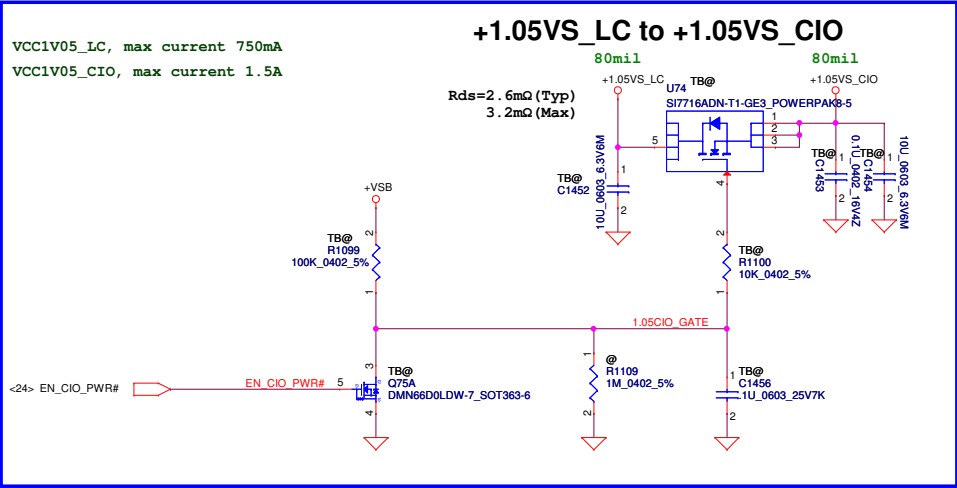
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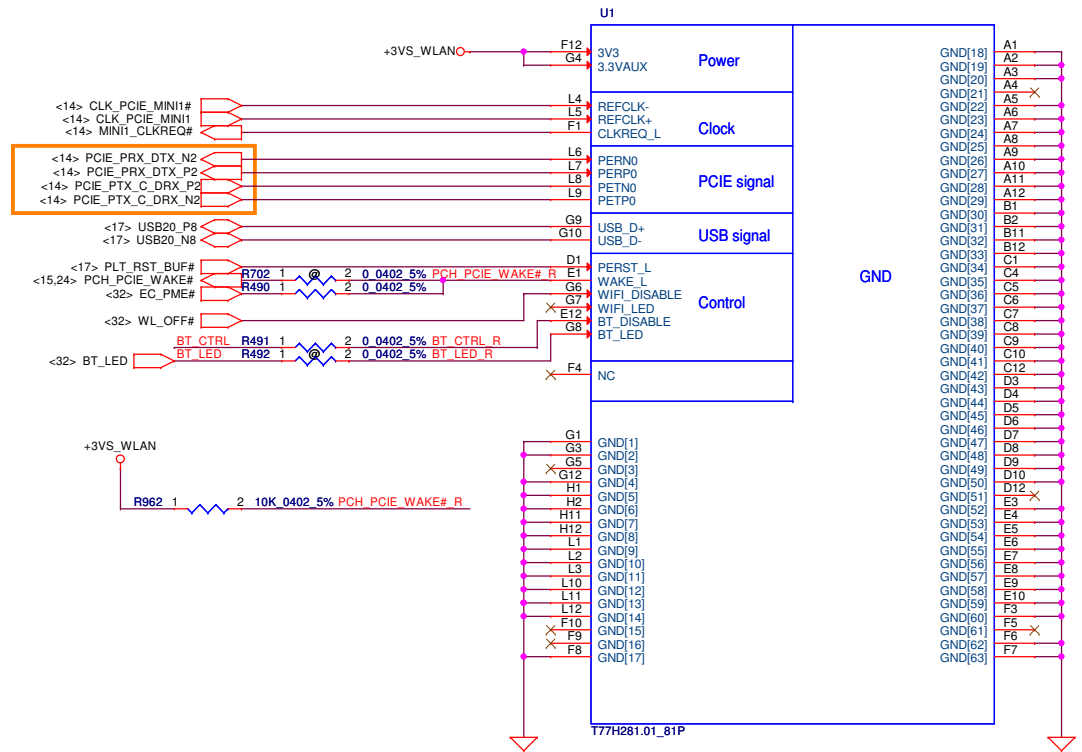
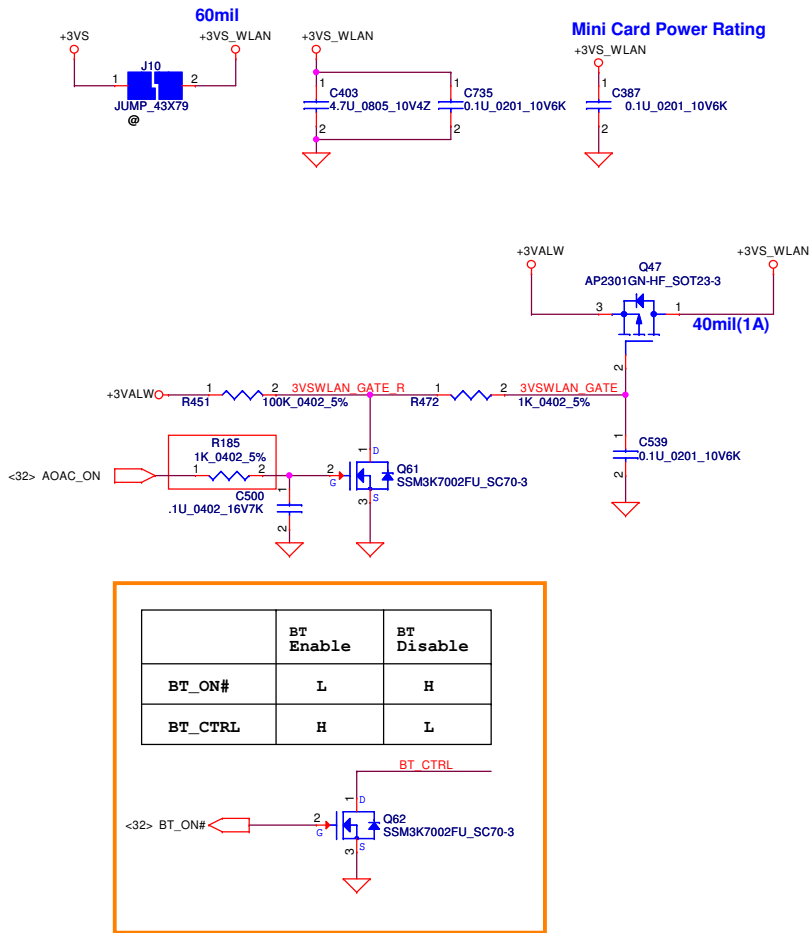
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				Customer	1.0	
Date: Thursday April 12 2012				JSheel	26	of 51



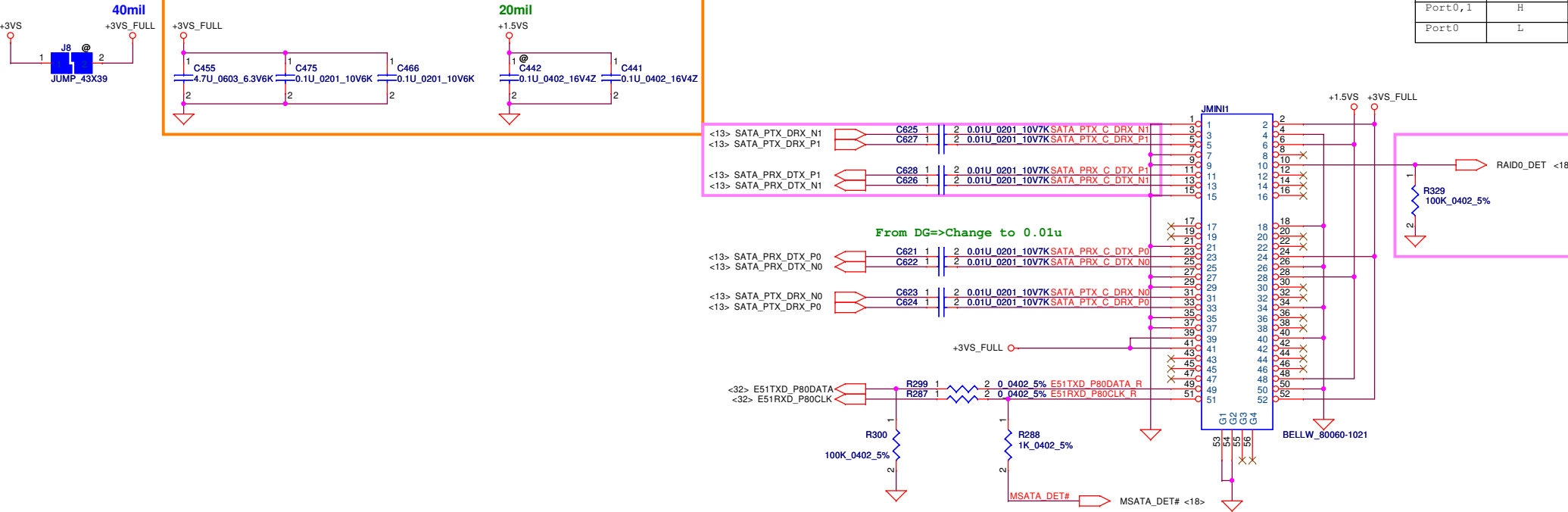
\_VCC1V05\_LC,max current 750mA  
\_VCC1V05\_CIO,max current 1.5A  
\_VCC3V3POC,max current 5mA  
\_VCC3V3\_LC,max current 350mA  
\_VCC\_DP@3V,max current 500mA  
\_VCC\_DP@12V,max current 0.8A  
in the case of 12V min power should be 10W



# For Wireless LAN

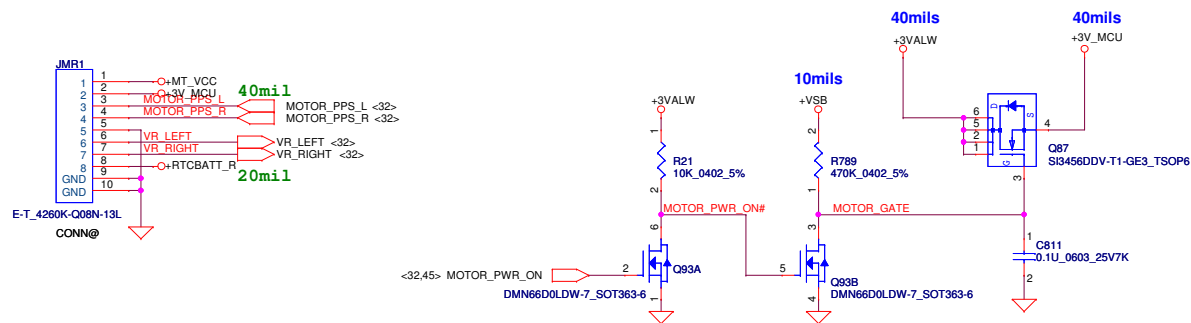


For mSATA

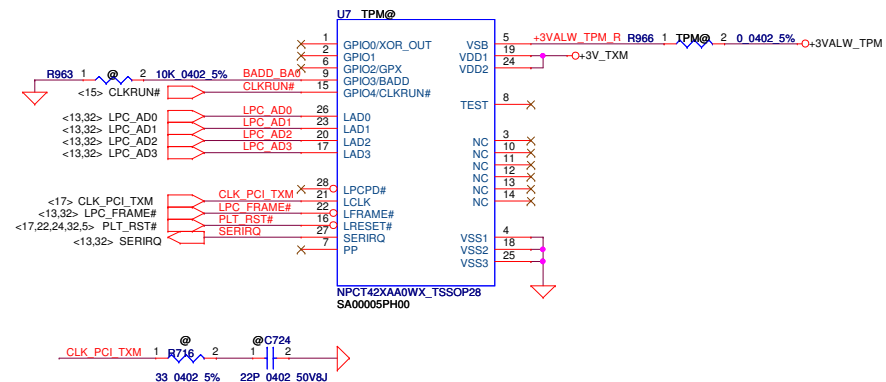
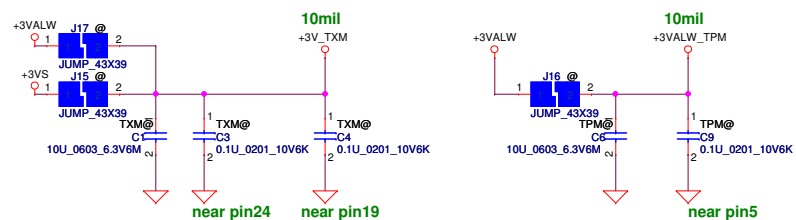


Function	RAID0_DET
Port0,1	H
Port0	L

## MOTOR/RTC

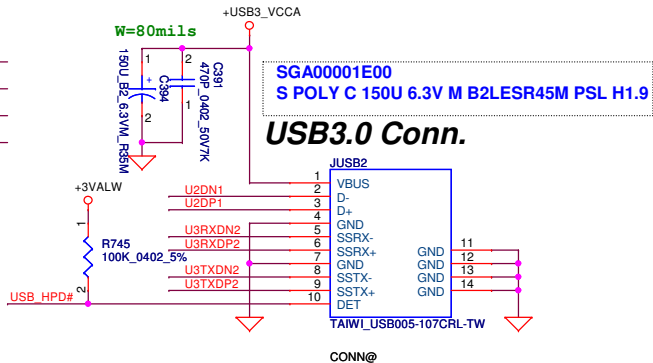
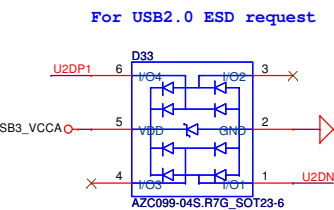
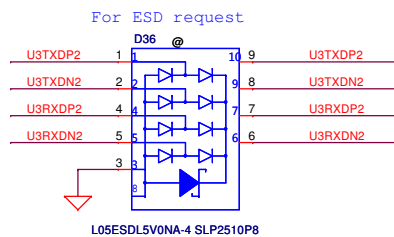
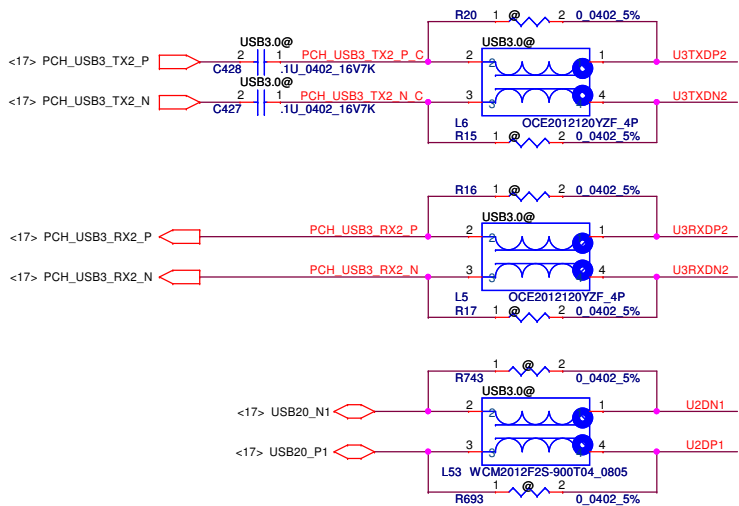
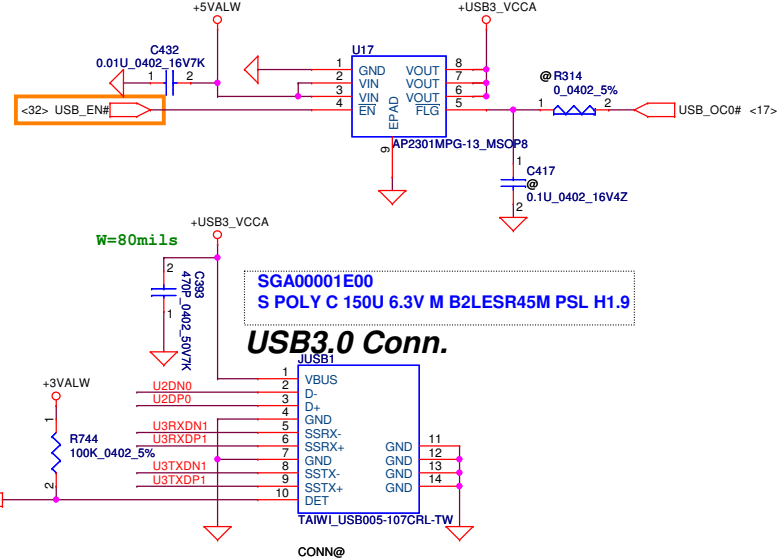
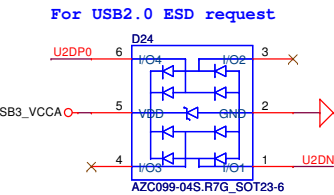
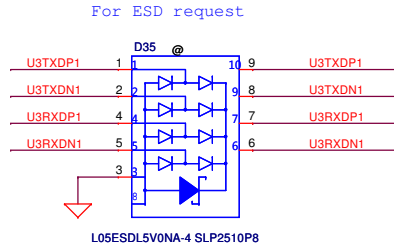
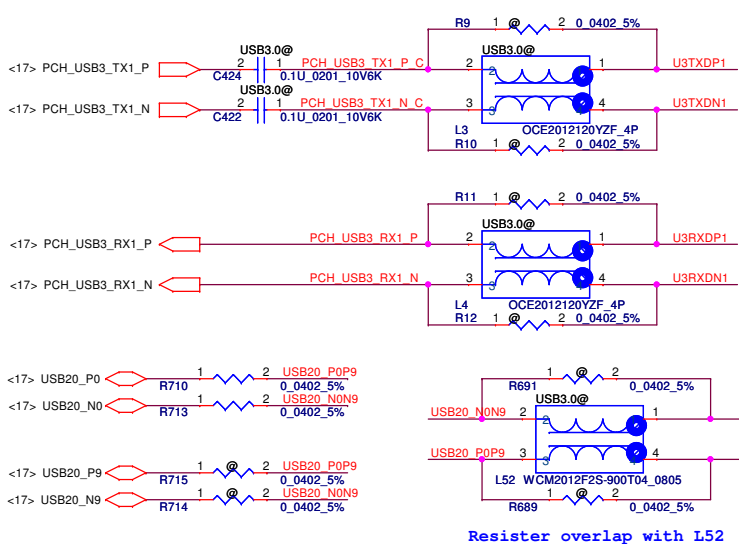


# TPM

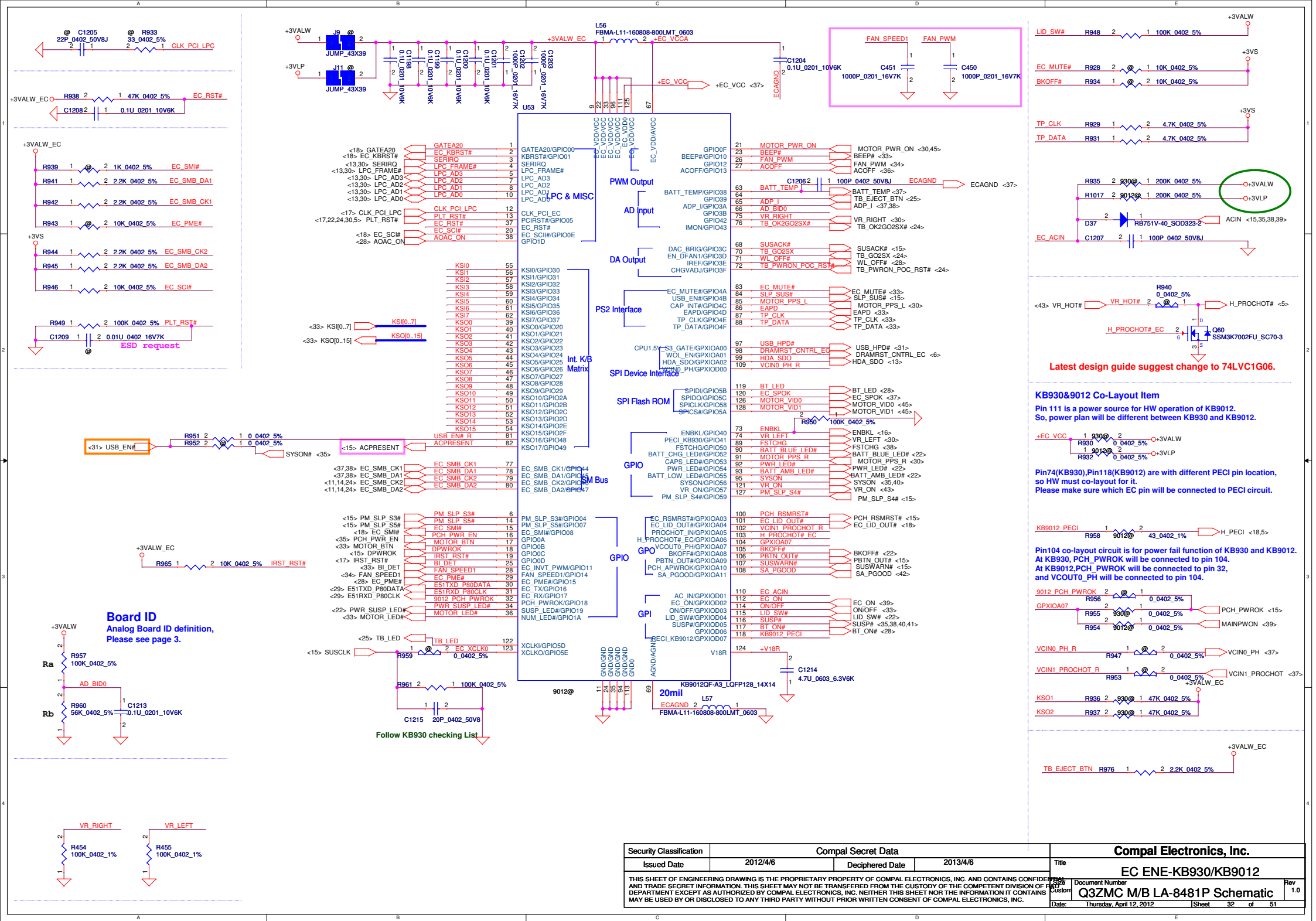


**TPM -Address:**  
**Pin9 BADD**  
**1: 7Eh-7Fh (Default)**  
**0: EEh-EFh**

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				Rev	1.0	
				Date:	Thursday, April 12, 2012	Sheet 30 of 51

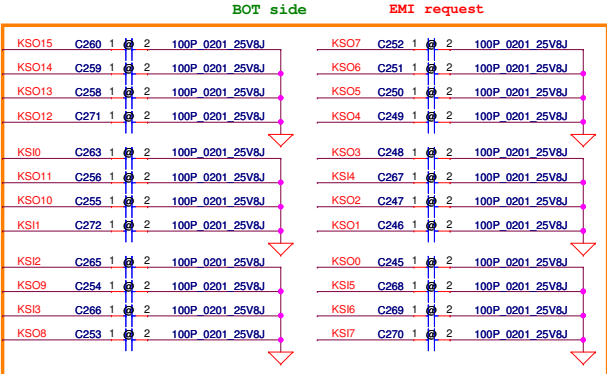
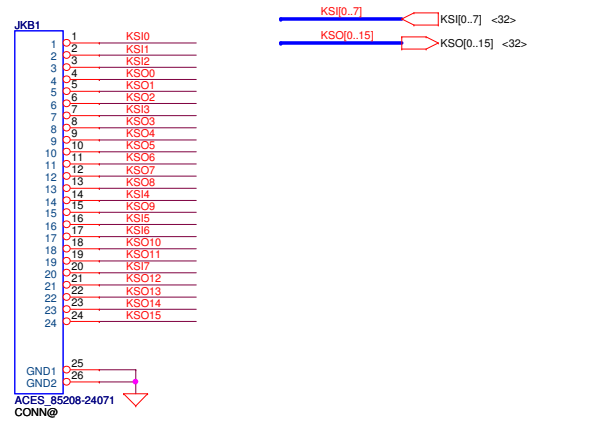


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				Q3ZMC M/B LA-8481P Schematic	
				Date:	Thursday, April 12, 2012
				Sheet	31 of 51
				Rev	1.0

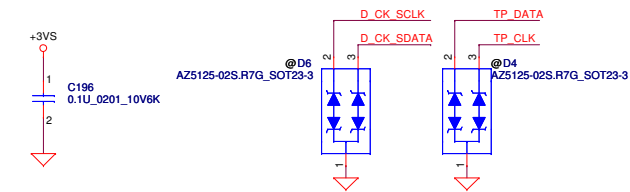
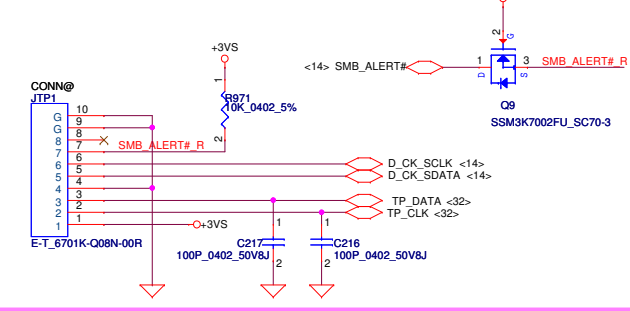




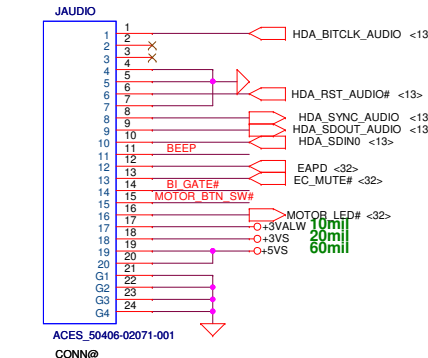
KB Conn.



TP Conn.

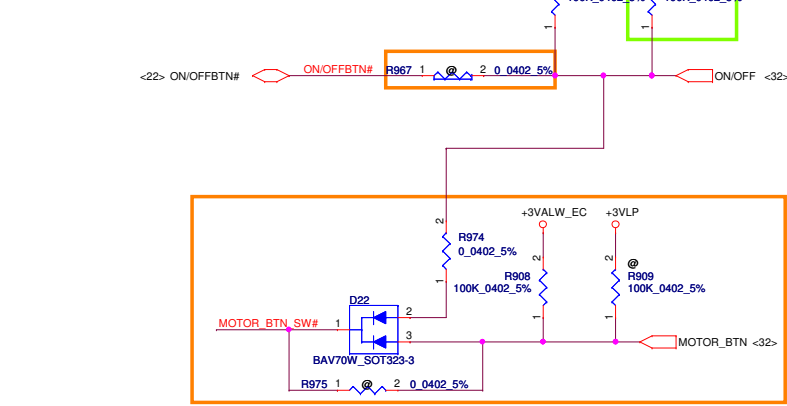


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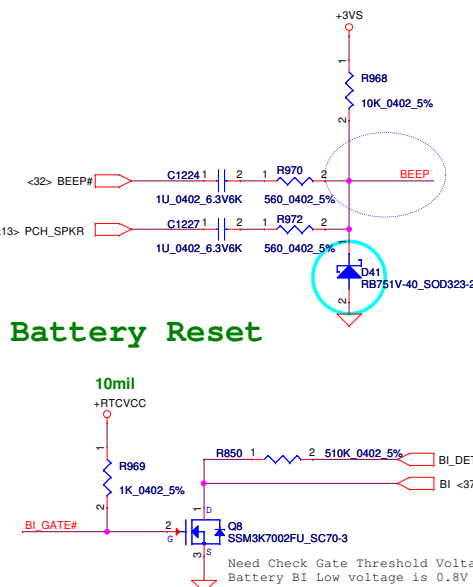


ON/OFF BTN

Motor BTN

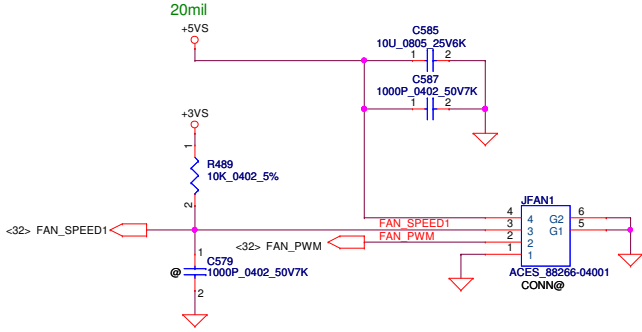


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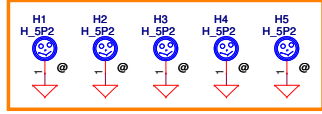


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								Customer		Document Number		Rev	
								Q3ZMC M/B LA-8481P Schematic		Date		Sheet	
								Thursday, April 12, 2012		33		of 51	

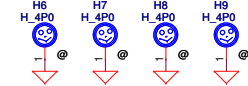
## FAN Conn



## Stand-Off



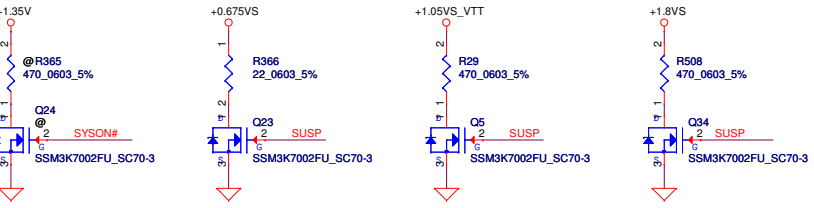
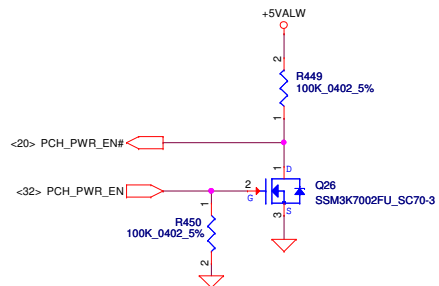
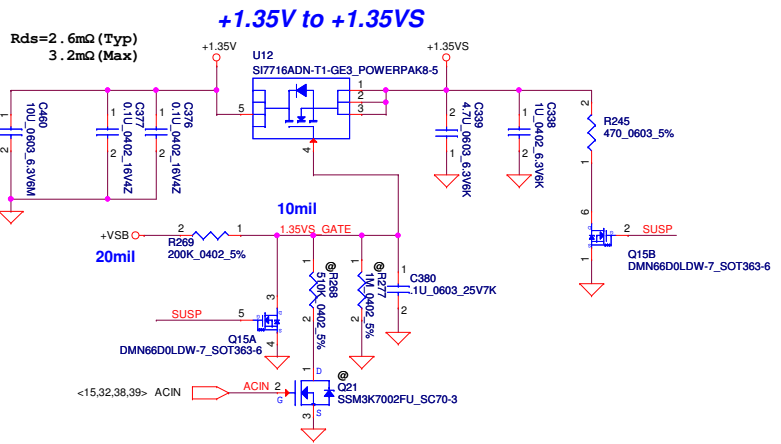
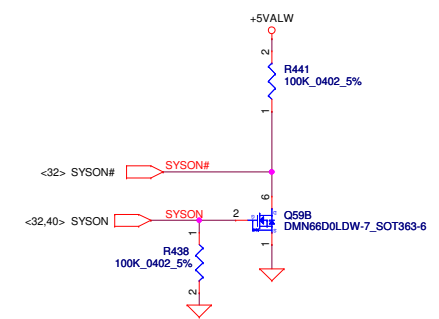
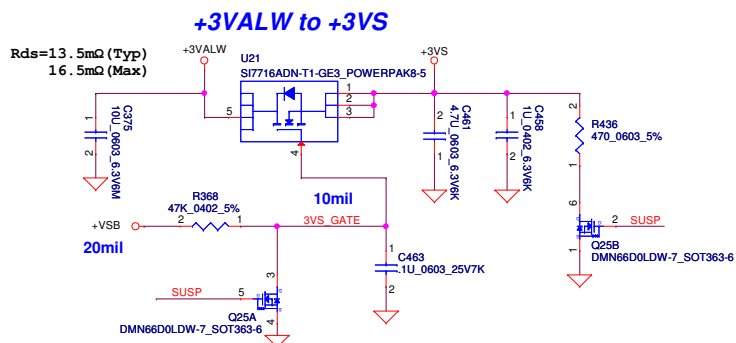
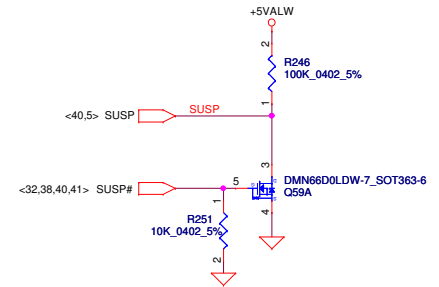
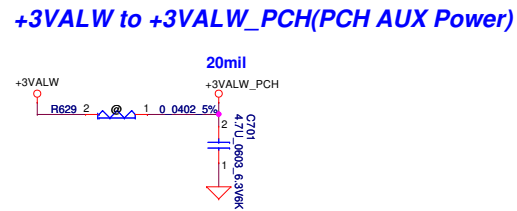
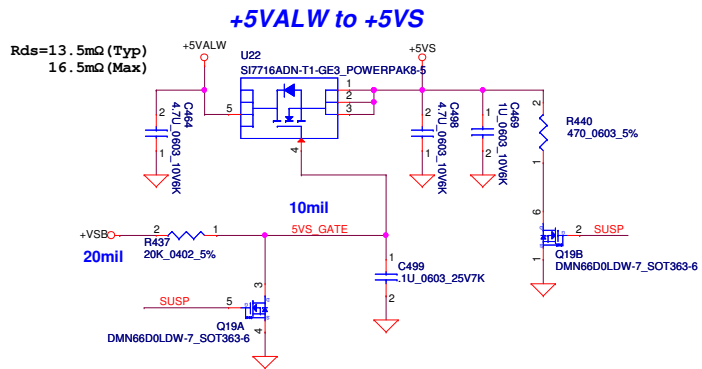
## Thermal module



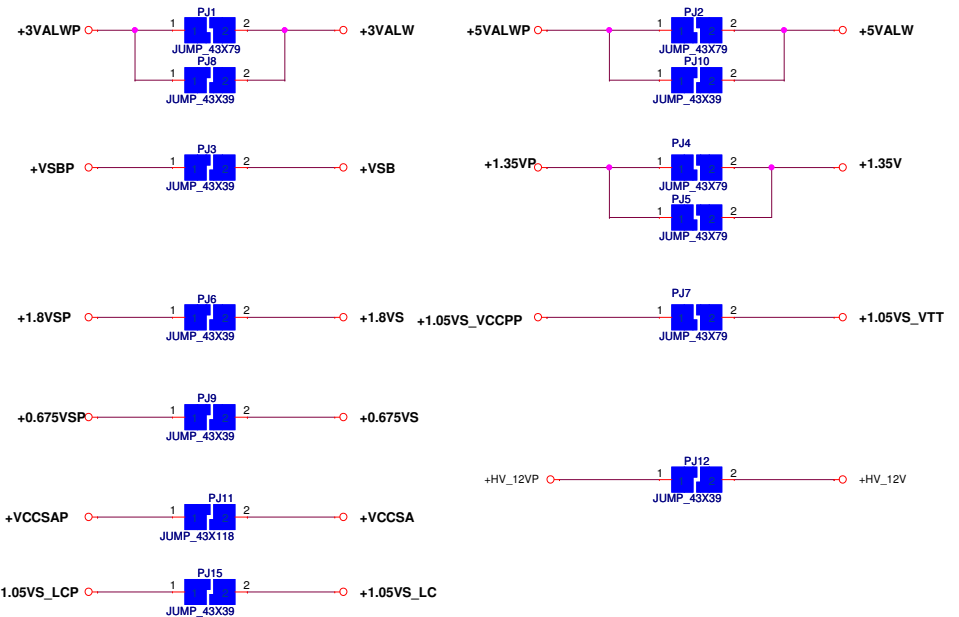
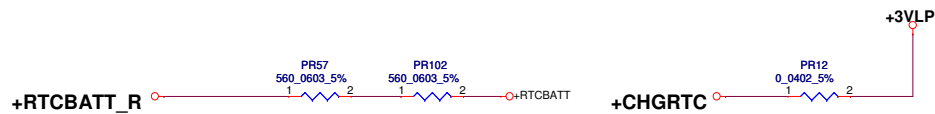
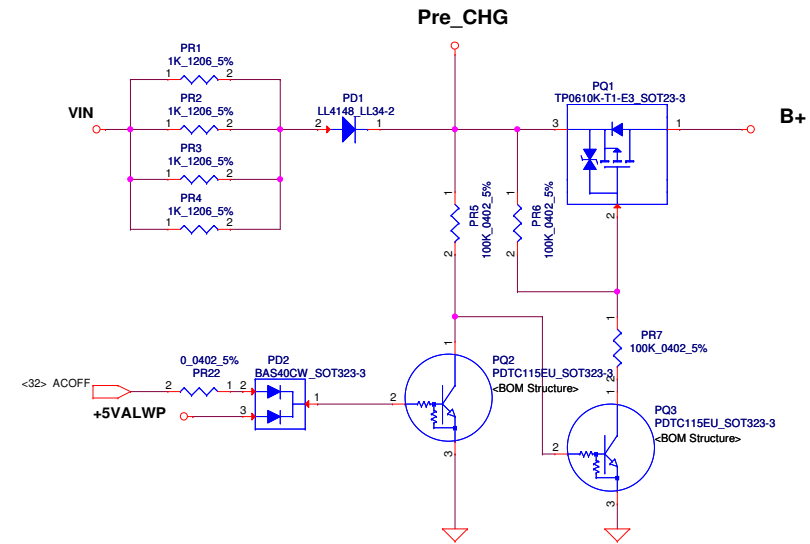
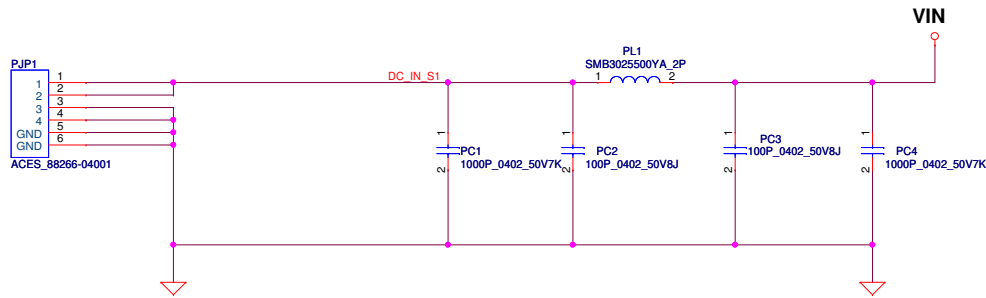
**定位孔**



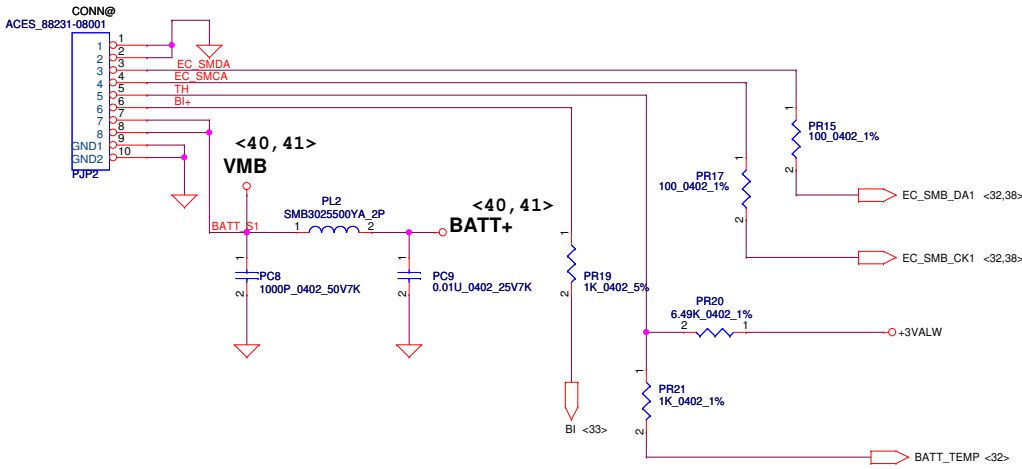
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						Step Motor, FAN, Screw Hole
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						Customer
						Q3ZMC M/B LA-8481P Schematic
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						Q3ZMC M/B LA-8481P Schematic		Thursday, April 12, 2012		Sheet 35 of 51	

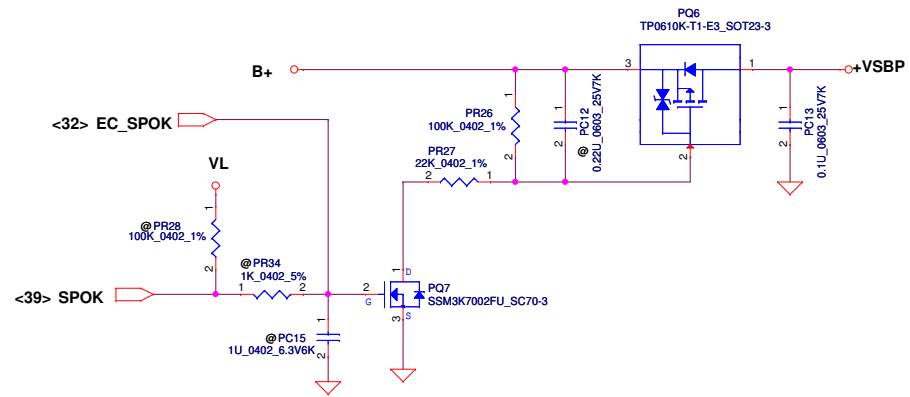
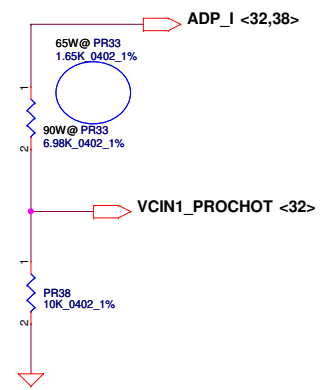


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				Date:	Thursday, April 12, 2012
				Sheet	36 of 51
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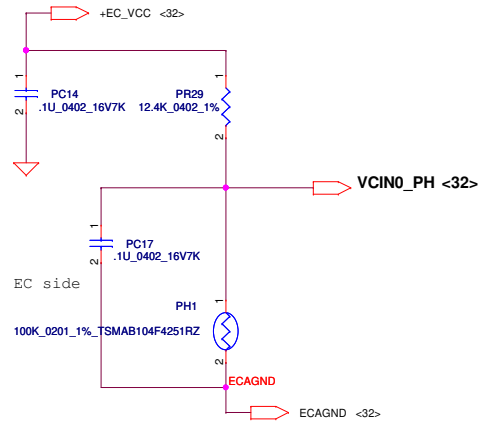


For 65W adapter==>action 70W , Recovery 54W  
 For 90W adapter==>action 97W , Recovery 75W  
 For 40W thunder bolt adapter==>action 50W , Recovery 38W  
 VCIN1=0.9V recover = 0.683V

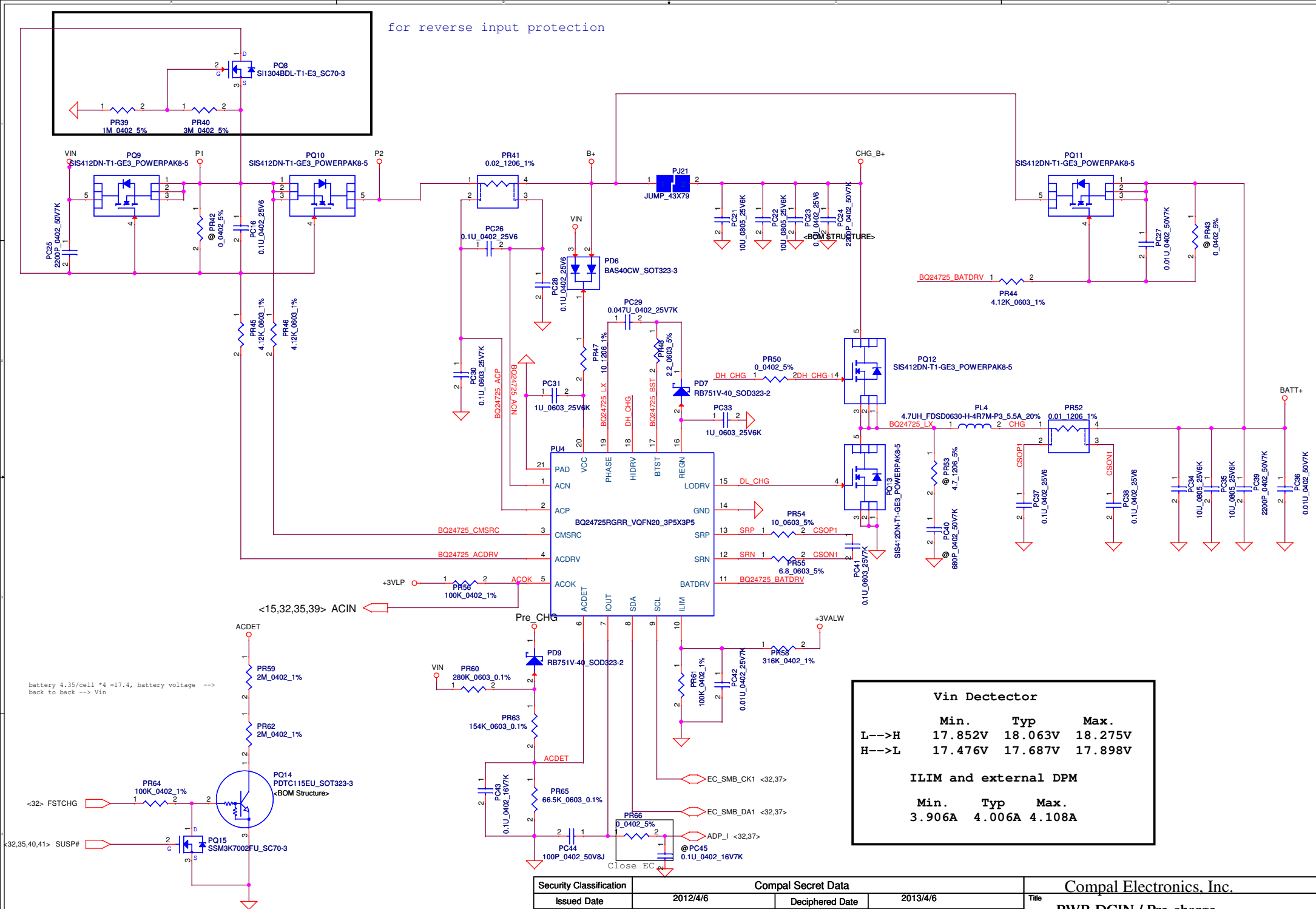
	G718	ENE9012
65W	3.92K	2.21K
90W	8.87K	6.98K
VCIN1	1.456V	1.2V
	1.148V	0.925V



PH1 under CPU botten side :  
 CPU thermal protection at 92 degree C for reference



for reverse input protection



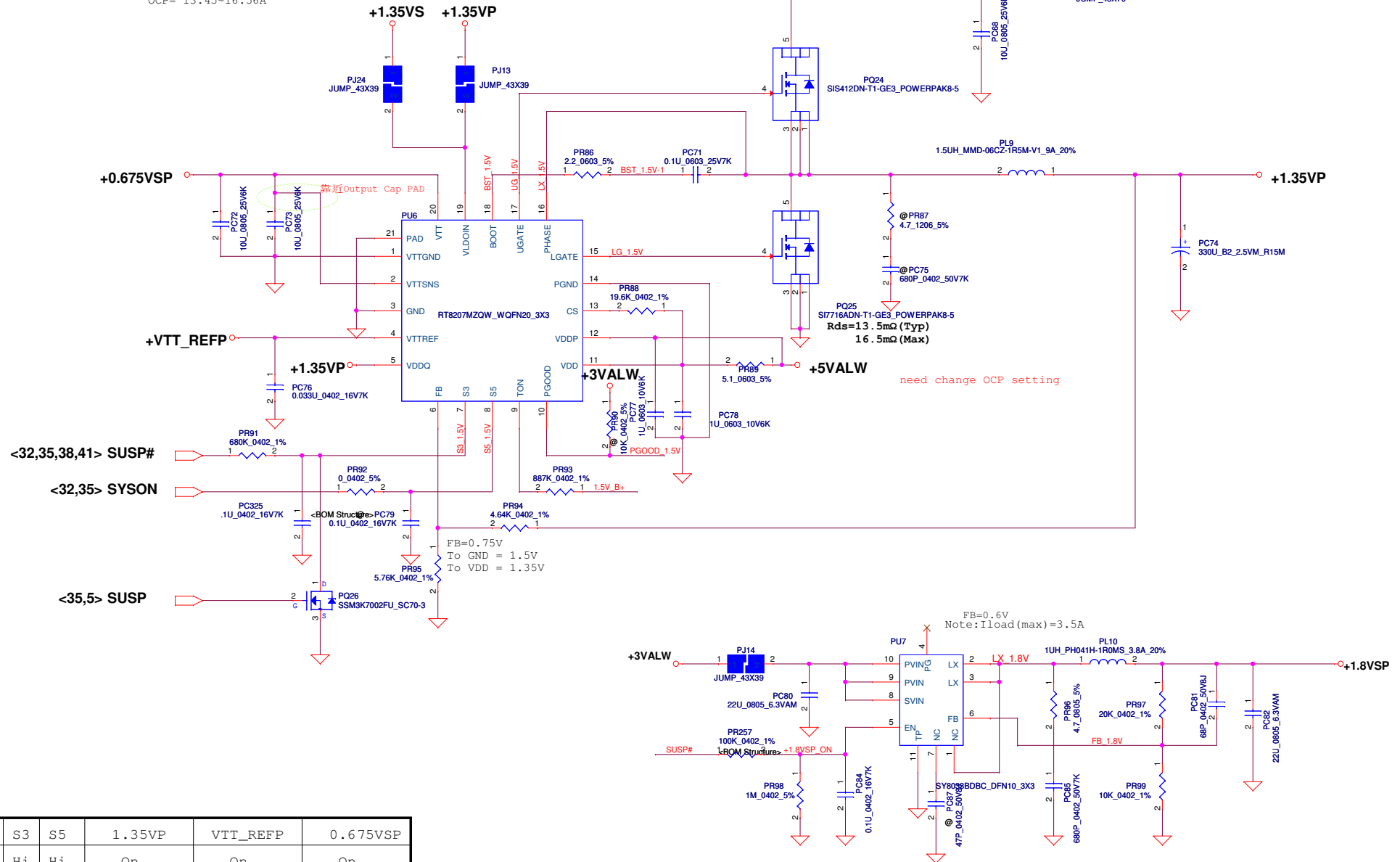
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Issued Date	2012/4/6	Deciphered Date	2013/4/6	Title	PWR DCIN / Pre-charge
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## ACIN



## ACIN

Ipeak = 9.8A, I<sub>max</sub> = 6.86A  
Delta I = 2.88A, F = 290KHz, R<sub>ton</sub> = 887K ohm  
R<sub>trip</sub> = 19.6K ohm  
OCP = 13.45~16.56A



need change OCP setting

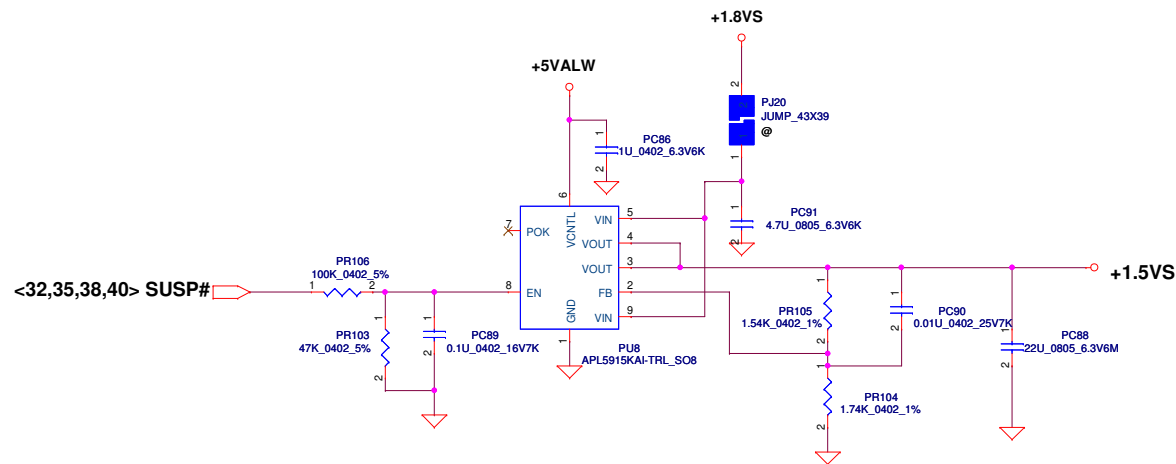
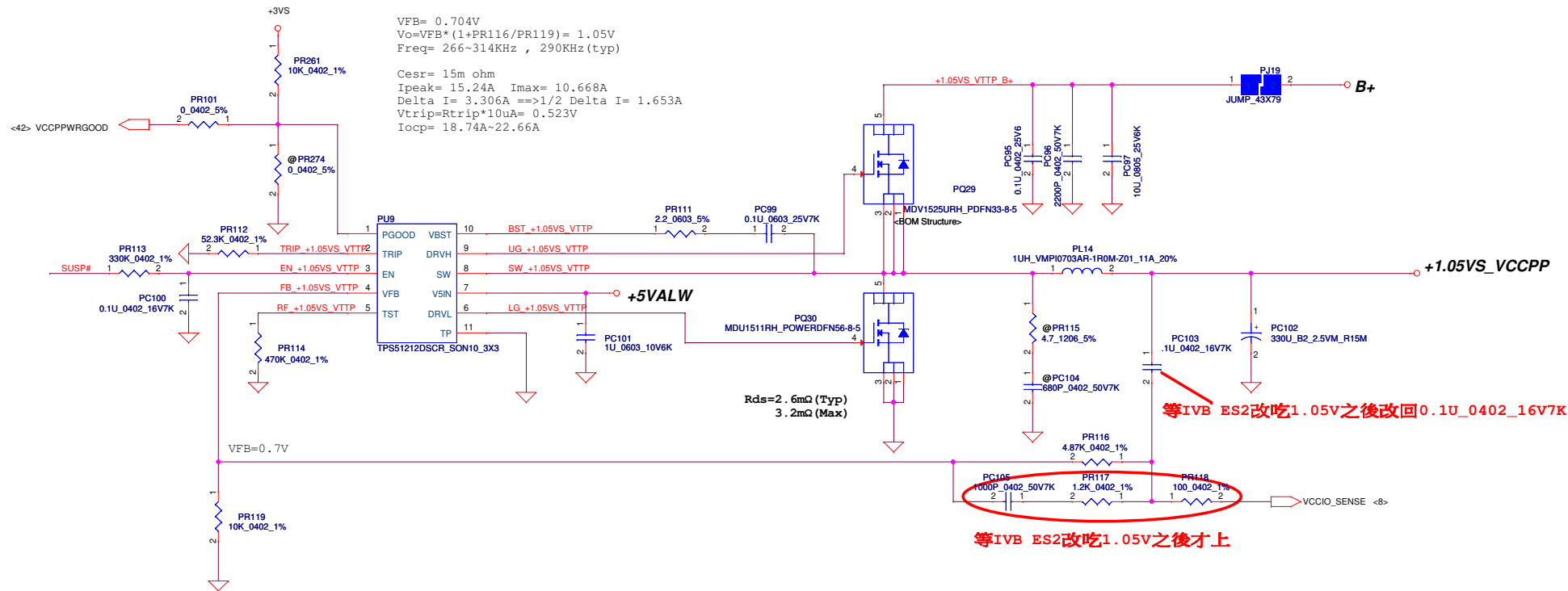
FB=0.6V  
Note: Iload(max)=3.5A

STATE	S3	S5	1.35VP	VTT_REFP	0.675VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)	Off (Discharge)
Note: S3 - sleep ; S5 - power off					

SY8033B enable pin without internal pull down, and RT8061or other 2nd source has 500K pull down resistor!So please review your application if R1>249K will cause enable pin logic high level is not enough

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				Custom	1.0
				Chief River VC	
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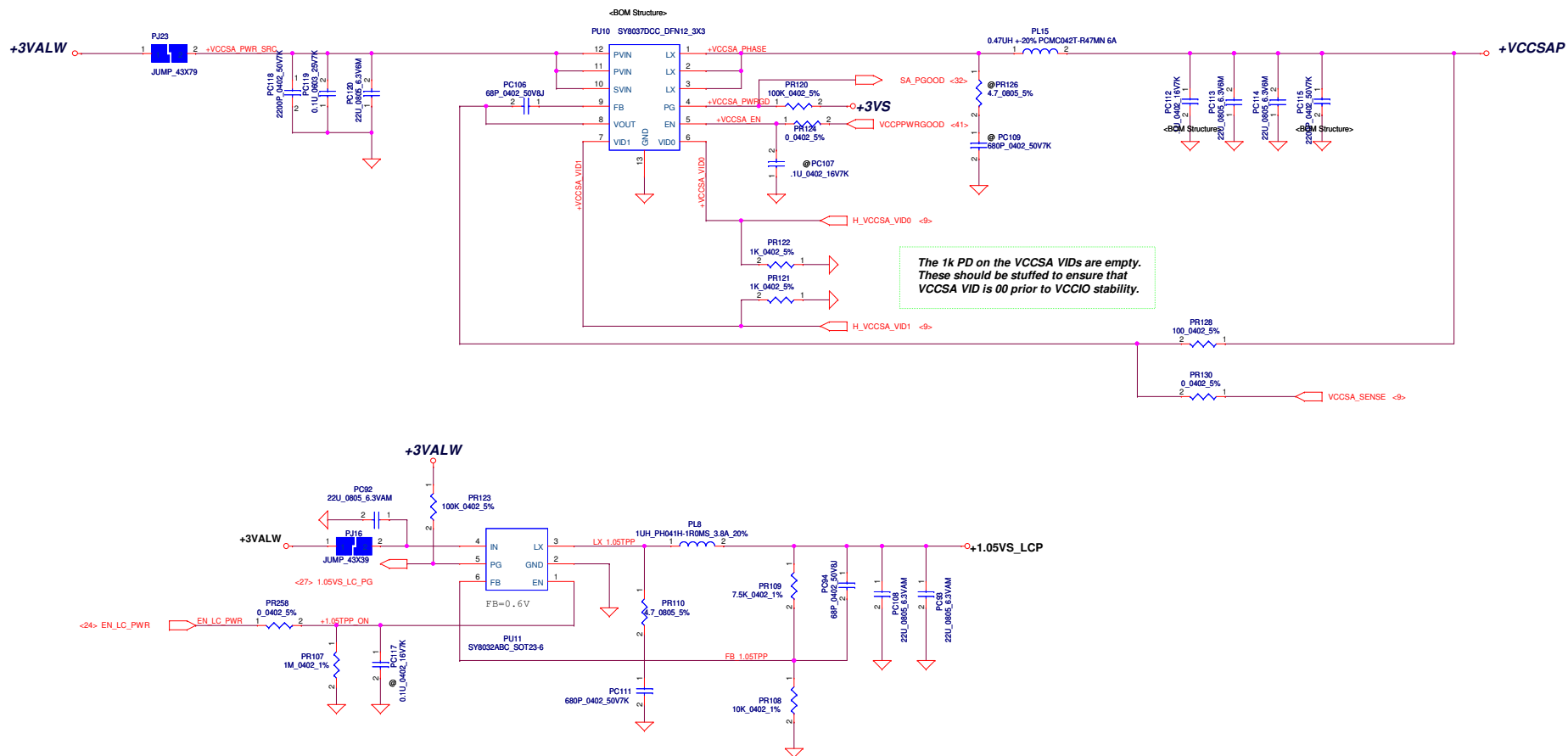




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				Customer	Chief River VC
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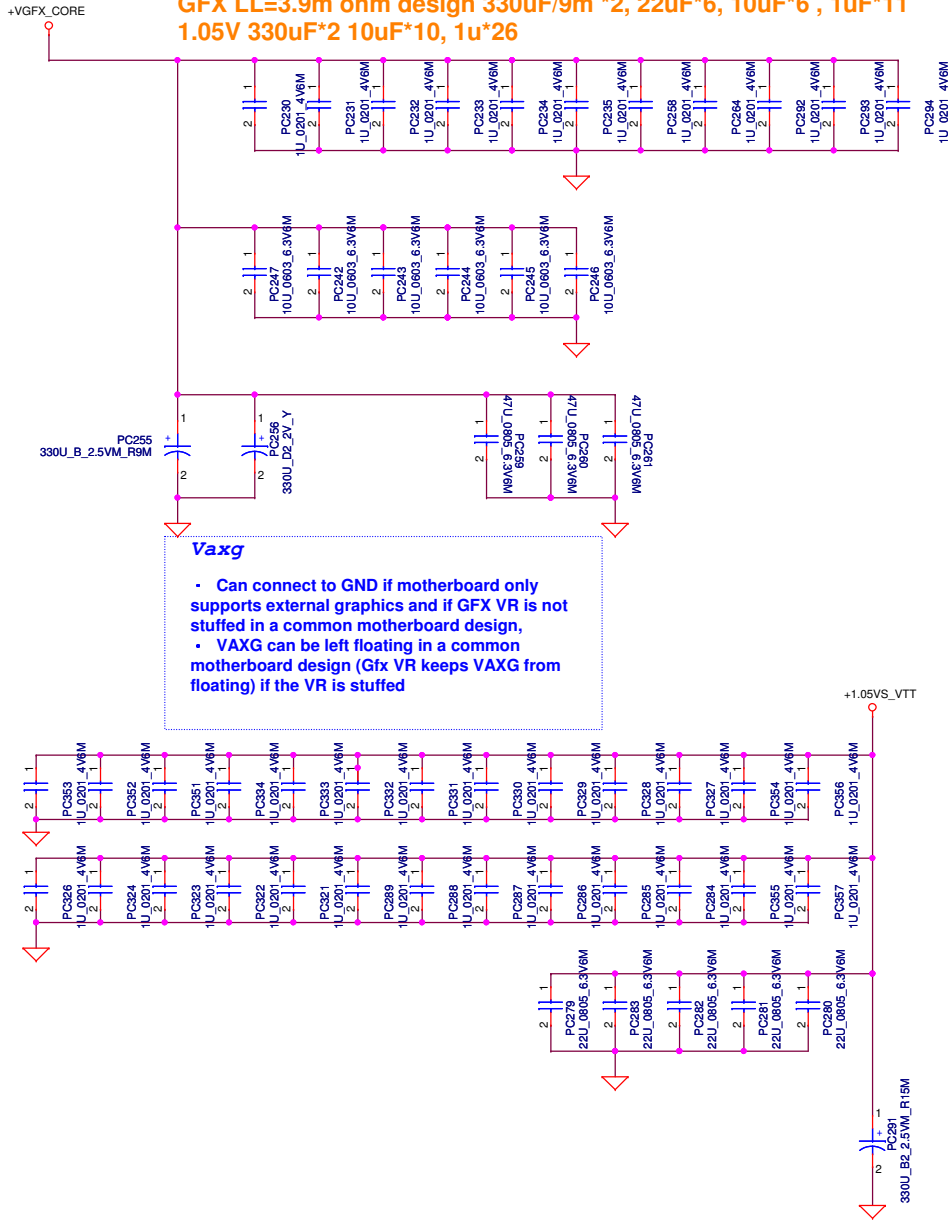
VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network

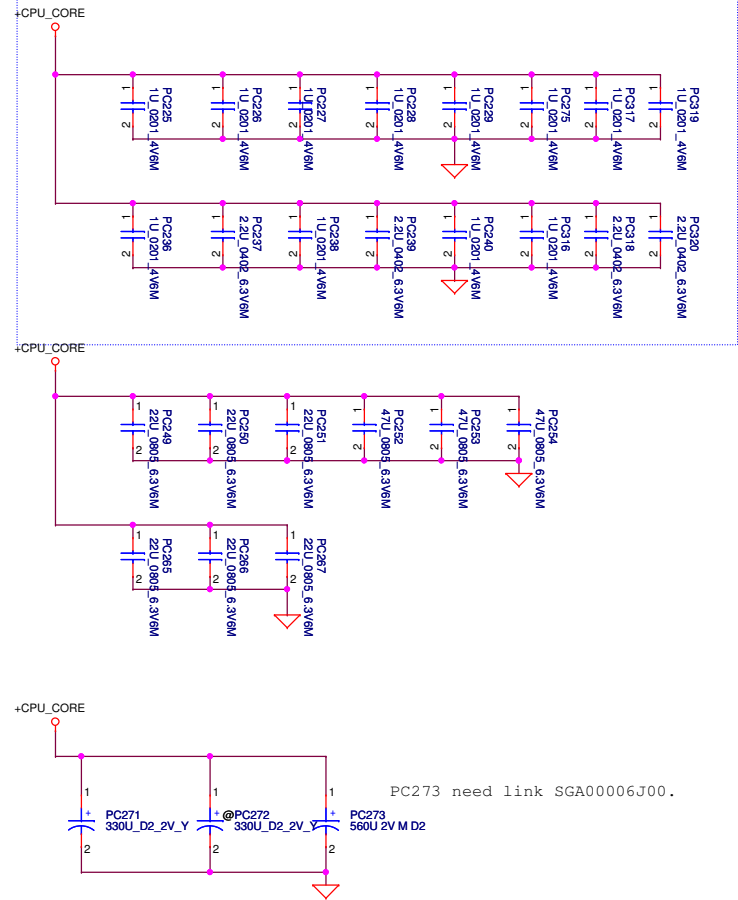




**PWR Rule**  
**CPU LL=2.9m ohm dedign 330uF/9m \*4, 22uF \*12, 2.2uF\*16**  
**GFX LL=3.9m ohm design 330uF/9m \*2, 22uF\*6, 10uF\*6, 1uF\*11**  
**1.05V 330uF\*2 10uF\*10, 1u\*26**

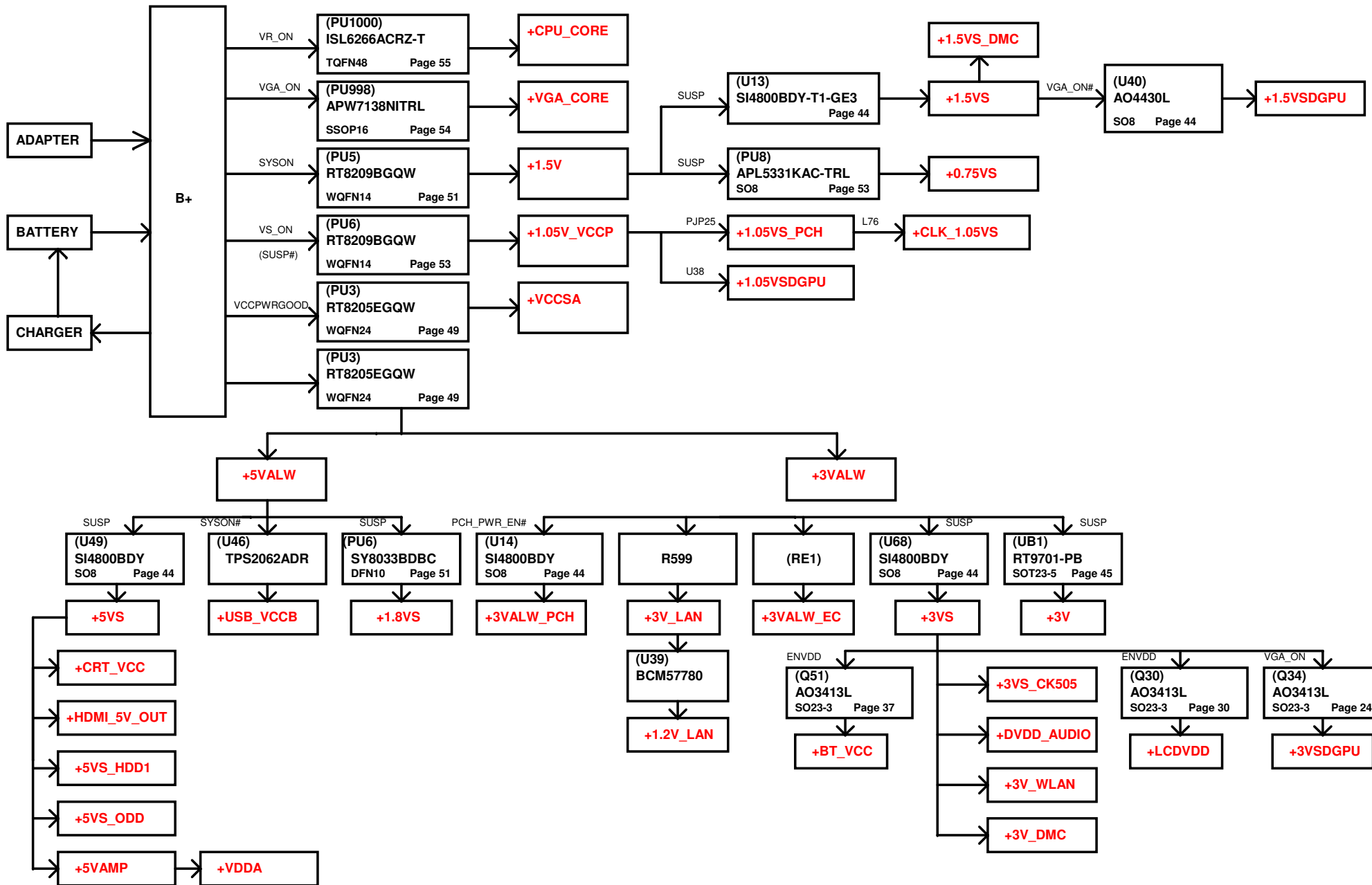


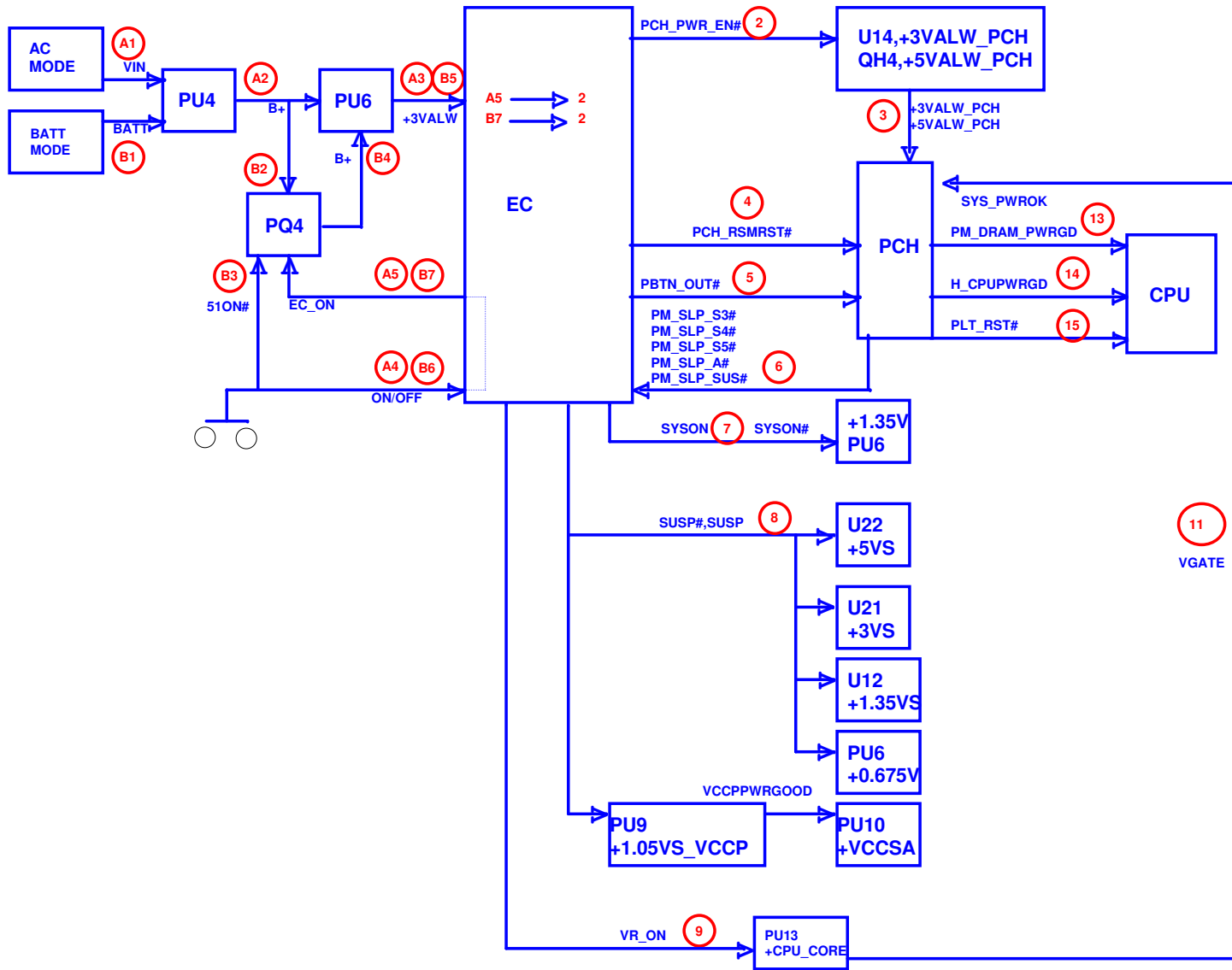
**INTEL Recommend**  
**3\*330uF(1 in other page),12\*22uF, 5 no stuff**  
**from PDDG 1.0**



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## Version change list (P.I.R. List)

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for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Add ADP_ID circuit	Acer will add pull down resistor in adapter to detect ADP_ID.	0.1	36	Add P01 SA003310280 (S IC LMV331IDCKRG4 SC70 5P COMPARATORS) Add P027 SB000009Q80 (S TR 2N7002KW 1N SOT323-3) Add PR13 PR16 SD034100280 (S RES 1/16W 10K +-1% 0402) Add PR14 SD034100380 (S RES 1/16W 100K +-1% 0402)	2011/12/05	EVT2
2	Add Jack_TEMP and PH1 circuit	Acer request add a thermistor on jack of DC in cable to protect jack.	0.1	37	Add PU3 SA000003K300 (S IC G718TMIU SOT23 8P OTP) Add PR30 SD000009900 (S RES 1/16W 46.4K +-1% 0402) Add PR35 SD034953180 (S RES 1/16W 9.53K +-1% 0402) Add PR37 SD034232280 (S RES 1/16W 23.2K +-1% 0402) Del PR127 SD028000080 (S RES 1/16W 0 +-5% 0402)	2011/12/05	EVT2
3	Adjust 1.35V ocp setting and add boost resistor	Adjust 1.35V ocp setting Add boost resistor	0.1	40	Change PR88 to SD000003580 (S RES 1/16W 19.6K +-1% 0402) Change PR86 to SD013220B80 (S RES 1/10W 2.2 +-5% 0603)	2011/12/05	EVT2
4	Add 1.05V boost resistor and adjust output voltage Change choke to 1uH	Add 1.05V boost resistor and adjust output voltage Change choke to 1uH for efficiency of heavy load	0.1	41	Change PR111 to SD013220B80 (S RES 1/10W 2.2 +-5% 0603) Change PR116 to SD034487100 (S RES 1/16W 4.87K +-1% 0402 (LF)) Change PL14 to SH00000KS00 (S COIL 1UH +-20% VMP10703AR-1R0M-201 11A)	2011/12/05	EVT2
5	Adjust GFX frequency	Adjust GFX frequency to 400kHz for reduce ripple	0.1	43	Change PR143 to SD034365280 (S RES 1/16W 36.5K +-1% 0402)	2011/12/05	EVT2
6	Adjust CPU output cap	Adjust CPU output cap for transient	0.1	44	Change PC273 to SGA00006J00 (S POLY C 560U 2V M D2 LESR4.5M SX H1.9) unpop PC272 SGA20331E10 (S POLY C 330U 2V Y D2 LESR9M EEFSX H1.9)	2011/12/05	EVT2
7	Adjust 0.675V enable timing	Adjust 0.675V enable timing	0.1	40	Change PC325 to SE076104K80 (S CER CAP .1U 16V K X7R 0402)	2011/12/05	EVT2
8	Adjust 1.05VS_LCP sequence	Change 1.05VS_LCP from APL5930 to SY8032 for thoundbolt sequence.	0.2	42	Change PU11 to SA000055100 (S IC SY8032ABC SOT23 6P PWM) Change PR107 to SD034100480 (S RES 1/16W 1M +-1% 0402) Add PL8 to SH00000MN00 (S COIL 1UH +-20% PH041H-1R0MS 3.8A) Add PR110 to SD002470B80 (S RES 1/8W 4.7 +-5% 0805) Change PC111 to SE074681K80 (S CER CAP 680P 50V K X7R 0402) Change PC92 to SE000008180 (S CER CAP 22U 6.3V M XES 0805 H1.25) Add PR123 to SD028100380 (S RES 1/16W 100K +-5% 0402) Change PR108 to SD034100280 (S RES 1/16W 10K +-1% 0402) Change PR109 to SD034750180 (S RES 1/16W 7.5K +-1% 0402) Change PC94 to SE071680J80 (S CER CAP 68P 50V J NPO 0402)	2012/01/05	DVT
9							
10	add boost resistor	add Charger boost resistor	0.2	38	Change PR48 to SD013220B80 (S RES 1/10W 2.2 +-5% 0603)	2012/01/05	DVT
11	add boost resistor	add 3V5V boost resistor	0.2	39	Change PR73 and PR74 to SD013220B80 (S RES 1/10W 2.2 +-5% 0603)	2012/01/05	DVT
12	add boost resistor	add CPU and GFX boost resistor	0.2	43	Change PR194 and PR206 to SD013220B80 (S RES 1/10W 2.2 +-5% 0603)	2012/01/05	DVT
13	Change main source	Change main source for reduce component kind	0.2	39	Change PL7 to SH00000MB00 (S COIL 4.7UH +-20% FSDSD0630-H-4R7M=P3 5.5A (7*7*3))	2012/01/05	DVT
14	Adjust Jack_TEMP resistor	Adjust Jack_TEMP resistor, because PCCP change thermistor to 0603 size (TSM1A104F4361RZ)	0.2	37	change PR30 to SD034442280 (S RES 1/16W 44.2K +-1% 0402) change PR37 to SD034215280 (S RES 1/16W 21.5K +-1% 0402)	2012/01/05	DVT
15	Add ADP_ID circuit	Add ADP_ID circuit(65W)	0.2	36	Add PR23 to SD028000080 (S RES 1/16W 0 +-5% 0402) change PR16 to SD034270280 (S RES 1/16W 27K +-1% 0402) Add PC142 to SE074102K80 (S CER CAP 1000P 50V K X7R 0402)	2012/01/05	DVT
16	Change main source	Change main source for 不完全替代 with HW	0.2		change P07,P026,P015,P027,P048 from SB000009Q80 to SB000009610 (S TR SSM3K7002FU 1N SC70-3)	2012/01/31	DVT
17							

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## Version change list (P.I.R. List)

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for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
18	Del ADP_ID circuit	Acer will change adapter type to 音叉式 from PoGo, so del ADP_ID circuit.	0.3	36	Del PU1 SA003310280 (S IC LMV331IDCKRG4 SC70 5P COMPARATORS) Del PQ27 SB000009Q80(S TR 2N7002KW 1N SOT323-3) Del PR13 SD034100280(S RES 1/16W 10K +-1% 0402) Del PR14 SD034100380(S RES 1/16W 100K +-1% 0402) Del PR23 to SD0280000080(S RES 1/16W 0 +-5% 0402) Del PR16 to SD034270280(S RES 1/16W 27K +-1% 0402) Del PC142 to SE074102K80(S CER CAP 1000P 50V K X7R 0402)	2012/03/13	PVT
19					Del PU3 SA000003K300 (S IC G718TM1U SOT23 8P OTP) Del PR30 to SD034442280(S RES 1/16W .44.2K +-1% 0402) Del PR35 SD034953180(S RES 1/16W 9.53K +-1% 0402) Del PR37 to SD034215280(S RES 1/16W 21.5K +-1% 0402) Add PC17 SE076104K80(S CER CAP .1U 16V K X7R 0402) Change PR29 to SD00000AJ80(S RES 1/16W 12.4K +-1% 0402)		
20	Del jack_temp circuit	Acer will change adapter type to 音叉式 from PoGo, so del jack_temp protect circuit.	0.3	37	Del PR28 SD034100380(S RES 1/16W 100K +-1% 0402) Del PR34 SD028100180(S RES 1/16W 1K +-5% 0402) Del PC15 SE000000K80(S CER CAP 1U 6.3V K X5R 0402)	2012/03/13	PVT
21	SPOK change to EC_SPOK	For reduce power consumption of DS3, so close +VSB power in DS3, DS4, DS5.	0.3	37	Change PU10 to SA000050000(S IC SY8037DDCC DFN 12P PWM)	2012/03/13	PVT
22	change VCCSA IC version	SY8037C IC version change to SY8037D for accord with intel VCCSA spec.	0.3	42		2012/03/13	PVT
23	Add snubber	Add snubber of GFX by hw request.	0.3	43	Add PR200 SD001470B80(S RES 1/4W 4.7 +-5% 1206) Add PC190 SE074681K80(S CER CAP 680P 50V K X7R 0402)	2012/03/13	PVT
24	Add MOTOR POWER	HW change motor power solution to PWM.	0.3	45	Add PU17 SA00005NY00(S IC MP2334DD-LF-Z QFN 12P PWM) Add PL28 SH00000N000(S COIL 2.2UH +-20% 1231AS-H-2R2M=P3 1.9A) Add PC366 SE000000U00(S CER CAP 1U 16V K X5R 0402) Add PC367 SE074471K80(S CER CAP 470P 50V K X7R 0402) Add PC368 SE075103K80(S CER CAP .01U 25V K X7R 0402) Add PC369, PC371 SE00000MA00(S CER CAP 4.7U 10V K X5R 0603) Add PC372 SE00000QK00(S CER CAP 10U 25V K X5R 0805 H1.25) Add PC373 SE068102J80(S CER CAP 1000P 25V J NPO 0402) Add PC375, PC376 SE00000G880(S CER CAP 0.1U 25V K X5R 0402) Add PR296 SD034300380(S RES 1/16W 300K +-1% 0402) Add PR297 SD034120280(S RES 1/16W 12K +-1% 0402) Add PR298 SD028100A00(S RES 1/16W 10 +-5% 0402) Add PR300 SD034432380(S RES 1/16W 432K +-1% 0402) Add PR301 SD000000680(S RES 1/16W 8.45K +-1% 0402) Add PR302, PR307, PR308 SD028100380(S RES 1/16W 100K +-5% 0402) Add PR303 SD000002300(S RES 1/16W 7.68K +-1% 0402) Add PR304 SD034576180(S RES 1/16W 5.76K +-1% 0402) Add PR299, PR305, PR306 SD028100280(S RES 1/16W 10K +-5% 0402) Add PQ49 SB00000DH00(S TR DMN66D0LDW-7 2N SOT363-6)	2012/03/13	PVT
25							
26							
27							
28	Adjust HW throttling point	Because thunder bolt adapter is 40W, OCP 130% adjust HW throttling to 125% 50W recover point 38W	0.3	37	Change PR33 to SD034165180(S RES 1/16W 1.65K +-1% 0402)	2012/03/13	PVT
29							
30							
31							
32							
33							
34							

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
0919(In Layout)							
1.Update R,C 0201,0402,0603,0805,1206 PCB footprint to small size					0928	1013	
2.Swap DDR Data BUS					1.Change RTC cap from 1U 0603 to 1U 0402:C502,C516	1.Add Step Motor circuit	
					2.Remove FAN some parts:R753,C788,D51,D52	2.On Board iSSD:i100 change to mSATA SSD	
					3.Change USB connector foot print to TAIWI_USB005-107CRL-TW_10P-T	3.WLAN change to on board:MD225	
					4.Change C196,C387,C735,C102 to 0.1uF_0201_10V6K:SE00000SV00	4.Change Card Reader	
					5.Remove L2	PCIE from Port4 to Port1	
0920						CLK from Port5 to Port4	
1.Change U74,U21,U22 mos to 3*3 thermal pad package:SB00000GW00						5.Change mSATA SATA port from Port1 to Port0	
						6.Add USB port 12 for mSATA	
0921						7.Remove D11,D12 and C357,C358 (HDMI RF request)	
1.TB chip:U66 footprint add "-NH" for Non HDI					0929	8.C396,C324 change to 0201	
2.1.8p_0402:C402,C404 change to 75ohm_0402:R263,R264					1.Remove C510,C511	9.Remove C472 for +5VALW source cap	
					2.Remove Camera Choke:L7,R13,R14		
					3.Q1,Q2 change to DMN66D0LDW-7_SOT363-6:SB00000DH00	1014	
					4.R273,R394 change from 0_0603 to 0_0402	1.Remove DPST_PWM buffer:U13,R783,R85	
					5.Remove Step Motor SW1	2.Change +3VS_FULLL cap:C475,C466 from 0.1uF_0402 to 0201	
					6.Change LED/B connector from 8 pin to 4 pin	3.Change SATA cap:C621,C622,C623,C624 from 0.01uF_0402 to 0201	
					7.Change Jumper from 43*118 to 43*79		
					=>J2,J8,J10,J11		
0922							
1.Change C1457,C1505 form 1.8P 0402 to 0201:SE00000HB80					0930		
2.Del DDR CHA,B no use CLK1,CLK1# circuit					1.Remove +VCCSA cap:C1182,C1183	1017	
3.Change C606,C607 from D2 330uF to B2 330uF 2.5V ESR 15mohm:SGA00004400					2.Remove +USB3_VCCA cap:C390	1.Add power source of +VCCAFDI_VRM at P.20	
4.Swap total KB connector:JKB1 pin define					3.Change C427,C428 to 0.1U_0201_10V6K	2.Update DS3,AOAC control signal connected to EC	
					4.Add ESD diode:D6 for TP SMBUS		
					5.Change L65 to 220ohm 3A 0805	1018~1021	
					6.Swap DDR ChB Data,DQS# 6,7		
					7.Change U12 mos to 3*3 thermal pad package:SB00000GW00	1024	
0923						1.Remove R130	
1.Add DS3 function:SUSWARN#,SUSACK#,EC_DRAMRST_GATE					8.Remove X2,C1361,C1362	2.Define DRAM ID	
2.Add Motor function:Motor_IN1,Motor_IN2,Motor_IN3,Motor_IN4,					9.C378+C375 change to 10uF*1	3.Update TB schematic	
Door_Det_L,Button: KSI0 & KSO10					10.C460+C459 change to 10uF*1	4.Swap USB2.0 ESD pin	
3.Remove PCH NCTF test point					11.Remove C986,C987,C989,C990	5.Add on/off BTN for debug	
4.HDMI Fuse:F1 change to P5WS5 use footprint:F_1812					=>Add 1uF 0201*10		
5.Remove HDMI common mode choke:L36,L38,L39,L40						1027	
6.Change 0.1uF_0402_16V7K to 0.1uF_0201_10V6K:SE00000SV00					1003	1.Swap JTP1 pin for new module	
=>C521,C520,C526,C449,C523,C537,C541,C494,C495,C490,C497,C771,C522,C471,C473					1.Change EC side GPIO:PWR_LED to PWR_LED#,Remove Q32,R512	2.Gerber schematic	
7.Change 0.01uF_0402_16V7K to 0.01uF_0201_10V7K:SE172103K80					2.For separate coaxial and wire,update eDP MB connector pin define		
=>C425,C462					3.Remove JLED1 connector		
8.Change C751,C752 to B2 220uF 2.5V ESR 15mohm:SGA00004500					4.Change C427:0.1U_0402_16V4Z to 0.1U_0201_10V6K:SE00000VS00	1028	
						For Load BOM	
0924						1.Update Block Diagram	
1.Make MB to Audio/B connector pin define					1005	2.Update CPU,PCH part number	
2.Change RP 8.2K:R256,R262,R276,R386 to 8.2K_0402					1.Swap DDR ChB Data,DQS# 6,7	3.Update BOM config	
3.Change RP 10K:R386 to 10K_0402					2.Change PCH PCIE 0.1U_0402_16V7K to 0.1U_0201_10V6K:SE00000SV00		
4.Update TB schematic p.24,25,27					=>C572,C573,C617,C618,C681,C682,C683,C684,C685,C686,C687,C688	1101	
5.Change Q64,Q68 from AO3419L:SB000006R10 to AP2301GN-HF:SB000007H10					2.Change eDP cap from 0.1U_0402_16V7K to 0.1U_0201_10V6K:SE00000SV00	1.For整合料	
6.Integration of all 2N7002 SOT23 parts to SSM3K7002F_SC59-3:SB000009080					=>C910,C911,C912,C913,C914,C915	2.Combine PWR schematic	
=>Q74,Q20,Q1,Q2,Q32,Q16,Q17,Q14,Q37,Q7,Q21,Q23,Q24,Q5,Q34,Q29,Q60,Q66,Q67,Q72					3.Add R80:0ohm of H_CPU_PWRGD for ESD request	3.A test SMT schematic	
Not yet=>Q6,Q78,Q79					4.Remove On Board WLAN:MD225		
					5.Add Motor parts (Not Ready)		
0925					6.Add iSSD i100 parts (Not Ready)		
1.Delete LVDS function,Combine eDP,Card Reader function to JLVDS1							
Remove:R259,R260,R285,R286,R156,R157,TXCLK+,-,TX0+1,TX1+,-,TX2+,-,DDC CLK,DATA					1006		
Remove:C462,C425,C412,L20,only place PU:R271,R272,PD:R270,R280					1.Change R754,R751 0ohm from 0603 to 0402		
2.Change all SSM3K7002F_SC59-3:SB000009080 to SSM37K002FU_SC70-3:SB000009610					2.Change C484 0.1U from 0603 to 0402		
=>Q74,Q20,Q1,Q2,Q32,Q16,Q17,Q14,Q37,Q7,Q21,Q23,Q24,Q5,Q34,Q29,Q60,Q66,Q67,Q72					3.For DS3,Change power source from +3VALW_PCH to +VCCSUS3_3		
Not yet=>Q6,Q78,Q79					4.Change R629 from 0_0805 to 0_0402		
3.Change 10U_0805_6.3V6M:SE093106M80 to 10U_0603_6.3V6M:SE000005T80					5.Change SATA cap from 0.1U_0402_16V7K to 0.01U_0201_10V7K		
=>C754,C543,C418,C465					=>C621~C628		
4.Remove 0_0603_5%:R416,R421,R426,R327							
0926							
1.Change HDMI level shift Q16,Q17 to DMN66D0LDW-7_SOT363-6:SB00000DH00							
2.Modify TB schematic 0402 cap to 0201							
0927							
1.Remove J7					1010		
2.Change C599 330U D2 2V ESR 9mohm to 330U B2 2.5V ESR 15mohm:SGA00004400					1.Add BATT_RST#,VR_LEFT,VR_RIGHT pin		
3.Change EC +3VALW_EC					2.Add iSSD i100 128GB*2 schematic		
0.1U_0402_16V4Z to 0.1U_0201_10V6K:SE00000SV00					3.Add USB_HPD# pin		
=>C1198,C1199,C1200,C1201,C1204							
1000P_0402_50V7K to 1000P_0201_16V7K:SE000007U80							
=>C1202,C1203					1011		
4.Remove R329					1.Add Battery Reset function		
5.Change C751,C752 to 22U_0805_6.3V6M:SE000000I10					2.Swap USB2.0,3.0 choke for connector side 順線		
6.Remove J4(one of +1.05VS_VTT to +1.05VS_PCH jumper)							

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